PIC18F6310/6410/8310/8410 Rev. B3 Silicon Errata

The PIC18F6310/6410/8310/8410 Rev. B3 parts you have received conform functionally to the Device Data Sheet (DS39635**B**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F6310/6410/8310/8410 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

All of the issues listed here will be addressed in future revisions of the PIC18F6310/6410/8310/8410 silicon.

The following silicon errata apply only to PIC18F6310/6410/8310/8410 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F6310	0000 1011 111	0 0011
PIC18F6410	0000 0110 111	0 0011
PIC18F8310	0000 1011 110	0 0011
PIC18F8410	0000 0110 110	0 0011

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: MSSP

In its current implementation, the I^2C™ Master mode operates as follows:

a) The Baud Rate Generator for I^2C in Master mode is slower than the rates specified in Table 16-3 of the Device Data Sheet.

For this revision of silicon, use the values shown in Table 1 in place of those shown in Table 16-3 of the Device Data Sheet. The differences are shown in **bold** text.

b) Use the following formula in place of the one shown in Register 16-4 (SSPCON1) of the Device Data Sheet for bit description SSPM3:SSPM0 = `1000`.

$$SSPADD = INT((F_{CY}/F_{SCL}) - (F_{CY}/1.111\ MHz)) - 1$$

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: I^2C™ CLOCK RATE w/BRG

FOSC	FCY	FCY * 2	BRG Value	FSCL (2 Rollovers of BRG)
40 MHz	10 MHz	20 MHz	**0Eh**	400 kHz(1)
40 MHz	10 MHz	20 MHz	**15h**	312.5 kHz
40 MHz	10 MHz	20 MHz	**59h**	100 kHz
16 MHz	4 MHz	8 MHz	**05h**	400 kHz(1)
16 MHz	4 MHz	8 MHz	**08h**	308 kHz
16 MHz	4 MHz	8 MHz	**23h**	100 kHz
4 MHz	1 MHz	2 MHz	**01h**	333 kHz(1)
4 MHz	1 MHz	2 MHz	**08h**	100 kHz
4 MHz	1 MHz	2 MHz	00h	1 MHz(1)

Note 1: The I^2C™ interface does not conform to the 400 kHz I^2C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

2. Module: MSSP

When the MSSP is configured for SPI Master mode, the SDO pin cannot be disabled by setting the TRISC<5> bit. The SDO pin always outputs the content of SSPBUF regardless of the state of the TRIS bit.

In Slave mode with Slave Select enabled, SSPM3:SSPM0 = 0010 (SSPCON1<3:0>), the SDO pin can be disabled by placing a logic high level on the $\overline{SS}$ pin (RF7).

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: MSSP

After an I^2C transfer is initiated, the SSPBUF register may be written for up to 10 T_{CY} before additional writes are blocked. The data transfer may be corrupted if SSPBUF is written during this time.

The WCOL bit is set any time an SSPBUF write occurs during a transfer.

Work around

Avoid writing SSPBUF until the data transfer is complete, indicated by the setting of the SSPIF bit (PIR1<3>).

Verify the WCOL bit (SSPCON1<7>) is clear after writing SSPBUF to ensure any potential transfer in progress is not corrupted.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: MSSP

In 10-bit Addressing mode, when a Repeated Start is issued followed by the high address byte and a write command (R/$\overline{W}$ = 0), an ACK is not issued.

Work around

There are two work arounds available:

1. Single-Master Environment:
   In a single-master environment, the user must issue a Stop, then a Start, followed by a write to the address high, then the address low followed by the data.
2. Multi-Master Environment:
   In a multi-master environment, the user must issue a Repeated Start, send a dummy write command to a different address, issue another Repeated Start and then send a write to the original address. This procedure will help maintain control of the bus.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: MSSP

I^2C Receive mode should be enabled (i.e., RCEN bit should be set) only when the system is idle (i.e., when ACKEN, RCEN, PEN, RSEN and SEN all equal zero). It should not be possible to set the RCEN bit when the system is not idle, however, the RCEN bit can be set under this circumstance.

Work around

Wait for the system to become idle before setting the RCEN bit. This requires a check for the following bits to be clear:

ACKEN, RCEN, PEN, RSEN and SEN.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: CCP

When operating either Timer1 or Timer3 as a counter with a prescale value other than 1:1 and operating the CCP in Compare mode with the Special Event Trigger (CCP1CON bits CCP1M3:CCP1M0 = 1011), the Special Event Trigger Reset of the timer occurs as soon as there is a match between TMRxH:TMRxL and CCPR1H:CCPR1L.

This differs from the PIC18F452, where the Special Event Trigger Reset of the timer occurs on the next prescaler output pulse after the match between TMRxH:TMRxL and CCPR1H:CCPR1L.

Work around

To achieve the same timer Reset period on the PIC18F8410 family as the PIC18F452 family for a given clock source, add 1 to the value in CCPR1H:CCPR1L. In other words, if CCPR1H:CCPR1L = x for the PIC18F452, to achieve the same Reset period on the PIC18F8410 family, CCPR1H:CCPR1L = x + 1, where the prescale is 1, 2, 4 or 8 depending on the T1CKPS1:T1CKPS0 bit values.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: CCP

The CCP1 and CCP2 configured for PWM mode, with 1:1 Timer2 prescaler and duty cycle set to the period minus 1, may result in the PWM output(s) remaining at a logic low level.

Clearing the PR2 register to select the fastest period may also result in the output(s) remaining at a logic low output level.

Work around

To ensure a reliable waveform, verify that the selected duty cycle does not equal the 10-bit period minus 1 prior to writing these locations, or use 1:4 or 1:16 Timer2 prescale. Also, verify the PR2 register is not written to 00h.

All other duty cycle and period settings will function as described in the Device Data Sheet.

The CCP modules remain capable of 10-bit accuracy.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: A/D

The A/D offset is greater than the specified limit in Table 26-25 of the Device Data Sheet. The additional Parameter A06A and updated conditions and limits are shown in **bold** text in Table 2.

Work around

Three work arounds exist.

1. Configure the A/D to use the VREF+ and VREF- pins for the voltage references. This is done by setting the VCFG<1:0> bits (ADCON1<5:4>).
2. Perform a conversion on a known voltage reference voltage and adjust the A/D result in software.
3. Increase system clock speed to 40 MHz and adjust A/D settings accordingly. Higher system clock frequencies decrease offset error.

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 2: A/D CONVERTER CHARACTERISTICS: PIC18F6310/6410/8310/8410 (INDUSTRIAL) PIC18LF6310/6410/8310/8410 (INDUSTRIAL)

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
A06A	**EOFF**	**Offset Error**	**—**	**—**	**<±1.5**	**LSb**	**VREF = VREF+ and VREF-**
A06	EOFF	Offset Error	—	—	**<±3.5**	LSb	**VREF = VSS and VDD**

9. Module: BOD

The BOD module may reset below the minimum operating voltage of the device when configured for BORV1:BORV0 = 11. The updated Reset voltage specifications are shown in **bold** in Table 3.

TABLE 3: BROWN-OUT RESET VOLTAGE

Param No.	Sym	Characteristic	Min	Typ	Max	Unit
D005	VBOR	**Brown-out Reset Voltage**				
		PIC18LF6310/6410/8310/8410				
		BORV1:BORV0 = 11	**N/A**	2.05	**N/A**	V

Work around

Use the next higher BOD voltage setting to ensure a low VDD is detected above 2.0V.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTAx register is set), an ongoing transmission's timing can be corrupted if the TX9D bit (for the next transmission) is not written immediately following the setting of TXxIF. This is because any write to the TXSTAx register results in a reset of the Baud Rate Generator which will effect any ongoing transmission.

Work around

Load TX9D just after TXxIF is set, either by polling TXxIF or by writing TX9D at the beginning of the Interrupt Service Routine, or only write to TX9D when a transmission is not in progress (TRMT = 1).

Date Codes that pertain to this issue:

All engineering and production devices.

11. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTAx register is set), the second byte may be corrupted if it is written into TXREGx immediately after the TMRT bit is set.

Work around

Execute a software delay, at least one-half the transmission's bit time, after TMRT is set and prior to writing subsequent bytes into TXREGx.

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: AUSART

The AUSART for PIC18F6310/6410/8310/8410 devices may not recognize a received Stop bit if the combined error rate is too high.

Work around

1. Increase the baud rate of the device by decrementing the SPBRGHx:SPBRGx register pair value by one. Verify that the new baud rate does not exceed the maximum combined error rate of the application.
2. Configure the transmitter to send two Stop bits.

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: Timer1/Timer3

When Timer1 or Timer3 is configured for external clock source and the CCPxCON register is configured with 0x0B (Compare mode, trigger special event), the timer is not reset on a Special Event Trigger.

Work around

Modify firmware to reset the Timer1/Timer3 registers upon detection of the compare match condition — TMRxL and TMRxH.

Date Codes that pertain to this issue:

All engineering and production devices.

14. Module: Timer1/Timer3

When Timer1 or Timer3 is in External Clock Synchronized mode and the external clock period is between 1 and 2 TCY, interrupts will occasionally be skipped.

Work around

Avoid using an external clock with a period (1/frequency) between 1 and 2 TCY.

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: Timer1/Timer3

When Timer1/Timer3 is operating in 16-bit mode and the prescale setting is not 1:1, a write to the TMR1H/TMR3H Buffer registers may lengthen the duration of the period between the increments of the timer for the period in which TMR1H/TMR3H was written.

Work around

Two work arounds are available: 1) Stop Timer1/Timer3 before writing the TMR1H/TMR3H registers; 2) Write TMR1L/TMR3L immediately after writing TMR1H/TMR3H.

Date Codes that pertain to this issue:

All engineering and production devices.

16. Module: Interrupts

If an interrupt occurs during a two-cycle instruction that modifies the STATUS, BSR or WREG register, the unmodified value of the register will be saved to the corresponding Fast Return (Shadow) register and upon a fast return from the interrupt, the unmodified value will be restored to the STATUS, BSR or WREG register.

For example, if a high priority interrupt occurs during the instruction, `MOVFF TEMP, WREG`, the `MOVFF` instruction will be completed and WREG will be loaded with the value of `TEMP` before branching to ISR. However, the previous value of WREG will be saved to the Fast Return register during ISR branching. Upon return from the interrupt with a fast return, the previous value of WREG in the Fast Return register will be written to WREG. This results in WREG containing the value it had before execution of `MOVFF TEMP, WREG`.

Affected instructions are:

`MOVFF Fs, Fd`
where `Fd` is WREG, BSR or STATUS;

`MOVSF Zs, Fd`
where `Fd` is WREG, BSR or STATUS; and

`MOVSS [Zs], [Zd]`
where the destination is WREG, BSR or STATUS.

Work around

1. Assembly Language Programming:

a) If any two-cycle instruction is used to modify the WREG, BSR or STATUS register, do not use the `RETFIE FAST` instruction to return from the interrupt. Instead, save/restore WREG, BSR and STATUS via software per Example 9-1 in the Device Data Sheet. Alternatively, in the case of `MOVFF`, use the `MOVF` instruction to write to WREG instead. For example, use:

```
MOVF   TEMP, W
MOVWF  BSR
```

instead of: `MOVFF TEMP, BSR`.

b) As another alternative, the following work around shown in Example 1 can be used. This example overwrites the Fast Return register by making a dummy call to `Foo` with the fast option in the high priority service routine.

EXAMPLE 1:

```
ISR @ 0x0008
  CALL Foo, FAST; store current value of WREG, BSR, STATUS for a second time
Foo:
  POP         ; clears return address of Foo call
  :           ; insert high priority ISR code here
  :
  RETFIEFAST
```

2. C Language Programming: The exact work around depends on the compiler in use. Please refer to your C compiler documentation for details.

   If using the Microchip MPLAB® C18 C Compiler, define both high and low priority interrupt handler functions as "low priority" by using the `pragma interruptlow` directive. This directive instructs the compiler to not use the `RETFIE FAST` instruction. If the proper high priority interrupt bit is set in the IPRx register, then the interrupt is treated as high priority in spite of the `pragma interruptlow` directive.

   The code segment shown in Example 2 demonstrates the work around using the C18 compiler. An optimized C18 version is also provided in Example 3. This example illustrates how it reduces the instruction cycle count from 10 cycles to 3.

Date Codes that pertain to this issue:

All engineering and production devices.

EXAMPLE 2:

```
#pragma interruptlow MyLowISR
void MyLowISR(void)
{
    // Handle low priority interrupts.
}

// Although MyHighISR is a high priority interrupt, use interruptlow pragma so that
// the compiler will not use retfie FAST.

#pragma interruptlow MyHighISR
void MyHighISR(void)
{
    // Handle high priority interrupts.
}

#pragma code highVector=0x08
void HighVector (void)
{
    _asm goto MyHighISR _endasm
}
#pragma code /* return to default code section */

#pragma code lowVector=0x18
void LowVector (void)
{
    _asm goto MyLowISR _endasm
}
#pragma code /* return to default code section */
```

EXAMPLE 3:

```
#pragma code high_vector_section=0x8
void high_vector (void)
{
  _asm
    CALL high_vector_branch, 1
  _endasm
}

void high_vector_branch (void)
{
  _asm
    POP
    GOTO high_isr
  _endasm
}

#pragma interrupt high_isr
void high_isr (void)
{
  ...
}
```

17. Module: External Memory Bus (EMB)

When the EMB is enabled and configured for 8-bit mode and EBDIS (MEMCON<7>) is clear, the BA0 pin continues to be active during table read and table write operations to internal program memory addresses. Under these conditions, BA0 should be inactive.

Work around

Set the EBDIS bit when performing table operations to internal program memory.

Date Codes that pertain to this issue:

All engineering and production devices.

18. Module: EUSART

The EUSART auto-baud feature may periodically measure the incoming baud rate incorrectly. The rate of incorrect baud rate measurements will depend on the frequency of the incoming synchronization byte and the system clock frequency.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

19. Module: EUSART

In Synchronous mode (SYNC = 1) with clock polarity high (SCKP = 1), the EUSART transmits a shorter than expected clock on the CKx pin for bit 0.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

20. Module: EUSART

In Synchronous mode, EUSART baud rates using SPBRGx values of '0' and '1' may not function correctly.

Work around

Use another baud rate configuration to generate the desired baud rate.

Date Codes that pertain to this issue:

All engineering and production devices.

21. Module: MSSP

In an I^2C™ system with multiple slave nodes, an unaddressed slave may respond to bus activity when data on the bus matches its address. The first occurrence will set the BF bit. The second occurrence will set the BF and SSPOV bits. In both situations, the SSPIF bit is not set and an interrupt will not occur. The device will vector to the Interrupt Service Routine only if the interrupt is enabled and an address match occurs.

Work around

The I^2C slave must clear the SSPOV bit after each I^2C address match to maintain normal operation.

Date Codes that pertain to this issue:

All engineering and production devices.

22. Module: MSSP

In I^2C Master mode, the BRG value of '0' may not work correctly.

Work around

Use a BRG value greater than '0' by setting SSPADD ≥ 1.

Date Codes that pertain to this issue:

All engineering and production devices.

23. Module: MSSP

In I^2C Master mode, the RCEN bit is set by software to begin data reception and cleared by the peripheral after a byte is received. After a byte is received, the device may take up to 80 T_{CY} to clear RCEN and 800 T_{CY} when using MPLAB® ICD 2 and MPLAB ICE emulators.

Work around

Single byte receptions are typically not affected, since the delay between byte receptions is typically long enough for the RCEN bit to clear. For multiple byte receptions, the software must wait until the bit is cleared by the peripheral before the next byte can be received.

Date Codes that pertain to this issue:

All engineering and production devices.

24. Module: MSSP

Setting the SEN bit initiates a Start sequence on the bus, after which, the SEN bit is cleared automatically by hardware. If the SEN bit is set again (without an address byte being transmitted), a Start sequence will not commence and the SEN bit will not be cleared. This condition causes the bus to remain in an active state. The system is Idle when ACKEN, RCEN, PEN, RSEN and SEN are clear.

Work around

Set the PEN or RSEN bit to transmit a Stop or Repeated Start sequence, although the SEN bit may still be set, indicating the bus is active. After the sequence has completed, the PEN, RSEN and SEN bit will be clear, indicating the bus is Idle. Clearing and setting the SSPEN bit will also reset the I^2C peripheral and clear the PEN, RSEN and SEN status bits.

Date Codes that pertain to this issue:

All engineering and production devices.

25. Module: MSSP

In SPI mode, the Buffer Full flag (BF bit in the SSPSTAT register), the Write Collision Detect bit (WCOL bit in SSPCON1) and the Receive Overflow Indicator bit (SSPOV in SSPCON1) are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPCON1 register).

For example, if SSPBUF is full (BF bit is set) and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

Work around

Ensure that if the buffer is full, SSPBUF is read (thus clearing the BF flag) and WCOL is clear before disabling the MSSP module. If the module is configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

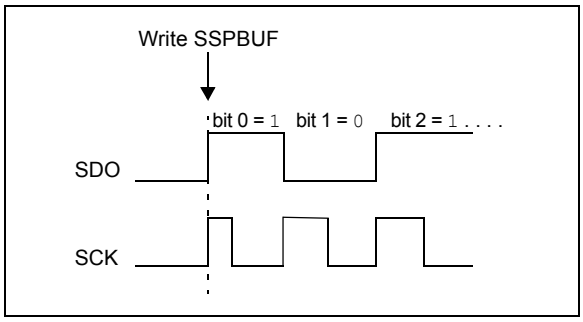
Date Codes that pertain to this issue:

All engineering and production devices.

26. Module: MSSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCK pulse may occur on the first bit of the transmitted/received data (Figure 1).

FIGURE 1: SCK PULSE VARIATION USING TIMER2/2



Work around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit and then turn Timer2 back on. Refer to Example 4 for sample code.

EXAMPLE 4: AVOIDING THE INITIAL SHORT SCK PULSE

```
LOOP BTFSS   SSPSTAT, BF    ;Data received?
                            ;(Xmit complete?)
     BRA     LOOP           ;No
     MOVF    SSPBUF, W      ;W = SSPBUF
     MOVWF   RXDATA         ;Save in user RAM
     MOVF    TXDATA, W      ;W = TXDATA
     BCF     T2CON, TMR2ON  ;Timer2 off
     CLRF    TMR2           ;Clear Timer2
     MOVWF   SSPBUF         ;Xmit New data
     BSF     T2CON, TMR2ON  ;Timer2 on
```

Date Codes that pertain to this issue:

All engineering and production devices.

27. Module: Timer1 (Asynchronous Counter)

When writing to the TMR1H register, under specific conditions, it is possible that the TMR1L register will miss a count while connected to the external oscillator via the T1OSO and T1OSI pins.

When Timer1 is started, the circuitry looks for a falling edge before a rising edge can increment the counter. Writing to the TMR1H register is similar to starting Timer1; therefore, the former logic stated applies any time the TMR1H register is written. If the TMR1H register is not completely written to during the high pulse of the external clock, then the TMR1L register will miss a count due to the circuit operation stated previously. The high pulse of a 32.768 kHz external clock crystal yields a 15.25 μs window for the write to TMR1H to occur. The amount of instructions that can be executed within this window is frequency dependent, as shown in Table 4 below.

Work around

Operating Conditions: FOSC ≥ 4 MHz, no wake-ups from Sleep, Timer1 interrupt enabled, global interrupts enabled.

The code excerpts in Example 5 and Example 6 show how the TMR1H register can be updated while the external clock (32.768 kHz) is still on its high pulse.

The importance of the code examples is that the **bold** instructions are executed within the first 15.25 μs high pulse on the external clock after the Timer1 overflow occurs. This will allow the TMR1L register to increment correctly.

TABLE 4: FREQUENCY DEPENDENT INSTRUCTION EXECUTION AMOUNTS

FOSC	TCY (μs)	TCY within 15.25 μs
1 MHz	4	3.81
2 MHz	2	7.63
4 MHz	1	15.25
8 MHz	0.5	30.5
16 MHz	0.25	61
20 MHz	0.2	76.25
40 MHz	0.1	152.5

EXAMPLE 5: PIC18 HIGH PRIORITY INTERRUPT SERVICE ROUTINE

```
ISR @ 0x0008                    ; (3-4Tcy), fixed interrupt latency

    BRA     HIGHINT             ; (2Tcy), go to high priority interrupt routine

HIGHINT
    BTFSC   PIR1, TMR1IF        ; (1Tcy), did a Timer1 overflow occur?
    BSF     TMR1H, 7            ; (1Tcy) Yes, reload for a 1 second overflow

    RETFIE  FAST
```

Total = 7-8 TCY (if Timer1 overflow occurred)

EXAMPLE 6: PIC18 LOW PRIORITY INTERRUPT SERVICE ROUTINE

```
ISR @ 0x0018                    ; (3-4Tcy), fixed interrupt latency

    MOVFF   STATUS, STATUS_TEMP ; (2Tcy), save STATUS register
    MOVFF   WREG, WREG_TEMP     ; (2Tcy), save working register, refer to note 1
    MOVFF   BSR, BSR_TEMP       ; (2Tcy), save BSR register, refer to note 1

    BTFSS   PIR1, TMR1IF        ; (2Tcy), did a Timer1 overflow occur?
    BRA     EXIT                ; No
    BSF     TMR1H, 7            ; (1Tcy) Yes, reload for a 1 second overflow

EXIT
    MOVFF   BSR_TEMP, BSR       ;restore BSR register, refer to note 1
    MOVFF   WREG_TEMP, WREG     ;restore working register, refer to note 1
    MOVFF   STATUS_TEMP, STATUS ;restore STATUS register
    RETFIE
```

Total = 12-13 TCY (if Timer1 overflow occurred)

Note: These instructions are required based on the function of the ISR. If the only code in the ISR is to reload Timer1, then they are not required, but may be required if additional code is added.

Date Codes that pertain to this issue: All engineering and production devices.

28. Module: EUSART

In rare situations, one or more extra zero bytes have been observed in a packet transmitted by the module operating in Asynchronous mode. The actual data is not lost or corrupted; only unwanted (extra) zero bytes are observed in the packet.

This situation has only been observed when the contents of the transmit buffer, TXREG, are transferred to the TSR during the transmission of a Stop bit. For this to occur, three things must happen in the same instruction cycle:

- TXREG is written to;
- the baud rate counter overflows (at the end of the bit period); and
- a Stop bit is being transmitted (shifted out of TSR).

Work around

If possible, do not use the module's double buffer capability. Instead, load the TXREG register when the TRMT bit (TXSTA<1>) is set, indicating the TSR is empty.

If double-buffering is used and back-to-back transmission is performed, then load TXREG immediately after TXIF is set or wait 1-bit time after TXIF is set. Both solutions prevent writing TXREG while a Stop bit is transmitted. Note that TXIF is set at the beginning of the Stop bit transmission.

If transmission is intermittent, then do the following:

- Wait for the TRMT bit to be set before loading TXREG
- Alternatively, use a free timer resource to time the baud period. Set up the timer to overflow at the end of Stop bit, then start the timer when you load the TXREG. Do not load the TXREG when timer is about to overflow.

Date Codes that pertain to this issue:

All engineering and production devices.

29. Module: EUSART/AUSART

In 9-Bit Asynchronous Full-Duplex Receive mode, the received data may be corrupted if the TX9D bit (TXSTA<0>) is not modified immediately after the RCIDL bit (BAUDCON<6>) is set.

Work around

Write to TX9D only when a reception is not in progress (RCIDL = 1). Since there is no interrupt associated with RCIDL, it must be polled in software to determine when TX9D can be updated.

Date Codes that pertain to this issue:

All engineering and production devices.

30. Module: EUSART

After the last received byte has been read from the EUSART receive buffer, RCREG, the value is no longer valid for subsequent read operations.

Work around

The RCREG register should only be read once for each byte received. After each byte is received from the EUSART, store the byte into a user variable. To determine when a byte is available to read from RCREG, poll the RCIDL bit (BAUDCON<6>) for a low-to-high transition, or use the EUSART receive interrupt, RCIF (PIR1<5>).

Date Codes that pertain to this issue:

All engineering and production devices.

31. Module: EUSART

With the auto-wake-up option enabled by setting the WUE (BAUDCON<1>) bit, the RCIF (PIR1<5>) bit will become set on a high-to-low transition on the RX pin. While the WUE bit is set, reading the receive buffer, RCREG, will not clear the RCIF interrupt flag. Therefore, the first opportunity to automatically clear RCIF by reading RCREG will happen only after WUE bit is cleared.

Note:	RCIF can only be cleared by reading RCREG.

Work around

1. Poll the WUE bit and read RCREG after the WUE bit is automatically cleared.

Date Codes that pertain to this issue:

All engineering and production devices.

32. Module: Timer1

In 16-Bit Asynchronous Counter mode (with or without use of the Timer1 oscillator), the TMR1H and TMR3H buffers do not update when TMRxL is read.

This issue only affects reading the TMRxH registers. The timers increment and set the interrupt flags as expected. The timer registers can also be written as expected.

Work around

1. Use 8-bit mode by clearing the RD16 bit (T1CON<7>).
2. Use the internal clock synchronization option by clearing the $\overline{\text{T1SYNC}}$ bit (T1CON<2>).

Date Codes that pertain to this issue:

All engineering and production devices.

33. Module: MSSP

The MSSP configured in SPI slave mode will generate a write collision if SSPBUF is updated and the previous SSPBUF contents have not been transferred to the shift register.

Reinitializing the MSSP by clearing and setting the SSPEN (SSPCON1<5>) bit prior to rewriting SSPBUF will not prevent the error condition.

Work around

Prior to updating the SSPBUF register with a new value, verify whether the previous contents were transferred by reading the BF (SSPSTAT<0>) bit. If the previous byte has not been transferred, update SSPBUF and clear the WCOL (SSPCON1<7>) bit if necessary.

Date Codes that pertain to this issue:

All engineering and production devices.

34. Module: MSSP

In SPI mode, the SDO output may change after the inactive clock edge of the bit '0' output. This may affect some SPI components that read data over 300 ns after the inactive edge of SCK.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

35. Module: MSSP

It has been observed that, following a Power-on Reset, I^2C mode may not initialize properly by just configuring the SCL and SDA pins as either inputs or outputs. This has only been seen in a few unique system environments.

A test of a statistically significant sample of pre-production systems, across the voltage and current range of the application's power supply, should indicate if a system is susceptible to this issue.

Work around

Before configuring the module for I^2C operation:

1. Configure the SCL and SDA pins as outputs by clearing their corresponding TRIS bits.
2. Force SCL and SDA low by clearing the corresponding LAT bits.
3. While keeping the LAT bits clear, configure SCL and SDA as inputs by setting their TRIS bits.

Once this is done, use the SSPCON1 and SSPCON2 registers to configure the proper I^2C mode as before.

Date Codes that pertain to this issue:

All engineering and production devices.

36. Module: Reset

This version of silicon does not support the functionality described in Note 1 of parameter D002 in **Section 26.1 "DC Characteristics: Supply Voltage"** of the data sheet. The RAM content may be altered during a Reset event if following conditions are met.

- Device is accessing RAM.
- Asynchronous Reset (i.e., WDT, BOR or $\overline{\text{MCLR}}$ occurs when a write operation is being executed (start of a Q4 cycle).

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

37. Module: External Memory Bus

For PIC18F8XXX devices, the Stack Pointer may incorrectly increment during a table read operation if the external memory bus wait states are enabled (i.e., Configuration bit, WAIT, is clear (CONFIG3L<7> = 0) and WAIT bits (MEMCON<5:4>) are not equal to '11').

Work around

If using the external memory bus and performing TBLRD operations with a non-zero wait state (CONFIG3L<7> = 0 and WAIT<1:0> (MEMCON<5:4>) are not equal to '11'), disable interrupts by clearing the GIE/GIEH (INTCON<7>) and PEIE/GIEL (INTCON<6>) bits prior to executing any TBLRD operation.

Date Codes that pertain to this issue:

All engineering and production devices.

38. Module: External Memory Bus

The A19:A16 address lines may release to their inactive states at the same time as Read/Write bus control pins ($\overline{OE}$, $\overline{WRH}$ and $\overline{WRL}$). This violates bus timing condition described in Figure 26.5 and Figure 26.6 of the data sheet. The result may be a device on the memory bus detecting an address change when a Read or Write is initiated.

This situation may be more likely to affect faster peripheral memory devices (e.g., Flash RAMs). Longer propagation delays on the control signal lines, which can be influenced by stray capacitance and other factors, are more likely to adversely affect the situation.

Work around

Two workarounds are presented here. Others may be available.

1. Use a hardware latch, triggered by falling edges on the ALE signal, on the A19:A16 address lines. This will hold the address until $\overline{WRL}$ or $\overline{WRH}$ can transition to an inactive state.
2. Add a delay circuit on the A19:A16 address lines to extend the valid time for the signals.

Date Codes that pertain to this issue:

All engineering and production devices.

39. Module: Power-up Timer

If Brown-out Reset (BOR) is disabled, then the Power-up Timer (PWRT) gets disabled irrespective of the state of the $\overline{PWRTEN}$ Configuration bit (CONFIG2L<0>).

Work around

Do either of the following:

1. Enable the BOR using any desired mode and set point.
2. If BOR operation is not desired:
   a) Configure the BOR using BOREN<1:0> = 01 (CONFIG2L<2:1>). BOR is controlled by SBOREN.
   b) Configure the BOR for the lowest voltage set point by clearing the BORV<1:0> bits (CONFIG2L<4:3>). In this configuration, the SBOREN bit resets to '1', enabling the BOR.
   c) When code execution begins following all Resets, disable the BOR by clearing the SBOREN bit (RCON<6>).

Date Codes that pertain to this issue:

All engineering and production devices.

40. Module: Analog-to-Digital (A/D) Converter Module

When the A/D clock source is selected as 2 TOSC or RC (when ADCS2:ADCS0 = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

Work around

Select a different A/D clock source (4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC or 64 TOSC) and avoid selecting the 2 TOSC or RC modes.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (8/2004)
First revision of this document which includes silicon issues 1-4 (MSSP), 5 (PWM), 6 (CCP), 7 (A/D), 8 (AUSART), 9 (External Memory Bus), 10 (Timer1/Timer3) and 11 (Timer1).

Rev B Document (02/2005)
Updated issues 1, 3, 4, 5 (MSSP), 12 (AUSART) and 14 (Timer1/Timer3) and added issues 6 (CCP), 9 (BOD), 10-11 (EUSART), 15 (Timer1/Timer3) and 16 (Interrupts).

Rev C Document (12/2005)
Updated issues 4 (MSSP) and 16 (Interrupts). Added issues 18-20 (EUSART), 21-25 (MSSP), 26 (MSSP – SPI Mode) and 27 (Timer1 – Asynchronous Counter).

Rev D Document (5/2006)
Updated issue 16 (Interrupts) with optimized C code example. Added issues 28-31 (EUSART), 32 (Timer1), 33-35 (MSSP), 36 (Reset), 37 (External Memory Bus) and 38 (External Memory Bus).

Rev E Document (2/2007)
Added issue 39 (Power-up Timer). Added date code applicability note to issues 18-20 (EUSART), 21-25 (MSSP), 26 (MSSP – SPI Mode), 27 (Timer1 – Asynchronous Counter) and 37-38 (External Memory Bus).

Rev F Document (7/2007)
Added issue 40 (A/D Converter Module).

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