dsPIC30F2010

dsPIC30F2010 Rev. A1 Silicon Errata

The dsPIC30F2010 (Rev. A1) samples that you have received conform to the specifications and functionality described in the following documents:

- DS70157 – "*dsPIC30F/33F Programmer's Reference Manual*"
- DS70118 – "*dsPIC30F2010 Data Sheet*"
- DS70046 – "*dsPIC30F Family Reference Manual*"

The exceptions to the specifications in the documents listed above are described in this Errata.

dsPIC30F2010 Rev A1 silicon is identified by performing a "Reset and Connect" operation to the device using MPLAB® ICD 2 within the MPLAB IDE. The following text is visible under the MPLAB ICD 2 section in the Output window within MPLAB IDE:

```
MPLAB ICD 2 Ready
Connecting to MPLAB ICD 2
...Connected
Setting Vdd source to target
Target Device dsPIC30F2010 found,
revision = 0x1
...Reading ICD Product ID
Running ICD Self Test
...Passed
MPLAB ICD 2 Ready
```

The errata described in this section will be addressed in future revisions of dsPIC30F2010 silicon.

Silicon Errata Summary

The following list summarizes the errata described in this document:

1. Y Data Space Dependency

   When an instruction that writes to a location in the address range of Y data memory is immediately followed by a MAC type DSP instruction that reads a location also resident in Y data memory, the operations will not be performed as specified.

2. MAC Class Instructions with ±4 Address Modification

   Sequential MAC instructions, which prefetch data from Y data space using ±4 address modification will cause an address error trap.

3. Decimal Adjust Instruction

   The Decimal Adjust instruction, DAW.b, may improperly clear the Carry bit, C (SR<0>).

4. PSV Operations Using SR

   In certain instructions, fetching one of the operands from program memory using Program Space Visibility (PSV) will corrupt specific bits in the STATUS Register, SR.

5. Early Termination of Nested DO Loops

   When using two DO loops in a nested fashion, terminating the inner-level DO loop by setting the EDT (CORCON<11>) bit will produce unexpected results.

6. Interrupting a REPEAT Loop

   When a REPEAT loop is interrupted by two or more interrupts in a nested fashion, an address error trap may be caused.

7. DISI Instruction

   The DISI instruction will not disable interrupts if a DISI instruction is executed in the same instruction cycle that the DISI counter decrements to zero.

8. 32-bit General Purpose Timers

   The 32-bit general purpose timers do not function as specified for prescaler ratios other than 1:1.

9. Output Compare Module in PWM Mode

   Output compare will produce a glitch when loading a 0% duty cycle in PWM mode. It will also miss the next compare after the glitch.

10. Output Compare

    The output compare module will produce a glitch on the output when an I/O pin is initially set high and the module is configured to drive the pin low at a specified time.

11. 10-bit Analog-to-Digital Converter (ADC) – Sequential Sampling

    Sampling multiple channels sequentially using any conversion trigger other than the auto-convert feature requires SAMC bits to be non-zero.

12. INT0, ADC and Sleep Mode

    ADC event triggers from the INT0 pin will not wake-up the device from Sleep mode if the SMPIx bits are non-zero.

13. Watchdog Timer

    The Watchdog Timer does not function as specified.

14. 4x PLL Operation

    The 4x PLL mode of operation may not function correctly for certain input frequencies.

15. Interrupt Controller – Sequential Interrupts

    Sequential interrupts after modifying the CPU IPL, interrupt IPL, interrupt enable or interrupt flag may cause an address error trap.

16. 8x PLL Mode

    If 8x PLL mode is used, the input frequency range is 5-10 MHz instead of 4-10 MHz.

17. SPI Module

    When enabled, the SPI module does not disable RF2 as general I/O.

18. Quadrature Encoder Interface (QEI) Module

    The QEI module does not generate an interrupt in a particular overflow condition.

19. Sleep Mode

    Execution of the Sleep instruction (`PWRSAV #0`) may cause incorrect program operation after the device wakes up from Sleep. The current consumption during Sleep may also increase beyond the specifications listed in the device data sheet.

20. I^2C™ Module

    The I^2C module loses incoming data bytes when operating as an I^2C slave.

21. Motor Control PWM – PWM Counter Register

    PTMR does not continue counting down after halting code execution in Debug mode.

22. I/O Port – Port Pin Multiplexed with IC1

    The Port I/O pin multiplexed with the Input Capture 1 (IC1) function cannot be used as a digital input pin when the UART auto-baud feature is enabled.

23. FRC

    Internal FRC accuracy does not perform to specification.

24. I^2C Module: 10-bit Addressing Mode

    When the I^2C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I^2C devices, the A10 and A9 bits may not work as expected.

25. Timer Module

    Clock switching prevents the device from waking up from Sleep.

26. PLL Lock Status Bit

    The PLL LOCK Status bit (OSCCON<5>) can occasionally get cleared and generate an oscillator failure trap even when the PLL is still locked and functioning correctly.

27. PSV Operations

    An address error trap occurs in certain addressing modes when accessing the first four bytes of any PSV page.

28. I^2C Module: 10-bit Addressing Mode

    The 10-bit slave does not set the RBF flag or load the I2CxRCV register on address match if the Least Significant bits of the address are the same as the 7-bit reserved addresses.

29. I^2C Module: 10-bit Addressing Mode

    When the I^2C module is configured as a 10-bit slave with an address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02.

30. I^2C Module

    When the I^2C module is enabled, the dsPIC® DSC device generates a glitch on the SDA and SCL pins, causing a false communication start in a single-master configuration or a bus collision in a multi-master configuration.

The following sections describe the errata and work around to these errata, where they may apply.

1. Module: Y Data Space Dependency

When an instruction that writes to a location in the address range of Y data memory (addresses between 0x0900 and 0x09FF) is immediately followed by a MAC type DSP instruction that reads a location also resident in Y data memory, the two operations will not be executed as specified. This is demonstrated in Example 1.

EXAMPLE 1: INCORRECT RESULTS

```
MOV     #0x090A, W0     ;Load address > =
                        ;0x900 into W0
MOV     #0x09B0, W10    ;Load address >=
                        ;0x900 into W10
MOV     W2, [W0++]      ;Perform indirect
                        ;write via W0 to
                        ;address >= 0x900
MAC     W4*W5, A, [W10]+=2, W5 ;Perform
                        ;read operation
                        ;using Y-AGU
```

Work arounds

Work around 1:

Insert a NOP between the two instructions as shown in Example 2.

EXAMPLE 2: CORRECT RESULTS

```
MOV     #0x090A, W0     ;Load address > =
                        ;0x900 into W0
MOV     #0x09B0, W10    ;Load address >=
                        ;0x900 into W10
MOV     W2, [W0++]      ;Perform indirect
                        ;write via W0 to
                        ;address >= 0x900
NOP                     ;No operation
MAC     W4*W5, A, [W10]+=2, W5 ;Perform
                        ;read operation
                        ;using Y-AGU
```

Work around 2:

If work around #1 is not feasible due to real-time application constraints, the user may take precautions to ensure that a write operation performed on a location in Y data memory is not immediately followed by a DSP MAC type instruction that performs a read operation of a location in Y data memory.

2. Module: MAC Class Instructions with ±4 Address Modification

Sequential MAC class instructions, which prefetch data from Y data space using ±4 address modification, will cause an address error trap. The trap occurs only when all of the following conditions are true:

1. Two sequential MAC class instructions (or a MAC class instruction executed in a REPEAT or DO loop) that prefetch from Y data space.
2. Both instructions prefetch data from Y data space using the + = 4 or - = 4 address modification.
3. Neither of the instruction uses an accumulator write back.

Work around

This problem can be avoided using any of the following methods:

1. Inserting any other instruction between the two MAC class instructions.
2. Adding an accumulator write back (a dummy write back if needed) to either of the MAC class instructions.
3. Do not use the + = 4 or - = 4 address modification.
4. Do not prefetch data from Y data space.

3. Module: CPU – DAW.b Instruction

The Decimal Adjust instruction, DAW.b, may improperly clear the Carry bit, C (SR<0>), when executed.

Work around

Check the state of the Carry bit prior to executing the DAW.b instruction. If the Carry bit is already set, set the Carry bit again after executing the DAW.b instruction. Example 3 shows how the application should process the Carry bit during a BCD addition operation.

EXAMPLE 3: CHECK CARRY BIT BEFORE DAW.b

```
    .include “p30f6010.inc”
    .......
    mov.b   #0x80, w0   ;First BCD number
    mov.b   #0x80, w1   ;Second BCD number
    add.b   w0, w1, w2  ;Perform addition
    bra     NC, L0      ;If C set go to L0
    daw.b   w2          ;If not,do DAW and
    bset.b  SR, #C      ;set the carry bit
    bra     L1          ;and exit
L0:daw.b    w2
L1: ....
```

4. Module: PSV Operations Using SR

When one of the operands of instructions shown in Table 1 is fetched from program memory using Program Space Visibility (PSV), the STATUS register, SR and/or the results may be corrupted.

These instructions are identified in Table 1. Example 4 demonstrates a scenario where this occurs.

Also, always use Work around 2 if the C compiler is used to generate code for dsPIC30F2010 devices.

TABLE 1: AFFECTED INSTRUCTIONS

Instruction(1)	Examples of Incorrect Operation(2)	Data Corruption IN
ADDC	ADDC W0, [W1++], W2 ;	SR<1:0> bits(3), Result in W2
SUBB	SUBB.b W0, [++W1], W3 ;	SR<1:0> bits(3), Result in W3
SUBBR	SUBBR.b W0, [++W1], W3 ;	SR<1:0> bits(3), Result in W3
CPB	CPB W0, [W1++], W4 ;	SR<1:0> bits(3)
RLC	RLC [W1], W4 ;	SR<1:0> bits(3), Result in W4
RRC	RRC [W1], W2 ;	SR<1:0> bits(3), Result in W2
ADD(Accumulator-based)	ADD [W1++], A ;	SR<1:0> bits(3)
LAC	LAC [W1], A ;	SR<15:10> bits(4)

Note 1: Refer to the "*dsPIC30F/33F Programmer's Reference Manual*" (DS70157) for details on the dsPIC30F Instruction set.

2: The errata only affects these instructions when a PSV access is performed to fetch one of the source operands in the instruction. A PSV access is performed when the Effective Address of the source operand is greater than 0x8000 and the PSV (CORCON<2>) bit is set to '1'. In the examples shown, the data access from program memory is made via the W1 register.

3: SR<1:0> bits represent Sticky Zero and Carry Status bits respectively.

4: SR<15:10> bits represent Accumulator Overflow and Saturation Status bits.

EXAMPLE 4: INCORRECT RESULTS

```
.include "p30fxxxx.inc"
.......
MOV.B   #0x00, W0  ;Load PSVPAG register
MOV.B   WREG, PSVPAG
BSET    CORCON, #PSV;Enable PSV
....
MOV     #0x8200, W1;Set up W1 for
                   ;indirect PSV access
                   ;from 0x000200
ADD     W3, [W1++], W5 ;This instruction
                       ;works ok
ADDC    W4, [W1++], W6 ;Carry flag and
                       ;W6 gets
                       ;corrupted here!
```

EXAMPLE 5: CORRECT RESULTS

```
.include "p30fxxxx.inc"
.......
MOV.B   #0x00, w0  ;Load PSVPAG register
MOV.B   WREG, PSVPAG
BSET    CORCON, #PSV;Enable PSV
....
MOV     #0x8200, W1;Set up W1 for
                   ;indirect PSV access
                   ;from 0x000200
ADD     W3, [W1++], W5 ;This instruction
                       ;works ok
MOV     [W1++], W2 ;Load W2 with data
                   ;from program memory
ADDC    W4, W2, W6 ;Carry flag and W4
                   ;results are ok!
```

Work arounds

Work around 1: For Assembly Language Source Code

To work around the erratum in the MPLAB ASM30 assembler, the application may perform a PSV access to move the source operand from program memory to RAM or a W register prior to performing the operations listed in Table 1. The work around for Example 4 is demonstrated in Example 5.

Work around 2: For C Language Source Code

For applications using C language, MPLAB C30 versions 1.20.04 or higher provide the following command-line switch that implements a work around for the erratum.

```
-merrata=psv
```

Refer to the "`readme.txt`" file in the MPLAB C30 v1.20.04 tool suite for further details.

5. Module: Early Termination of Nested DO Loops

When using two DO loops in a nested fashion, terminating the inner-level DO loop by setting the EDT (CORCON<11>) bit will produce unexpected results. Specifically, the device may continue executing code within the outer DO loop forever. This erratum does not affect the operation of the MPLAB C30 compiler.

Work around

The application should save the DCOUNT SFR prior to entering the inner DO loop and restore it upon exiting the inner DO loop. This work around is shown in Example 6.

EXAMPLE 6: SAVE AND RESTORE DCOUNT

```
        .include “p30fxxxx.inc”
        .......
        DO #CNT1, LOOP0    ;Outer loop start
        ....
        PUSH    DCOUNT     ;Save DCOUNT
        DO      #CNT2, LOOP1   ;Inner loop
        ....               ;starts
        BTSS    Flag, #0
        BSET    CORCON, #EDT;Terminate inner
        ....               ;DO-loop early
        ....
LOOP1:  MOV     W1, W5     ;Inner loop ends
        POP     DCOUNT     ;Restore DCOUNT
        ...
LOOP0:   MOV    W5, W8     ;Outer loop ends

Note:   For details on the functionality of
        EDT bit, see section 2.9.2.4
        in the dsPIC30F Family Reference
        Manual.
```

6. Module: Interrupting a REPEAT Loop

When interrupt nesting is enabled (or NSTDIS (INTCON1<15>) bit is ‘0’), the following sequence of events will lead to an address error trap:

1. REPEAT loop is active.
2. An interrupt is generated during the execution of the REPEAT loop.
3. The CPU executes the Interrupt Service Routine (ISR) of the source causing the interrupt.
4. Within the ISR, when the CPU is executing the first instruction cycle of the 3-cycle RETFIE (Return from Interrupt) instruction, a second interrupt is generated by a source with a higher interrupt priority.

Work around

Processing of Interrupt Service Routines should be disabled while the RETFIE instruction is being executed. This may be accomplished in two different ways:

1. Place a DISI instruction immediately before the RETFIE instruction in all Interrupt Service Routines of interrupt sources that may be interrupted by other higher priority interrupt sources (with priority levels 1 through 6). This is shown in Example 7 in the Timer1 ISR. In this example, a DISI instruction inhibits level 1 through level 6 interrupts for 2 instruction cycles, while the RETFIE instruction is executed.

EXAMPLE 7: DISI BEFORE RETFIE

```
__T1Interrupt:     ;Timer1 ISR
    PUSH    W0     ;This line optional
    .......
    BCLR    IFS0, #T1IF
    POP     W0     ;This line optional
    DISI    #1
    RETFIE     ;Another interrupt occurs
               ;here and it is processed
               ;correctly
```

2. Immediately prior to executing the RETFIE instruction, increase the CPU priority level by modifying the IPL<2:0> (SR<7:5>) bits to ‘111’ as shown in Example 8. This will disable all interrupts between priority levels 1 through 7.

EXAMPLE 8: RAISE IPL BEFORE RETFIE

```
__T1Interrupt:     ;Timer1 ISR
    PUSH    W0
    .......
    BCLR    IFS0, #T1IF
    MOV.B   #0xE0, W0
    MOV.B   WREG, SR
    POP     W0
    RETFIE     ;Another interrupt occurs
               ;here and it is processed
               ;correctly
```

7. Module: DISI Instruction

When a user executes a DISI #7, for example, this will disable interrupts for 7 + 1 cycles (7 + the DISI instruction itself). In this case, the DISI instruction uses a counter which counts down from 7 to 0. The counter is loaded with 7 at the end of the DISI instruction.

If the user code executes another DISI on the instruction cycle where the DISI counter has become zero, the new DISI count is loaded, but the DISI state machine does not properly re-engage and continue to disable interrupts. At this point, all interrupts are enabled. When the user code executes a DISI instruction next time, the feature will act normally and block interrupts.

To summarize, it is only when a DISI execution is coincident with the current DISI count = 0, that the issue occurs. Executing a DISI instruction before the DISI counter reaches zero will not produce this error. In this case, the DISI counter is loaded with the new value, and interrupts remain disabled until the counter becomes zero.

Work around

When executing multiple DISI instructions within the source code, make sure that subsequent DISI instructions have at least one instruction cycle between the time that the DISI counter decrements to zero and the next DISI instruction. Alternatively, ensure that the subsequent DISI instructions are called before the DISI counter decrements to zero.

8. Module: 32-bit General Purpose Timers

Pairs of 16-bit timers may be combined to form 32-bit timers. For example, Timer2 and Timer3 are combined into a single 32-bit timer. For this release of silicon, when a 32-bit timer is prescaled by ratios other than 1:1, unexpected results may occur.

Work around

None. The application may only use the 1:1 prescaler for 32-bit timers.

9. Module: Output Compare in PWM Mode

If the desired duty cycle is '0' (OCxRS = 0), the module will generate a high level glitch of 1 TCY. The second problem is that on the next cycle after the glitch, the OC pin does not go high, or in other words, it misses the next compare for any value written on OCxRS.

Work around

There are two possible solutions to this problem:

1. Load a value greater than '0' to the OCxRS register when operating in PWM mode. In this case, no 0% duty cycle is achievable.
2. If the application requires 0% duty cycles, the output compare module can be disabled for 0% duty cycles, and re-enabled for non-zero percent duty cycles.

10. Module: Output Compare

A glitch will be produced on an output compare pin under the following conditions:

- The user software initially drives the I/O pin high using the output compare module or a write to the associated PORT register.
- The output compare module is configured and enabled to drive the pin low at some point in later time (OCxCON = Ox0002 or OCxCON = 0x0003).

When these events occur, the output compare module will drive the pin low for one instruction cycle (TCY) after the module is enabled.

Work around

None. However, the user may use a timer interrupt and write to the associated PORT register to control the pin manually.

11. Module: 10-bit Analog-to-Digital Converter (ADC)

Sampling multiple channels sequentially using any conversion trigger source other than the auto-convert feature requires SAMC bits to be non-zero. Thus, if the following conditions are all satisfied, the module may not operate as specified:

- Multiple S/H channels are sampled sequentially

  CHPS(ADCON2<9:8>) is not equal to '00' and SIMSAM(ADCON1<3>) = 0

- Auto-convert option is not chosen as the conversion trigger

  SSRC(ADCON1<7:5>) is not equal to '111'

- SAMC(ADCON3<12:8>) is equal to '00000'

Work around

Set the value of the SAMC bits to anything other than '00000'. The module will now operate as specified.

12. Module: INT0, ADC and Sleep Mode

ADC event triggers from the INT0 pin will not wake-up the device from Sleep mode if the SMPIx bits are non-zero. This implies that if the ADC is configured to generate an interrupt after a certain number of INT0 triggered conversions, the ADC conversions will not be triggered and the device will remain in Sleep. The ADC will perform conversions and wake-up the device only if it is configured to generate an interrupt after each INT0 triggered conversion (SMPI<3:0> = 0000).

Work around

None. If ADC event trigger from the INT0 pin is required, initialize SMPI<3:0> to '0000' (interrupt on every conversion).

13. Module: Watchdog Timer

The Watchdog Timer does not function as specified. If the CLRWDT instruction is not executed before the Watchdog Timer is half-expired or greater, the device will reset.

Work around

The user must always issue the CLRWDT instruction before the Watchdog timer is half-expired. For instance, if the Watchdog time-out period is configured for 2 msec, the CLRWDT instruction must be executed faster than every 1 msec.

14. Module: 4x PLL Operation

When the 4x PLL mode of operation is selected, the specified input frequency range of 4-10 MHz is not fully supported.

When device V_{DD} is 2.5-3.0V, the 4x PLL input frequency must be in the range of 4-5 MHz. When device V_{DD} is 3.0-3.6V, the 4x PLL input frequency must be in the range of 4-6 MHz for both industrial and extended temperature ranges.

Work around

1. Use 8x PLL or 16x PLL mode of operation and set final device clock speed using the POST<1:0> oscillator postscaler control bits (OSCCON<7:6>).
2. Use the EC without PLL Clock mode with a suitable clock frequency to obtain the equivalent 4x PLL clock rate.

15. Module: Interrupt Controller – Sequential Interrupts

When an interrupt nesting is enabled (or NSTDIS (INTCON1<15>) bit is '0'), the following sequence of events will lead to an address error trap. The generic terms "Interrupt 1" and "Interrupt 2" are used to represent any two enabled dsPIC30F interrupts.

1. Interrupt 1 processing begins.
2. Interrupt 1 is negated by user software by one of the following methods:
   - CPU IPL is raised to Interrupt 1 IPL level or higher or
   - Interrupt 1 IPL is lowered to CPU IPL level or lower or
   - Interrupt 1 is disabled (Interrupt 1 IE bit set to '0') or
   - Interrupt 1 flag is cleared
3. Interrupt 2 occurs with a priority higher than Interrupt 1.

Work around

The user may disable interrupt nesting or execute a DISI instruction before modifying the CPU IPL or Interrupt 1 setting. A minimum DISI value of 2 is required if the DISI is executed immediately before the CPU IPL or Interrupt 1 is modified, as shown in Example 9. If the MPLAB C30 compiler is being used, one must inspect the Disassembly Listing in the MPLAB IDE file to determine the exact number of cycles to disable level 1-6 interrupts. One may use a large DISI value and then set the DISICNT register to zero, as shown in Example 10. A macro may also be used to perform this task, as shown in Example 11.

EXAMPLE 9: USING DISI

```
.include       "p30fxxxx.inc"
...
DISI#2  ; protect the disable of INT1
BCLRIEC1, #INT1IE; disable interrupt 1
...     ; next instruction protected by DISI
```

EXAMPLE 10: RAISING CPU INTERRUPT PRIORITY LEVEL

```
.include       "p30fxxxx.h"
...
__asm__ volatile ("DISI #0x1FFF");   // protect CPU IPL modification
SRbits.IPL = 0x5;                    // set CPU IPL to 5
DISICNT = 0x0;                       // remove DISI protection
```

EXAMPLE 11: USING MACRO

```
#define DISI_PROTECT(X) {\
    __asm__ volatile ("DISI #0x1FFF");\
    X;                \
    DISICNT = 0; }

DISI_PROTECT(SRbits.IPL = 0x5);   // safely modify the CPU IPL
```

16. Module: 8x PLL Mode

If 8x PLL mode is used, the input frequency range is 5-10 MHz instead of 4-10 MHz.

Work around

None. If 8x PLL is used, ensure that the input crystal or clock frequency is 5 MHz or greater.

17. Module: SPI

The SPI module does not have full control of the RF2 pin when the SPIEN bit is set. This means that RF2 can be used as general I/O when the SPI module is enabled.

Work around

It is recommended to avoid using the RF2 pin as I/O if the SPIEN bit is set.

18. Module: QEI Interrupt Generation

The Quadrature Encoder Interface (QEI) module does not generate an interrupt when MAXCNT is set to 0xFFFF and the following events occur:

1. POSCNT underflows from 0x0000 to 0xFFFF.
2. POSCNT stops.
3. POSCNT overflows from 0xFFFF to 0x0000.

This sequence of events occurs when the motor is running in one direction, which causes POSCNT to underflow to 0xFFFF. Once this happens, the motor stops and starts to run in the opposite direction, which generates an overflow from 0xFFFF to 0x0000. The QEI module does not generate an interrupt when this condition occurs.

Work around

To prevent this condition from occurring, set MAXCNT to 0x7FFF, which will cause an interrupt to be generated by the QEI module.

In addition, a global variable can be used to keep track of bit 15, so that when an overflow or underflow condition is present on POSCNT, the variable will toggle bit 15. Example 12 shows the code required for this global variable.

EXAMPLE 12:

```
unsigned int POSCNT_b15 = 0;
unsigned int Motor_Position = 0;

int main(void)
{
            // ... User's code

            MAXCNT = 0x7FFF;       // Instead of 0xFFFF

            Motor_Position = POSCNT_b15 + POSCNT;

            // ... User's code
}
void __attribute__((__interrupt__)) _QEIInterrupt(void)
{
            IFSxbits.QEIIF = 0;    // Clear QEI interrupt flag
                                   // x=2 for dsPIC30F
                                   // x=3 for dsPIC33F
            POSCNT_b15 ^= 0x8000;  // Overflow or Underflow
}
```

19. Module: Sleep Mode

Execution of the Sleep instruction (PWRSAV #0) may cause incorrect program operation after the device wakes up from Sleep. The current consumption during Sleep may also increase beyond the specifications listed in the device data sheet.

Work arounds

To avoid this issue, any of the following three work arounds can be implemented, depending on the application requirements.

Work around 1:

Ensure that the PWRSAV #0 instruction is located at the end of the last row of Program Flash Memory available on the target device and fill the remainder of the row with NOP instructions.

This can be accomplished by replacing all occurrences of the PWRSAV #0 instruction with a function call to a suitably aligned subroutine. The address( ) attribute provided by the MPLAB ASM30 assembler can be utilized to correctly align the instructions in the subroutine. For an application written in C, the function call would be GotoSleep( ), while for an assembly language application, the function call would be CALL _GotoSleep.

The address error trap service routine software can then replace the invalid return address saved on the stack with the address of the instruction immediately following the _GotoSleep or GotoSleep( ) function call. This ensures that the device continues executing the correct code sequence after waking up from Sleep mode.

Example 13 demonstrates the work around described above, as it would apply to a dsPIC30F2010 device.

EXAMPLE 13:

```
; ------------------------------------------------------------------------------------------------
.global __reset
.global _main
.global _GotoSleep
.global __AddressError
.global __INT1Interrupt
; ------------------------------------------------------------------------------------------------
    .section *, code
_main:
    BSET    INTCON2, #INT1EP  ; Set up INT pins to detect falling edge
    BCLR    IFS1, #INT1IF     ; Clear interrupt pin interrupt flag bits
    BSET    IEC1, #INT1IE     ; Enable ISR processing for INT pins
    CALL    _GotoSleep        ; Call function to enter SLEEP mode
_continue:
    BRA  _continue
; ------------------------------------------------------------------------------------------------
; Address Error Trap
__AddressError:
    BCLR    INTCON1, #ADDRERR
    ; Set program memory return address to _continue
    POP.D   W0
    MOV.B   #tblpage (_continue), W1
    MOV     #tbloffset (_continue), W0
    PUSH.D  W0
    RETFIE
; ------------------------------------------------------------------------------------------------
__INT1Interrupt:
    BCLR   IFS1, #INT1IF         ; Ensure flag is reset
    RETFIE                       ; Return from Interrupt Service Routine
; ------------------------------------------------------------------------------------------------
    .section *, code, address (0x1FC0)
_GotoSleep:
; fill remainder of the last row with NOP instructions
    .rept 31
        NOP
    .endr
; Place SLEEP instruction in the last word of program memory
    PWRSAV #0
```

Work around 2:

Instead of executing a `PWRSAV #0` instruction to put the device into Sleep mode, perform a clock switch to the 512 kHz Low-Power RC (LPRC) Oscillator with a 64:1 postscaler mode. This enables the device to operate at 0.002 MIPS, thereby significantly reducing the current consumption of the device. Similarly, instead of using an interrupt to wake-up the device from Sleep mode, perform another clock switch back to the original oscillator source to resume normal operation. Depending on the device, refer to **Section 7. "Oscillator"** (DS70054) or **Section 29. "Oscillator"** (DS70268) in the "*dsPIC30F Family Reference Manual*" (DS70046) for more details on performing a clock switch operation.

Note:	The above work around is recommended for users for whom application hardware changes are not possible.

Work around 3:

Instead of executing a `PWRSAV #0` instruction to put the device into Sleep mode, perform a clock switch to the 32 kHz Low-Power (LP) Oscillator with a 64:1 postscaler mode. This enables the device to operate at 0.000125 MIPS, thereby significantly reducing the current consumption of the device. Similarly, instead of using an interrupt to wake-up the device from Sleep mode, perform another clock switch back to the original oscillator source to resume normal operation. Depending on the device, refer to **Section 7. "Oscillator"** (DS70054) or **Section 29. "Oscillator"** (DS70268) in the "*dsPIC30F Family Reference Manual*" (DS70046) for more details on performing a clock switch operation.

Note:	The above work around is recommended for users for whom application hardware changes are possible, and also for users whose application hardware already includes a 32 kHz LP Oscillator crystal.

20. Module: I²C

When the I²C module is configured as a slave, either in single-master or multi-master mode, the I²C receiver buffer is filled whether a valid slave address is detected or not. Therefore, an I²C receiver overflow condition occurs and this condition is indicated by the I2COV flag in the I2CSTAT register.

This overflow condition inhibits the ability to set the I²C receive interrupt flag (SI2CF) when the last valid data byte is received. Therefore, the I²C slave Interrupt Service Routine (ISR) is not called and the I²C receiver buffer is not read prior receiving the next data byte.

Work arounds

To avoid this issue, either of the following two work arounds can be implemented, depending on the application requirements.

Work around 1:

For applications in which the I²C receiver interrupt is not required, the following procedure can be used to receive valid data bytes:

1. Wait until the RBF flag is set.
2. Poll the I²C receiver interrupt SI2CIF flag.
3. If SI2CF is not set in the corresponding Interrupt Flag Status (IFSx) register, a valid address or data byte has not been received for the current slave. Execute a dummy read of the I²C receiver buffer, I2CRCV; this will clear the RBF flag. Go back to step 1 until SI2CF is set and then continue to Step 4.
4. If the SI2CF is set in the corresponding Interrupt Flag Status (IFSx) register, valid data has been received. Check the D_A flag to verify that an address or a data byte has been received.
5. Read the I2CRCV buffer to recover valid data bytes. This will also clear the RBF flag.
6. Clear the I²C receiver interrupt flag SI2CF.
7. Go back to step 1 to continue receiving incoming data bytes.

Work around 2:

Use this work around for applications in which the I²C receiver interrupt is required. Assuming that the RBF and the I2COV flags in the I2CSTAT register are set due to previous data transfers in the I²C bus (i.e., between master and other slaves); the following procedure can be used to receive valid data bytes:

1. When a valid slave address byte is detected, SI2CF bit is set and the I²C slave interrupt service routine is called; however, the RBF and I2COV bits are already set due to data transfers between other I²C nodes.
2. Check the status of the D_A flag and the I2COV flag in the I2CSTAT register when executing the I²C slave service routine.
3. If the D_A flag is cleared and the I2COV flag is set, an invalid data byte was received but a valid address byte was received. The overflow condition occurred because the I²C receive buffer was overflowing with previous I²C data transfers between other I²C nodes. This condition only occurs after a valid slave address was detected.
4. Clear the I2COV flag and perform a dummy read of the I²C receiver buffer, I2CRCV, to clear the RBF bit and recover the valid address byte. This action will also avoid the loss of the next data byte due to an overflow condition.
5. Verify that the recovered address byte matches the current slave address byte. If they match, the next data to be received is a valid data byte.
6. If the D_A flag and the I2COV flag are both set, a valid data byte was received and a previous valid data byte was lost. It will be necessary to code for handling this overflow condition.

21. Module: Motor Control PWM – PWM Counter Register

If the PTDIR bit is set (when PTMR is counting down), and the CPU execution is halted (after a breakpoint is reached), PTMR will start counting up as if PTDIR was zero.

Work around

None.

22. Module: I/O Port – Port Pin Multiplexed with IC1

If the user application enables the auto-baud feature in the UART module, the I/O pin multiplexed with the IC1 (Input Capture) pin cannot be used as a digital input.

Work around

None.

23. Module: FRC

Internal FRC accuracy is outside the specification documented in **"Electrical Characteristics"**, Table 22-17 "AC Characteristics: Internal RC Accuracy" of the "*dsPIC30F2010 Data Sheet*" (DS70118).

The actual internal FRC accuracy is:

- ±4% for 25°C
- ±5% for -40°C and 85°C
- ±6% for 125°C

24. Module: I^2C

If there are two I^2C devices on the bus, one of them is acting as the Master receiver and the other as the Slave transmitter. If both devices are configured for 10-bit addressing mode, and have the same value in the A10 and A9 bits of their addresses, then when the Slave select address is sent from the Master, both the Master and Slave acknowledge it. When the Master sends out the read operation, both the Master and the Slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

Work around

In all I^2C devices, the addresses as well as bits A10 and A9 should be different.

25. Module: Timer

When the timer is being operated in Asynchronous mode using the secondary oscillator (32.768 kHz) and the device is put into Sleep mode, a clock switch to any other oscillator mode before putting the device to Sleep prevents the timer from waking the device from Sleep.

Work around

Do not clock switch to any other oscillator mode if the timer is being used in Asynchronous mode using the secondary oscillator (32.768 kHz).

26. Module: PLL Lock Status Bit

The PLL LOCK Status bit (OSCCON<5>) can occasionally get cleared and generate an oscillator failure trap even when the PLL is still locked and functioning correctly.

Work around

The user application must include an oscillator failure trap service routine. In the trap service routine, first inspect the status of the Clock Failure Status bit (OSCCON<3>). If this bit is clear, return from the trap service routine immediately and continue program execution.

27. Module: PSV Operations

An address error trap occurs in certain addressing modes when accessing the first four bytes of an PSV page. This only occurs when using the following addressing modes:

- MOV.D
- Register Indirect Addressing (word or byte mode) with pre/post-decrement

Work around

Do not perform PSV accesses to any of the first four bytes using the above addressing modes. For applications using the C language, MPLAB C30 version 3.11 or higher, provides the following command-line switch that implements a work around for the erratum.

```
-merrata=psv_trap
```

Refer to the `readme.txt` file in the MPLAB C30 v3.11 tool suite for further details.

28. Module: I²C

In 10-bit Addressing mode, some address matches do not set the RBF flag or load the receive register I2CxRCV if the lower address byte matches the reserved addresses. In particular, these include all addresses with the form XX0000XXXX and XX1111XXXX, with the following exceptions:

- 001111000X
- 011111001X
- 101111010X
- 111111011X

Work around

Ensure that the lower address byte in 10-bit Addressing mode does not match any 7-bit reserved addresses.

29. Module: I²C

When the I²C module is configured as a 10-bit slave with and address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02; however, the module acknowledges both address bytes.

Work around

None.

30. Module: I²C

When the I²C module is enabled by setting the I2CEN bit in the I2CCON register, the dsPIC DSC device generates a glitch on the SDA and SCL pins. This glitch falsely indicates “Communication Start” to all devices on the I²C bus, and can cause a bus collision in a multi-master configuration.

Additionally, when the I2CEN bit is set, the S and P bits of the I²C module are set to values ‘1’ and ‘0’, respectively, which indicate a “Communication Start” condition.

Work arounds

To avoid this issue, either of the following two work arounds can be implemented, depending on the application requirements.

Work around 1:

In a single-master environment, add a delay between enabling the I²C module and the first data transmission. The delay should be equal to or greater than the time it takes to transmit two data bits.

In the multi-master configuration, in addition to the delay, all other I²C masters should be synchronized and wait for the I²C module to be initialized before initiating any kind of communication.

Work around 2:

In dsPIC DSC devices in which the I²C module is multiplexed with other modules that have precedence in the use of the pin, it is possible to avoid this glitch by enabling the higher priority module before enabling the I²C module.

Use the following procedure to implement this work around:

1. Enable the higher priority peripheral module that is multiplexed on the same pins as the I²C module.
2. Set up and enable the I²C module.
3. Disable the higher priority peripheral module that was enabled in step 1.

Note:	Work around 2 works only for devices that share the SDA and SCL pins with another peripheral that has a higher precedence over the port latch, such as the UART. The priority is shown in the pin diagram located in the data sheet. For example, if the SDA and SCL pins are shared with the UART and SPI pins, and the UART has higher precedence on the port latch pin.

APPENDIX A: REVISION HISTORY

Revision A (4/2004)

Original version of the document.

Revision B (11/2004)

Added silicon issues 3 and 4.

Revision C (12/2004)

Removed “Reset during Run-Time Self Programming (RTSP) of Program Flash Memory” – issue does not occur on this revision of silicon. Added silicon issue 7.

Revision D (3/2005)

Added silicon issues 8 and 9.

Revision E (10/2006)

Added silicon issues 2, 3, 7, 9, 10, 12 and 16.

Revision F (8/2007)

Added silicon issues 17 (SPI), 18 (QEI Interrupt Generation), and 19 (Sleep Mode). Removed document status.

Revision G (12/2007)

Updated silicon issue 4 (PSV Operations Using SR), and added silicon issues 20 and 21 (I^2C), 22 (Motor Control PWM – PWM Counter Register), 23 (I/O Port – Port Pin Multiplexed with IC1), and 24 (FRC).

Revision H (5/2008)

Added silicon issues 25 and 26 (I^2C), and 27 (Timer).

Revision J (9/2008)

Replaced issues 20 and 25 (I^2C) with issue 30 (I^2C). Added silicon issues 26 (PLL Lock Status Bit), 27 (PSV Operations) and 28-30 (I^2C).

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