PIC24FJ64GB004 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ64GB004 family devices that you have received conform functionally to the current Device Data Sheet (DS39940**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ64GB004 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ64GB004 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A2
PIC24FJ32GB002	4203h	0002h
PIC24FJ32GB004	420Bh	
PIC24FJ64GB002	4207h	
PIC24FJ64GB004	420Fh	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJ64GA1/GB0 Families Flash Programming Specification"* (DS39934) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A2
Output Compare	Cascaded mode	1.	Cascaded mode does not work as expected.	X
Power-Saving Modes	Sleep mode	2.	Transitory increase in IPD under certain conditions.	X
USB	—	3.	Issue with Host mode, low-speed operation.	X
USB	—	4.	CRC errors while using external transceiver.	X
UART	Break Character Generation	5.	Will not generate back-to-back Break characters.	X
Oscillator	Secondary Oscillator Configuration	6.	High-current draw when external signal applied under certain conditions.	X
SPI	Master mode	7.	Spurious transmission and reception of null data on wake-up from Sleep (Master mode).	X
SPI	Master mode	8.	Inaccurate SPITBF flag with high clock divider.	X
Triple (Enhanced) Comparator	—	9.	No interrupt generation with internal band gap reference.	X
Core	Doze Mode	10.	Instruction execution glitches following Doze bit changes.	X
Oscillator	Two-Speed Start-up	11.	Feature is not functional.	X
A/D	—	12.	Disabled voltage references during Debug mode.	X
Interrupts	INTx	13.	External interrupts missed when writing to INTCON2.	X
Oscillator	—	14.	POSCEN bit does not work with Primary + PLL modes	X
A/D Converter	—	15.	Module continues to draw current when disabled.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: Output Compare (Cascaded Mode)

When using Cascaded (32-bit) mode, Trigger and Synchronous modes do not work as expected. The even numbered module does not become synchronized to the odd numbered module, resulting in errors in the Most Significant 16 bits of the output. In certain modes, the even numbered module does not generate any output. This behavior is independent of the OCTRIG trigger/sync selection for the even numbered module.

Work around

None.

Affected Silicon Revisions

A2							
X							

2. Module: Power-Saving Modes (Sleep Mode)

When entering Sleep mode, a transitory increase over the specified Power-Down Base Current (I_{PD}) may occur. This has only been observed in some parts and then only under *both* of the following circumstances:

- the operating temperature is below -20°C; and
- Sleep mode is entered within 20 seconds of a POR event.

Following the increase, I_{PD} returns to the normal specified level at 20 seconds after the POR event.

Deep Sleep mode is not affected.

Work around

None

Affected Silicon Revisions

A2							
X							

This issue only applies to devices with date codes prior to 1001NNN as identified by the package markings.

3. Module: USB

While operating in Host mode and attached to a low-speed device through a full-speed USB hub, the PRE signal may not be generated correctly. This will result in not being able to communicate correctly with the low-speed device.

Work around

Connect low-speed devices directly to the application and not through a USB hub.

Affected Silicon Revisions

A2							
X							

4. Module: USB

When the module is configured to use an external transceiver, the CRC5 value of some packets may be incorrect.

Work around

Use the module's internal transceiver.

Affected Silicon Revisions

A2							
X							

5. Module: UART

The UART module will not generate consecutive Break characters. Trying to perform a back-to-back Break character transmission will cause the UART module to transmit the dummy character used to generate the first Break character instead of transmitting the second Break character. Break characters are generated correctly if they are followed by non-Break character transmission.

Work around

None.

Affected Silicon Revisions

A2							
X							

6. Module: Oscillator (Secondary Oscillator Configuration)

Under certain circumstances, applying voltages to the comparator inputs, C2INC and C2IND (SOSCO/RA4 and SOSCI/RB4, respectively), may cause the microcontroller's current draw to increase. This happens only when all of the following conditions are met:

- RA4 and RB4 are configured to function as digital I/O, rather than as Secondary Oscillator pins (SOSCEL<1:0> = 00);
- the pins are configured as digital inputs (TRIS<4> and TRISB<4> = 1); and
- the voltage applied to the pins approaches 1/2 V_{DD}.

This occurs regardless of the signal source. A comparator input voltage or a digital clock input of sufficient amplitude will have the same result.

Work around

If it is necessary to use RA4 and RB4 as comparator inputs, C2INC and C2IND, program the SOSCEL Configuration bits (CW3<9:8>) for one of the oscillator modes (SOSCEL<1:0> = 11 or 01), rather than as digital I/O.

In addition, use the internal 31 kHz RC Oscillator (LPRC) as the clock source for any systems that might otherwise use the Secondary Oscillator or an external Timer1 source. In addition to Timer1, this includes the RTCC and the Deep Sleep WDT.

Affected Silicon Revisions

A2							
X							

7. Module: SPI (Master Mode)

When operating in Enhanced Buffer Master mode, the module may transmit two bytes or two words of data, with a value of 0h, immediately upon the microcontroller waking up from Sleep mode. At the same time, the module "receives" two words or two bytes of data, also with the value of 0h.

The transmission of null data occurs even if the Transmit Buffer registers are empty prior to the microcontroller entering Sleep mode. The received null data requires that the receive buffer be read twice to clear the "received" data.

This behavior has not been observed when the module is operating in any other mode.

Work around

When operating in Enhanced Buffer Master mode, disable the module (SPIEN = 0) before entering Sleep mode.

Affected Silicon Revisions

A2							
X							

8. Module: SPI (Master Mode)

When operating in Enhanced Buffer Master mode, the Transmit Buffer Full flag, SPITBF, may be cleared before all data in the FIFO buffer has actually been set. This may result in data being overwritten before it can be sent.

This has only been observed when the SPI clock prescalers are configured for a divider of greater than 1:4.

This behavior has not been observed when the module is operating in any other mode.

Work around

Several options are available:

- If possible, use a total clock prescale factor of 1:4 or less.
- Do not use SPITBF to indicate when new data can be written to the buffer. Instead, use the SPIRBF or SPIBEC flags to track the number of bytes actually transmitted.
- If the SPITBF flag must be used, always wait at least one-half SPI clock cycle before writing to the transmit buffer.

Affected Silicon Revisions

A2							
X							

9. Module: Triple (Enhanced) Comparator

When any of the internal band gap options (V_{BG}, $V_{BG}/2$ or $V_{BG}/6$) are selected by the voltage reference module as the comparator's CV_{REF-} input, the comparator may not generate an interrupt when a preprogrammed event is detected.

The CV_{REF+} input works as previously described.

Work around

If it is necessary to use the internal band gap as a reference, do the following:

1. Enable the comparator's output (CMCON<14> = 1) and map the output to a pin with CN functionality or map an INTx function to this same pin. This method only consumes one I/O pin and requires no external connections.
2. Monitor the pin for an interrupt event.

Affected Silicon Revisions

A2							
X							

10. Module: Core (Doze Mode)

Operations that immediately follow any manipulations of the DOZE<2:0> or DOZEN bits (CLKDIV<14:11>) may not execute properly. In particular, for instructions that operate on an SFR, data may not be read properly. Also, bits automatically cleared in hardware may not be cleared if the operation occurs during this interval.

Work around

Always insert a NOP instruction before and after either of the following:

- Enabling or disabling Doze mode by setting or clearing the DOZEN bit
- Before or after changing the DOZE<2:0> bits

Affected Silicon Revisions

A2							
X							

11. Module: Oscillator (Two-Speed Start-up)

Two-Speed Start-up is not functional. Leaving the IESO Configuration bit in its default state (Two-Speed Start-up enabled) may result in unpredictable operation.

Work around

None. Always program the IESO Configuration bit to disable the feature (CW2<15> = 0).

Affected Silicon Revisions

A2							
X							

12. Module: A/D Converter

When using PGEC3 and PGED3 to debug an application, all voltage references will be disabled. This includes V_{REF+}, V_{REF-}, AV_{DD} and AV_{SS}. Any A/D conversion will always equal 03FFh.

Work around

Use either PGEC1/PGED1 or PGEC2/PGED2 to debug any A/D functionality.

Affected Silicon Revisions

A2							
X							

13. Module: Interrupts (INTx)

Writing to the INTCON2 register may cause an external interrupt event (inputs on INT0 through INT2) to be missed. This only happens when the interrupt event and the write event occur during the same clock cycle.

Work around

If this cannot be avoided, write the data intended for INTCON2 to any other register in the interrupt block of the SFR (addresses 0080h to 00E0h); then write the data to INTCON2.

Be certain to write the data to a register not being actively used by the application, or to any of the interrupt flag registers, in order to avoid spurious interrupts. For example, if the interrupts controlled by IEC4 are not being used in the application, the code sequence would be:

```
IEC4 = 0x1E;
INTCON2 = 0x1E;
IEC4 = 0;
```

It is the user's responsibility to determine an appropriate register for the particular application.

Affected Silicon Revisions

A2							
X							

14. Module: Oscillator

The POSCEN bit (OSCCON<2>) has no effect when a Primary Oscillator with PLL mode is selected (COSC<2:0> = 011). If XTPLL, HSPLL or ECPLL Oscillator mode are selected, and the device enters Sleep mode, the Primary Oscillator will be disabled, regardless of the state of the POSCEN bit.

XT, HS and EC Oscillator modes (without the PLL) will continue to operate as expected.

Work around

None.

Affected Silicon Revisions

A2							
X							

15. Module: A/D Converter

Once the A/D module is enabled (AD1CON1<15> = 1), it may continue to draw extra current, even if the module is later disabled (AD1CON1<15> = 0).

Work around

In addition to disabling the module through the ADON bit, set the corresponding PMD bit (ADC1MD, PMD1<0>) to power it down completely.

Disabling the A/D module through the PMD register also disables the AD1PCFG registers, which in turn, affects the state of any port pins with analog inputs. Users should consider the effect on I/O ports and other digital peripherals on those ports when ADC1MD is used for power conservation.

Affected Silicon Revisions

A2							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the Device Data Sheet (DS39940**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Guidelines for Getting Started with 16-Bit Microcontrollers

Section 2.4 Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE) has been replaced with a new and more detailed section. The entire text follows:

2.4 Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE)

Note:	This section applies only to PIC24FJ devices with an on-chip voltage regulator.

The on-chip voltage regulator enable/disable pin (ENVREG or DISVREG, depending on the device family) must always be connected directly to either a supply voltage or to ground. The particular connection is determined by whether or not the regulator is to be used:

- For ENVREG, tie to VDD to enable the regulator, or to ground to disable the regulator
- For DISVREG, tie to ground to enable the regulator or to VDD to disable the regulator

Refer to **Section 26.2 "On-Chip Voltage Regulator"** for details on connecting and using the on-chip regulator.

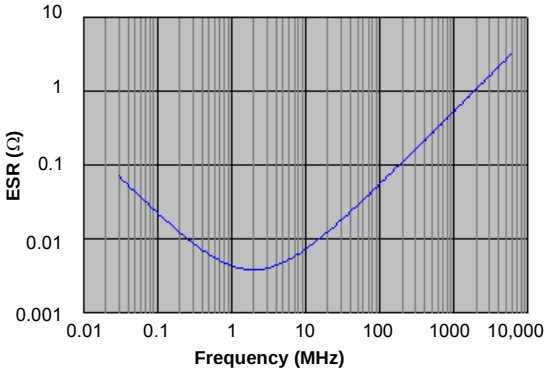
When the regulator is enabled, a low-ESR (< 5Ω) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

The placement of this capacitor should be close to VCAP/VDDCORE. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 29.0 "Electrical Characteristics"** for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 29.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at 25°C, 0V DC bias.

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TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to 125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to 85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to 125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to 85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to 125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to 85ºC

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

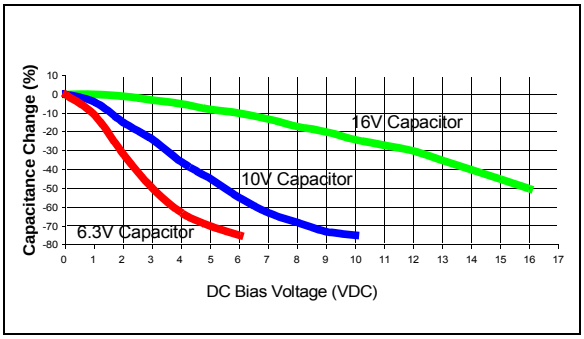
Typical low cost, 10 µF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 µF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal voltage regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for 16V, 10V and 6.3V rated capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V core voltage. Suggested capacitors are shown in Table 2-1.

2. Module: Electrical Characteristics

Changes, shown in bold, have been made to the DC10 and DC18 rows in Table 29-3. The updated table is shown below:

TABLE 29-3 DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions:		2.0V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
Operating Voltage							
DC10	Supply Voltage						
	VDD		**VBORMIN**	—	3.6	V	Regulator enabled
	VDD		VDDCORE	—	3.6	V	Regulator disabled
	VDDCORE		**2.0**	—	2.75	V	Regulator disabled
DC12	VDR	RAM Data Retention Voltage(2)	1.5	—	—	V	
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	VSS	—	—	V	
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	0-3.3V in 0.1s 0-2.5V in 60 ms
DC18	VBOR	Brown-out Reset Voltage	**1.96**	**2.03**	**2.15**	V	**16 MHz (8 MIPS) operation is supported until BOR is active**

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This is the limit to which VDD can be lowered without losing RAM data.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2009)

Initial release of this document; issued for revision A2. Includes silicon issues 1 (Output Compare – Cascaded Mode), 2 (Power-Saving Modes, Sleep Mode), 3-4 (USB) and 5 (UART).

Rev B Document (2/2010)

Adds new silicon issues 6 (Oscillator – Secondary Oscillator Configuration), 7 and 8 (SPI – Master Mode), 9 (Triple (Enhanced) Comparator), 10 (Core – Doze Mode) and 11 (Oscillator – Two-Speed Start-up) to silicon revision A2.

Rev C Document (2/2010)

Update to silicon issue 2 (Power-Saving Modes – Sleep Mode)

Rev D Document (8/2010)

Adds new silicon issues 12 (A/D Converter), 13 (Interrupts – INTx) 14 (Oscillator) and 15 (A/D Converter) to silicon revision A2.

Rev E Document (9/2010)

Revised silicon issue 15 (A/D Converter) to reflect updated definition of issues. Added data sheet clarification issues 1 (Guidelines For Getting Started with 16-Bit Microcontrollers) and 2 (Electrical Characteristics).

Rev F Document (11/2010)

Revised data sheet clarification issue 2 (Electrical Characteristics).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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