PIC18F87J11 Family
Silicon Errata and Data Sheet Clarification

The PIC18F87J11 family devices that you have received conform functionally to the current Device Data Sheet (DS39778**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F87J11 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A6**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F87J11 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)					
		A1	A2	A4	A5	A6	C1
PIC18F66J11	444h	1h	2h	4h	5h	6h	10h
PIC18F66J16	446h						
PIC18F67J11	448h						
PIC18F86J11	44Eh						
PIC18F86J16	450h						
PIC18F87J11	452h						

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC18F6XJXX/8XJXX Flash Microcontroller Programming Specification"* (DS39644) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Num	Issue Summary	Affected Revisions(1)					
				A1	A2	A4	A5	A6	C1
MSSPx	I^2C™ Slave Reception	1.	When configured for I^2C slave reception, the MSSPx module may not receive the correct data if the SSPxBUF register is not read within a window after an SSPxIF interrupt occurs.	X	X	X	X	X	X
Oscillator Configuration	PLL	2.	When Phase Lock Loop (PLL) is enabled, if the PLL input frequency is higher than 8 MHz, there may be problems accessing the RAM.	X	X				
Voltage Regulator	VDDCORE	3.	If VDDCORE drops below approximately 2.45V while the on-chip core voltage regulator is enabled and operating in Voltage Tracking mode, the REGSLP bit (WDTCON <7>) will be automatically cleared.	X					
SRAM	Read/Write	4.	Any read or write access to SRAM will increase the current consumption of the device – varying with how often the SRAM is accessed.	X					
Low-Voltage Detect	LVDSTAT	5.	The LVDSTAT VDDCORE status bit is not implemented in the cited revision of silicon.	X					
MSSPx	I^2C™ Master mode	6.	In Master mode, the first clock may become narrower than the configuration width if the slave performs a clock stretch and release.	X	X	X	X	X	X
EUSART	Synchronous Mode	7.	The TRMT bit may not indicate when the TSR register is empty.	X	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**).

1. Module: Master Synchronous Serial Port (MSSPx)

When configured for I²C™ slave reception, the MSSPx module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPxBUF) is not read within a window after the SSPxIF interrupt (PIRx<3>) has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I²C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPxCON2<0>).
- Each time the SSPxIF is set, read the SSPxBUF before the first rising clock edge of the next byte being received.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1		
X	X	X	X	X	X		

2. Module: Oscillator Configurations (PLL)

When Phase Lock Loop (PLL) is enabled, if the PLL input frequency is higher than 8 MHz, there may be problems accessing the RAM.

Work around

Limit the PLL input frequency from 4 MHz to 8 MHz. This will cause the system clock to operate from 16 MHz to 32 MHz.

If it is necessary to run the device above 32 MHz, do not enable PLL and use the EC mode.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1		
X	X						

3. Module: Voltage Regulator

If V_{DDCORE} drops below approximately 2.45V while the on-chip core voltage regulator is enabled, and operating in Voltage Tracking mode, the REGSLP bit (WDTCON <7>) will be automatically cleared. The REGSLP bit cannot be set again by firmware until V_{DDCORE} rises back above the 2.45V approximate threshold.

Additionally, the REGSLP bit retains its previous state upon all Resets except POR.

Work around

None.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1		
X							

4. Module: SRAM

Any access to SRAM, either in the form of read or write operations, will increase the current consumption of the device, depending on how often the SRAM is accessed. A small current increase is normal, but in this cited silicon revision, the difference may be significant and of particular concern for low-power applications.

For further details, see Table 3.

TABLE 3: TYPICAL CURRENT CONSUMPTION

Case 1:			
Voltage Regulator Enabled Temperature = 25°C SEC_RUN mode using 32 kHz Timer1 Crystal			
Condition	**IDD (μA)**	**VDD (V)**	
No RAM access(1)	59	3.3	
Typ RAM access(2)	201	3.3	
Extreme RAM access(3)	906	3.3	
Case 2:			
Voltage Regulator Disabled VDDCORE is tied to VDD Temperature = 25°C SEC_RUN mode using 32 kHz Timer1 Crystal			
Condition	**IDD (μA)**	**VDD (V)**	**VDDCORE (V)**
No RAM access(1)	20	2.5	2.5
Typ RAM access(2)	132	2.5	2.5
Extreme RAM access(3)	723	2.5	2.5

Note 1: Code execution patterns where no instructions access SRAM.
2: Code execution that accesses SRAM, once every seven instruction cycles.
3: Code execution where every instruction cycle executes an instruction that accesses SRAM.

Work around

None.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1		
X							

5. Module: Low-Voltage Detect

The LVDSTAT, VDDCORE status bit (WDTCON<6>), is not implemented in this revision of silicon.

Work around

None.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1		
X							

6. Module: MSSPx (I²C™ Master)

If the module is in I²C Master mode, and the slave performs clock stretching, the first clock pulse after the slave releases the SCLx line may be narrower than the configured clock width. This may result in the slave missing the first clock in the next transmission/reception.

Work around

If the module is in I²C Master mode, do not allow the slave to perform clock stretching. Alternately, the master can slow down the SCLx clock frequency to a level where the slave can detect the narrowed clock pulse.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1		
X	X	X	X	X	X		

7. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In Synchronous Slave Transmission mode, the TRMT bit (TXSTA<1>) may not indicate when the TSR register is empty.

Work around

Instead of polling the TRMT bit to determine the status of the EUSART, poll the TXIF flag (PIR1<4>) to determine when new data can be written to the TXREG register.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1		
X	X	X	X	X	X		

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39778**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Table 27-1: Memory Programming Requirements

On page 398, the parameter, D132, which provides the minimum and maximum voltage levels of the Self-Timed Erase or Write for VDD and VDDCORE, are included. A new parameter (D133B) is added. The TWE parameter number and conditions column are changed. The changed/appended values are indicated in bold text in the following table:

TABLE 27-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	10K	—	—	E/W	-40°C to +85°C
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132B	VPEW	**Voltage for Self-Timed Erase or Write**					
		VDD	**2.35**	—	**3.6**	V	**ENVREG tied to VDD**
		VDDCORE	**2.25**	—	**2.7**	V	**ENVREG tied to VSS**
D133A	TIW	Self-Timed Write Cycle Time	—	2.8	—	ms	
D133B	**TIE**	**Self-Timed Page Erase Cycle Time**	**—**	**33.0**	**—**	**ms**	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	3	14	mA	
D140	TWE	Writes per Erase Cycle	—	—	1	—	**For each physical address**

† Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2. Module: Table 27-2: Comparator Specifications

On page 399, the maximum Input Offset Voltage (Parameter No. D300) is changed to ±25 mV.

The parameter numbers for TRESP and TMC2OV are changed to D303 and D304, respectively.

A new parameter, D305, for VIRV is added.

The changed/appended values are indicated in bold text in the following table:

TABLE 27-2: COMPARATOR SPECIFICATIONS

Operating Conditions: 3.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	±5.0	**±25**	mV	
D301	VICM	Input Common Mode Voltage	0	—	AVDD – 1.5	V	
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	
D303	TRESP	Response Time(1)	—	150	400	ns	
D304	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	µs	
D305	**VIRV**	**Internal Reference Voltage**	**—**	**1.2**	**—**	**V**	

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

3. Module: Table 27-4: Internal Voltage Regulator Specifications

On page 399, the comments column for the CF is changed. The note which states “These parameters are characterized but not tested” is removed. The changed content is indicated in bold text in the following table:

TABLE 27-4: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	VRGOUT	Regulator Output Voltage*	—	2.5	—	V	
	CF	External Filter Capacitor Value*	4.7	10	—	µF	**Capacitor must be low series resistance (<5 Ohms)**

4. Module: Section 27.3 "DC Characteristics: PIC18F87J11 Family (Industrial)"

On page 396, the characteristics and conditions of the Input Leakage Current are updated for the Analog (D060) and included for the Digital (D060A) I/O ports. The changed values are indicated in bold text in the following table:

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
		All I/O Ports:				
D030		with TTL Buffer	VSS	0.15 VDD	V	VDD < 3.3V
D030A			—	0.8	V	3.3V ≤ VDD ≤ 3.6V
D031		with Schmitt Trigger Buffer	VSS	0.2 VDD	V	
D032		$\overline{MCLR}$	VSS	0.2 VDD	V	
D033		OSC1	VSS	0.3 VDD	V	HS, HSPLL modes
D033A		OSC1	VSS	0.2 VDD	V	EC, ECPLL modes
D034		T1CKI	VSS	0.3	V	
	VIH	**Input High Voltage**				
		I/O Ports with Non 5.5V Tolerance:(2)				
D040		with TTL Buffer	0.25 VDD + 0.8V	VDD	V	VDD < 3.3V
D040A			2.0	VDD	V	3.3V ≤ VDD ≤ 3.6V
D041		with Schmitt Trigger Buffer	0.8 VDD	VDD	V	
		I/O Ports with 5.5V Tolerance:(2)				
Dxxx		with TTL Buffer	0.25 VDD + 0.8V	5.5	V	VDD < 3.3V
DxxxA			2.0	5.5	V	3.3V ≤ VDD ≤ 3.6V
Dxxx		with Schmitt Trigger Buffer	0.8 VDD	5.5	V	
D042		$\overline{MCLR}$	0.8 VDD	VDD	V	
D043		OSC1	0.7 VDD	VDD	V	HS, HSPLL modes
D043A		OSC1	0.8 VDD	VDD	V	EC, ECPLL modes
D044		T1CKI	1.6	VDD	V	
	IIL	**Input Leakage Current(1)**				
D060		**I/O Ports with Non 5.5V Tolerance(2)**	—	±1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D060A		**I/O Ports with 5.5V Tolerance(2)**	**—**	**±1**	**μA**	**VSS ≤ VPIN ≤ 5.5V, Pin at high-impedance**
D061		$\overline{MCLR}$	—	±1	μA	Vss ≤ VPIN ≤ VDD
D063		OSC1	—	±5	μA	Vss ≤ VPIN ≤ VDD

Note 1: Negative current is defined as current sourced by the pin.

2: Refer to Table 10-1 for the pins that have corresponding tolerance limits.

5. Module: Example 6-2: Erasing a Flash Program Memory Row

On page 94, an instruction to enable the write process to memory for erasing the Flash programming memory row is missing in the example. The changed content is indicated in bold text in the following example:

EXAMPLE 6-2: ERASING A FLASH PROGRAM MEMORY ROW

```
                MOVLW CODE_ADDR_UPPER          ; load TBLPTR with the base
                MOVWF TBLPTRU                  ; address of the memory block
                MOVLW CODE_ADDR_HIGH
                MOVWF TBLPTRH
                MOVLW CODE_ADDR_LOW
                MOVWF TBLPTRL
          ERASE_ROW
                BSF EECON1, WREN               ; enable write to memory
                BSF EECON1, FREE               ; enable Row Erase operation
                BCF INTCON, GIE                ; disable interrupts
      Required  MOVLW 55h
      Sequence  MOVWF EECON2                   ; write 55h
                MOVLW 0AAh
                MOVWF EECON2                   ; write 0AAh
                BSF EECON1, WR                 ; start erase (CPU stall)
                BSF INTCON, GIE                ; re-enable interrupts
```

6. Module: Section 19.3 “SPI Mode” and Section 19.4 “I²C™ Mode”

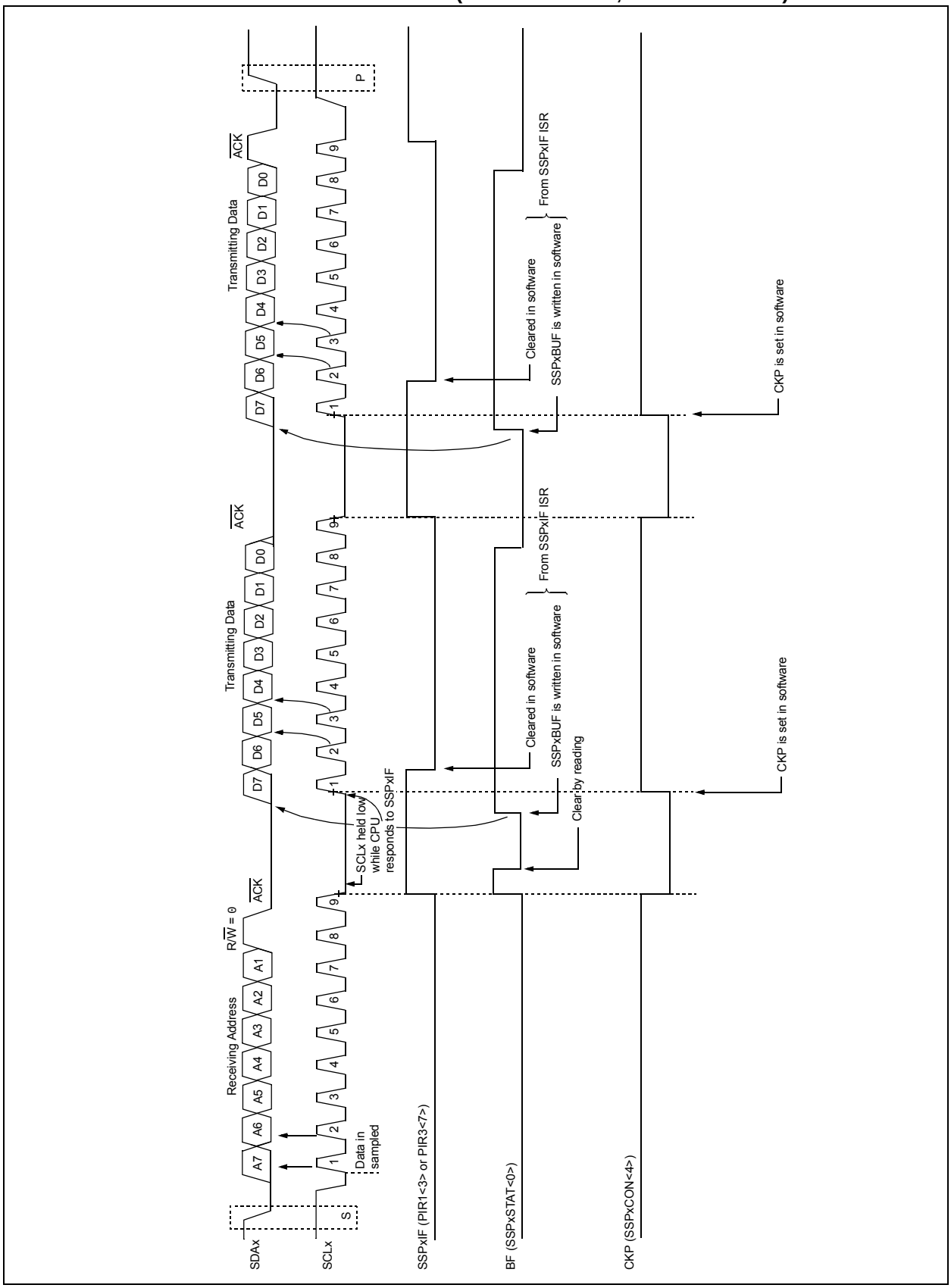
In **Section 19.3 “SPI Mode”** on page 223 and **Section 19.4 “I²C™ Mode”** on page 233, the following new note is included to describe the procedure to disable the MSSPx module:

Note:	Disabling the MSSPx module by clearing the SSPEN (SSPxCON1<5>) bit may not reset the module. It is recommended to clear the SSPxSTAT, SSPxCON1 and SSPxCON2 registers and select the mode prior to setting the SSPEN bit to enable the MSSPx module.

7. Module: Figure 19-10: I²C™ Slave Mode Timing (Transmission, 7-Bit Address)

On page 244, the figure is replaced with the new timing diagram provided in Figure 19-10.

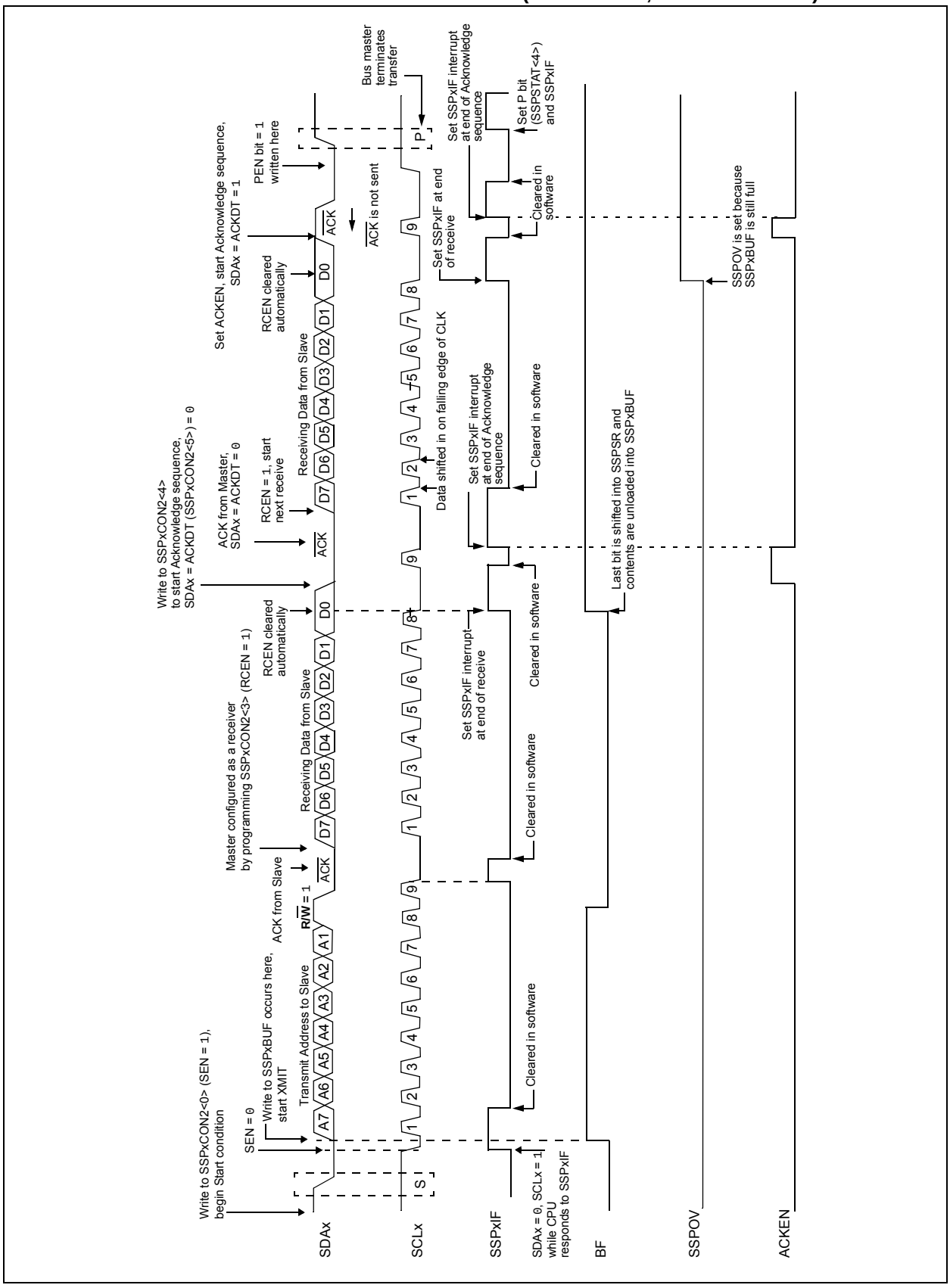
FIGURE 19-10: I²C™ SLAVE MODE TIMING (TRANSMISSION, 7-BIT ADDRESS)



8. Module: Figure 19-24: I²C™ Master Mode Waveform (Reception, 7-Bit Address)

On page 261, the condition (R/$\overline{W}$) when the Acknowledge signal (ACK) is received from the slave, after transmitting the address to the slave, is changed to ‘1’. The changed value is indicated in bold text in Figure 19-24.

FIGURE 19-24: I²C™ MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)



9. Module: Table 1-3: PIC18F6XJ1X Pinout I/O Descriptions

On page 20, the pin type for the RF3, RF4 and RF5 pins is changed from I (Input) to I/O (Input/Output). The changed content is indicated in bold text in the following table.

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	64-TQFP			
				PORTF is a bidirectional I/O port.
RF1/AN6/C2OUT	17			
RF1		I/O	ST	Digital I/O.
AN6		I	Analog	Analog input 6.
C2OUT		O	—	Comparator 2 output.
RF2/PMA5/AN7/C1OUT	16			
RF2		I/O	ST	Digital I/O.
PMA5		O	—	Parallel Master Port address.
AN7		I	Analog	Analog input 7.
C1OUT		O	—	Comparator 1 output.
RF3/AN8/C2INB	15			
RF3		**I/O**	ST	Digital **I/O**.
AN8		I	Analog	Analog input 8.
C2INB		I	Analog	Comparator 2 input B.
RF4/AN9/C2INA	14			
RF4		**I/O**	ST	Digital **I/O**.
AN9		I	Analog	Analog input 8.
C2INA		I	Analog	Comparator 2 input A.
RF5/AN10/C1INB/CV_{REF}	13			
RF5		**I/O**	ST	Digital **I/O**.
AN10		I	Analog	Analog input 10.
C1INB		I	Analog	Comparator 1 input B.
CV_{REF}		O	Analog	Comparator reference voltage output.
RF6/AN11/C1INA	12			
RF6		I/O	ST	Digital I/O.
AN11		I	Analog	Analog input 11.
C1INA		I	Analog	Comparator 1 input A.
RF7/$\overline{SS1}$	11			
RF7		I/O	ST	Digital I/O.
$\overline{SS1}$		I	TTL	SPI slave select input.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for ECCP2/P2A when Configuration bit, CCP2MX, is set.

2: Alternate assignment for ECCP2/P2A when Configuration bit, CCP2MX, is cleared.

10. Module: Memory Organization

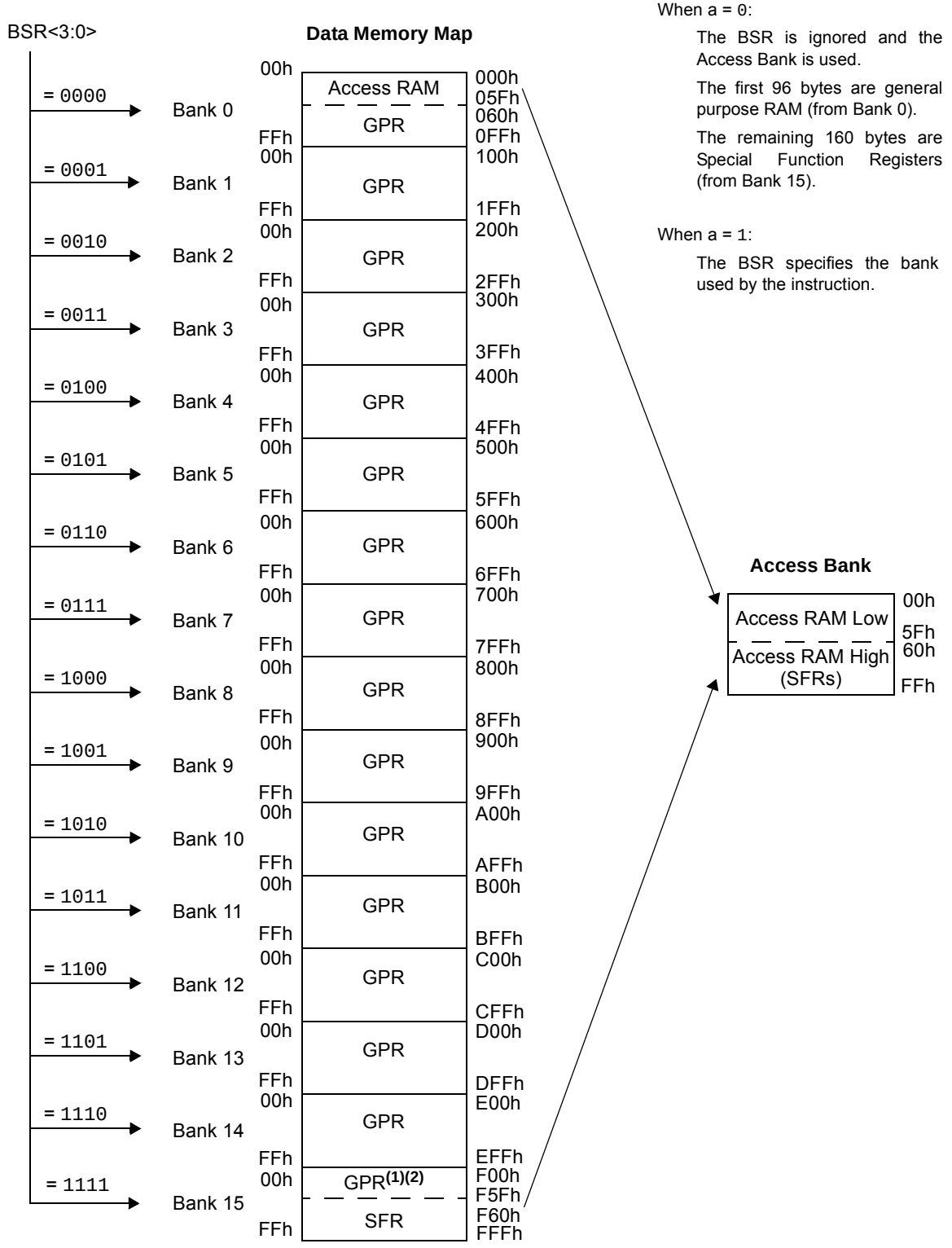
On page 75, the note at the end of **Section 5.3.4** "**Special Function Registers"** has been amended. The new information is indicated in bold text.

Note:	Addresses, F5Ah through F5Fh, are not part of the Access Bank. These registers must always be accessed using the Bank Select Register. **Addresses, F40h to F59h, are not implemented and not accessible to the user.**

11. Module: Memory Organization

On page 73, in Figure 5-7, Note 2 has been added. The additional note is indicated in bold text in Figure 5-7.

FIGURE 5-7: DATA MEMORY MAP FOR PIC18F87J11 FAMILY DEVICES



Note 1: Addresses F5Ah through F5Fh are also used by SFRs, but are not part of the Access RAM. Users must always use the complete address, or load the proper BSR value, to access these registers.

2: Addresses, F40h to F59h, are not implemented and are not accessible to the user.

12. Module: Guidelines for Getting Started with PIC18FJ Microcontrollers

Section 2.4 "Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)" has been replaced with a new and more detailed section. The entire text follows:

2.4 Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)

The on-chip voltage regulator enable pin, ENVREG, must always be connected directly to either a supply voltage or to ground. Tying ENVREG to VDD enables the regulator, while tying it to ground disables the regulator. Refer to **Section 23.3.2 "On-Chip Voltage Regulator"** for details on connecting and using the on-chip regulator.

When the regulator is enabled, a low-ESR (< 5Ω) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1 Capacitors with equivalent specification can be used.

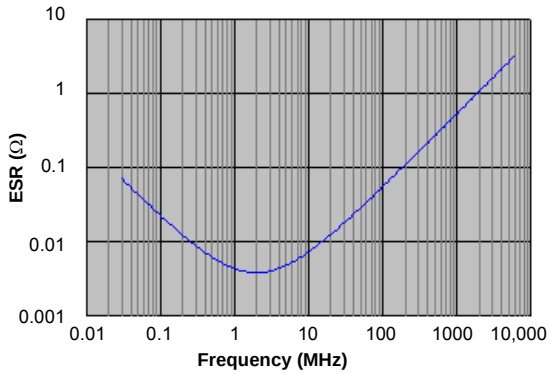
Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 26.0 "Electrical Characteristics"** for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 26.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

Note that the "LF" versions of some low pin count PIC18FJ parts (e.g., the PIC18LF45J10) do not have the ENVREG pin. These devices are provided with the voltage regulator permanently disabled; they must always be provided with a supply voltage on the VDDCORE pin.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at 25°C, 0V DC bias.

TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to 125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to 85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to 125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to 85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to 125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to 85ºC

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the VDDCORE voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

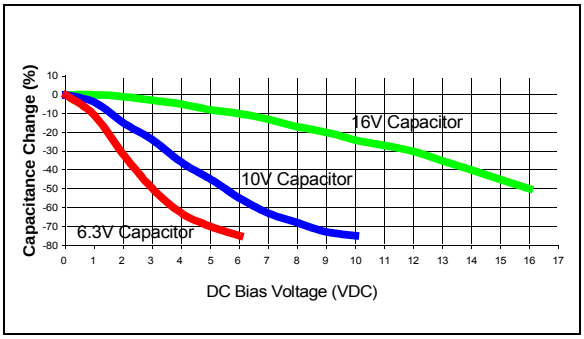
Typical low cost, 10 µF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 µF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum VDDCORE voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the Vddcore regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for X7R type and Y5V type capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the VDDCORE voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V VDDCORE voltage. Suggested capacitors are shown in Table 2-1.

DOCUMENT REVISION HISTORY

Rev A Document (2/2010)

Combined existing silicon and data sheet errata documents into the new, single document format. Added the A6 silicon revision, but no issues or clarifications.

This document replaces these errata documents:

- DS80418A, *"PIC18F87J11 Family Rev. A5 Silicon Errata"*
- DS80417A, *"PIC18F87J11 Family Rev. A4 Silicon Errata"*
- DS80344A, *"PIC18F87J11 Family Rev. A2 Silicon Errata"*
- DS80305B, *"PIC18F87J11 Family Rev. A1 Silicon Errata"*
- DS80408B, *"PIC18F87J11 Family Data Sheet Errata"*

Rev B Document (7/2010)

Added silicon issue 6 (MSSPx I^2C™ Master).

Added data sheet clarifications 10 and 11 (Memory Organization).

Rev C Document (8/2010)

Added silicon revision B0; includes existing silicon issues 1 (Master Synchronous Serial Port – MSSPx) and 6 (MSSPx – I^2C Master).

No new data sheet clarifications added.

Rev D Document (2/2011)

Replaced silicon revision B0 with revision C1 for lower pin count devices. Added silicon issue 12 (Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART). Removed data sheet clarification 12 (Electrical Characteristics).

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