

PIC18F2450/4450 Rev. A4 Silicon Errata

The PIC18F2450/4450 Rev. A4 parts you have received conform functionally to the Device Data Sheet (DS39760D), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2450/4450 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F2450/4450 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2450	0010 0100 001	0 0011
PIC18F4450	0010 0100 000	0 0011

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F2450/4450 silicon.

1. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN bit, RCSTA <7>, = 0)
- The EUSART is re-enabled (RCSTA <7> = 1)
- A two-cycle instruction is executed

Work around

Add a 2-TcY delay after re-enabling the EUSART.

1. Disable Receive Interrupts (RCIE bit, PIE1<5>, = 0).
2. Disable the EUSART (RCSTA <7>, = 0).
3. Re-enable the EUSART (RCSTA <7> = 1).
4. Re-enable Receive Interrupts (PIE1<5> = 1).
(This is the first TcY delay.)
5. Execute an NOP instruction.
(This is the second TcY delay.)

Date Codes that pertain to this issue:

All engineering and production devices.

PIC18F2450/4450

REVISION HISTORY

Rev A Document (10/2008)

Original release of this errata. Silicon issue 1 (EUSART).

Note the following details of the code protection feature on Microchip devices:

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