PIC24HJ12GP201/202 Rev. A2/A3/A4 Silicon Errata

The PIC24HJ12GP201/202 (Rev. A2/A3/A4) devices you received were found to conform to the specifications and functionality described in the following documents:

- "*PIC24HJ12GP201/202 Data Sheet*" (DS70282)
- "*dsPIC30F/33F Programmer's Reference Manual*" (DS70157)

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- PIC24HJ12GP201
- PIC24HJ12GP202

PIC24HJ12GP201/202 Rev. A2/A3/A4 silicon is identified by performing a "Reset and Connect" operation to the device using MPLAB® ICD 2 or MPLAB REAL ICE™ in-circuit emulator, with MPLAB IDE v7.60 or later. The output window will show a successful connection to the device specified in *Configure>Select Device*. The resulting DEVREV register values for Rev. A2/A3/A4 silicon are 0x3001, 0x3002, and 0x3003, respectively.

The errata described in this document will be addressed in future revisions of silicon.

Silicon Errata Summary

The following list summarizes the errata described in further detail in the remainder of this document:

1. JTAG Programming

   JTAG programming does not work.

2. UART

   UART receptions may be corrupted if the Baud Rate Generator (BRG) is set up for 4x mode.

3. UART

   The auto-baud feature may not calculate the correct baud rate when the BRG is set up for 4x mode.

4. UART

   With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.

5. UART

   The auto-baud feature measures baud rate inaccurately for certain baud rate and clock speed combinations.

6. Traps and Idle Mode

   If a clock failure occurs when the device is in Idle mode, the oscillator failure trap does not vector to the Trap Service Routine (TSR).

7. UART

   When an auto-baud is detected, the receive interrupt may occur twice.

8. UART

   When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

9. UART Module

   The 16x baud clock signal on the BCLK pin is present only when the module is transmitting.

10. SPI Module

    The SPIxCON1 DISSCK bit does not influence port functionality.

11. I^2C™ Module

    The BCL bit in I2CSTAT can only be cleared with a 16-bit operation, and can be corrupted with 1-bit or 8-bit operations on I2CSTAT.

12. I^2C Module

    The ACKSTAT bit is cleared shortly after being set following a slave transmit.

13. I^2C Module: 10-bit Addressing Mode

    When the I^2C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I^2C devices, the A10 and A9 bits may not work as expected.

14. Product Identification

    Revision A2 devices marked as extended temperature range (E) devices only support industrial temperature range (I).

15. UART (UxE Interrupt)

    The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

16. UART Module

    When the UART module is operating in 8-bit mode (PDSEL = 0x) and using the IrDA® encoder/ decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

17. Internal Voltage Regulator

    When the VREGS (RCON<8>) bit is set to a logic '0', higher sleep current may be observed.

18. PSV Operations

    An address error trap occurs in certain addressing modes when accessing the first four bytes of any PSV page.

19. I^2C Module: 10-bit Addressing Mode

    When the I^2C module is configured as a 10-bit slave with an address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02.

20. I^2C Module

    With the I^2C module enabled, the port bits and external interrupt input functions (if any) associated with SCL and SDA pins do not reflect the actual digital logic levels on the pins.

21. I^2C Module: 10-bit Addressing Mode

    The 10-bit slave does not set the RBF flag or load the I2CxRCV register on address match if the Least Significant bits of the address are the same as the 7-bit reserved addresses.

The following sections describe the errata and work around to these errata, where they may apply.

1. Module: JTAG Programming

JTAG programming does not work.

Work around

None.

2. Module: UART

UART receptions may be corrupted if the Baud Rate Generator is set up for 4x mode (BRGH = 1).

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

3. Module: UART

The auto-baud feature may not calculate the correct baud rate when the High Baud Rate Enable bit, BRGH, is set. With the BRGH bit set, the baud rate calculation used is the same as BRG = 0.

Work around

If the auto-baud feature is needed, use the Low Baud Rate mode by clearing the BRGH bit.

4. Module: UART

With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.

Work around

To prevent the Sync Break character from being loaded into the FIFO, load the UxBRG register with either 0x0000 or 0xFFFF prior to enabling the auto-baud feature (ABAUD = 1).

5. Module: UART

The auto-baud feature may miscalculate certain baud rate and clock speed combinations, resulting in a BRG value that is greater than or less than the expected value by 1. This may result in reception or transmission failures.

Work around

Test the auto-baud rate at various clock speed and baud rate combinations that would be used in an application. If an inaccurate BRG value is generated, manually correct the baud rate in user software.

6. Module: Traps and Idle Mode

If a clock failure occurs when the device is in Idle mode, the oscillator failure trap does not vector to the Trap Service Routine. Instead, the device will simply wake-up from Idle mode and continue code execution if the Fail-Safe Clock Monitor (FSCM) is enabled.

Work around

Whenever the device wakes up from Idle (assuming the FSCM is enabled) the user software should check the state of the OSCFAIL bit (INTCON1<1>) to determine whether a clock failure occurred, and then perform the appropriate clock switch operation. Regardless, the Trap Service Routine must be included in the user application.

7. Module: UART

When an auto-baud is detected, the receive interrupt may occur twice. The first interrupt occurs at the beginning of the Start bit and the second after reception of the Sync field character.

Work around

If an extra interrupt is detected, ignore the additional interrupt.

8. Module: UART

When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

This issue does not affect the other UART configurations.

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

9. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = 11), the 16x baud clock signal on the BCLK pin is present only when the module is transmitting. The pin is idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

10. Module: SPI

Setting the DISSCK bit in the SPIxCON1 register does not allow the user application to use the SCK pin as a general purpose I/O pin.

Work around

None.

11. Module: I^2C

The BCL bit in I2CSTAT can be cleared only with a 16-bit operation, and can be corrupted with 1-bit or 8-bit operations on I2CSTAT.

Work around

Use 16-bit operations to clear BCL.

12. Module: I^2C

During I^2C communication, after a device operating in Slave mode transmits data to the master, the ACKSTAT bit in the I2CxSTAT register is set or cleared depending on whether the master sent an ACK or NACK after the byte of data. If the ACKSTAT bit is set, it will be cleared again after some delay.

Work around

Store the value of the ACKSTAT bit immediately after an I^2C interrupt occurs.

13. Module: I^2C

If there are two I^2C devices on the bus, one of them is acting as the Master receiver and the other as the Slave transmitter. If both devices are configured for 10-bit addressing mode, and have the same value in the A10 and A9 bits of their addresses, then when the Slave select address is sent from the Master, both the Master and Slave acknowledge it. When the Master sends out the read operation, both the Master and the Slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

Work around

In all I^2C devices, the addresses as well as bits A10 and A9 should be different.

14. Module: Product Identification

Revision A2 devices marked as extended temperature range (E) devices only support industrial temperature range (I).

Work around

Use Revision A3 or newer devices marked as extended temperature range (E) devices.

15. Module: UART (UxE Interrupt)

The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur.

16. Module: UART (IrDA®)

When the UART is operating in 8-bit mode (PDSEL = 0x) and using the IrDA encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

Work around

None.

17. Module: Internal Voltage Regulator

When the VREGS (RCON<8>) bit is set to a logic '0', higher sleep current may be observed.

Work around

Ensure VREGS (RCON<8>) bit is set to a logic '1' for device Sleep mode operation.

18. Module: PSV Operations

An address error trap occurs in certain addressing modes when accessing the first four bytes of an PSV page. This only occurs when using the following addressing modes:

- MOV.D
- Register indirect addressing (word or byte mode) with pre/post-decrement

Work around

Do not perform PSV accesses to any of the first four bytes using the above addressing modes. For applications using the C language, MPLAB C30 version 3.11 or higher, provides the following command-line switch that implements a work around for the erratum.

```
-merrata=psv_trap
```

Refer to the `readme.txt` file in the MPLAB C30 v3.11 tool suite for further details.

19. Module: I²C

When the I²C module is configured as a 10-bit slave with and address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02; however, the module acknowledges both address bytes.

Work around

None.

20. Module: I²C

With the I²C module enabled, the port bits and external interrupt input functions (if any) associated with the SCL and SDA pins do not reflect the actual digital logic levels on the pins.

Work around

If the SDA and/or SCL pins need to be polled, these pins should be connected to other port pins in order to be read correctly. This issue *does not* affect the operation of the I²C module.

21. Module: I²C

In 10-bit Addressing mode, some address matches don't set the RBF flag or load the receive register, I2CxRCV, if the lower address byte matches the reserved addresses. In particular, these include all addresses with the form XX0000XXXX and XX1111XXXX, with the following exceptions:

- 001111000X
- 011111001X
- 101111010X
- 111111011X

Work around

Ensure that the lower address byte in 10-bit Addressing mode does not match any 7-bit reserved addresses.

APPENDIX A: REVISION HISTORY

Revision A (5/2007)

Initial release of this document, which includes silicon issues 1 (JTAG Programming), 2 (UART) through 5 (UART) and 6 (Traps and Idle Mode).

Revision B (11/2007)

Added silicon issues 7 (UART) and 8 (UART).

Revision C (4/2008)

Added silicon issues 9 (UART), 10 (SPI), 11-13 (I^2C) and 14 (Product Identification).

Revision D (9/2008)

Added reference to silicon revision A4. Updated silicon issue 14 (Product Identification). Added silicon issues 15 (UART (UxE Interrupt)), 16 (UART (IrDA®)), 17 (Internal Voltage Regulator), 18 (PSV Operations), and 19-21 (I^2C).

NOTES:

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