# PIC18F2221/2321/4221/4321 Family Silicon Errata and Data Sheet Clarification

The PIC18F2221/2321/4221/4321 devices that you have received conform functionally to the current Device Data Sheet (DS39689**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F2221/2321/4221/4321 silicon.

| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B3**). |
|---|---|

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

| **Note:** | If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance. |
|---|---|

The DEVREV values for the various PIC18F2221/2321/4221/4321 silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | Device ID(1) | Revision ID for Silicon Revision(2) | | |
|---|---|---|---|---|
| | | B2 | B3 | |
| PIC18F2221 | 216h | 2h | 3h | |
| PIC18F2321 | 212h | | | |
| PIC18F4221 | 214h | | | |
| PIC18F4321 | 210h | | | |

**Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

**2:** Refer to the *"PIC18F2XXX/4XXX Family Flash Microcontroller Programming Specification"* (DS39622) for detailed information on Device and Revision IDs for your specific device.

**TABLE 2: SILICON ISSUE SUMMARY**

| Module | Feature | Item Number | Issue Summary | Affected Revisions(1) | | |
|---|---|---|---|---|---|---|
| | | | | B2 | B3 | |
| 10-Bit A/D | 2 TOSC or RC | 1. | When the A/D clock source is set as 2 TOSC or RC, the Integral Linearity Error and Differential Linearity Error may exceed the data sheet specification, in extremely rare cases, at codes 511 and 512. | X | X | |
| MSSP | $I^2C$™ Slave Reception | 2. | When configured for $I^2C$ slave reception, the MSSP module may not receive the correct data if the SSPBUF register is not read within a window after an SSPIF interrupt occurs | X | X | |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

## Silicon Errata Issues

| | |
|---|---|
| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B3**). |

### 1. Module: 10-Bit Analog-to-Digital Converter (A/D)

When the AD clock source is selected as 2 TOSC or RC (when ADCS<2:0 = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512.

**Work around**

Select the AD clock source as 4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC or 64 TOSC and avoid selecting 2 TOSC or RC.

**Affected Silicon Revisions**

| B2 | B3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 2. Module: Master Synchronous Serial Port (MSSP)

When configured for $I^2C$™ slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

**Work around**

The issue can be resolved in either of these ways:

- Prior to the $I^2C$ slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

**Affected Silicon Revisions**

| B2 | B3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39689**F**):

| **Note:** | Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity. |
|---|---|

### 1. Module: Configuration Bits and Device IDs

Table 23-1: Configuration Bits and Device IDs, on Page 253, has been changed to designate Bit 3 of CONFIG4L as unimplemented.

The table is changed as shown.

**TABLE 23-1: CONFIGURATION BITS AND DEVICE IDs**

| File Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default/ Unprogrammed Value |
|---|---|---|---|---|---|---|---|---|---|---|
| 300001h | CONFIG1H | IESO | FCMEN | — | — | FOSC3 | FOSC2 | FOSC1 | FOSC0 | 00-- 0111 |
| 300002h | CONFIG2L | — | — | — | BORV1 | BORV0 | BOREN1 | BOREN0 | $\overline{\text{PWRTEN}}$ | ---1 1111 |
| 300003h | CONFIG2H | — | — | — | WDTPS3 | WDTPS2 | WDTPS1 | WDTPS0 | WDTEN | ---1 1111 |
| 300005h | CONFIG3H | MCLRE | — | — | — | — | LPT1OSC | PBADEN | CCP2MX | 1--- -011 |
| 300006h | CONFIG4L | $\overline{\text{DEBUG}}$ | XINST | BBSIZ1 | BBSIZ0 | — | LVP | — | STVREN | 1000 -1-1 |
| 300008h | CONFIG5L | — | — | — | — | — | — | CP1 | CP0 | ---- --11 |
| 300009h | CONFIG5H | CPD | CPB | — | — | — | — | — | — | 11-- ---- |
| 30000Ah | CONFIG6L | — | — | — | — | — | — | WRT1 | WRT0 | ---- --11 |
| 30000Bh | CONFIG6H | WRTD | WRTB | WRTC | — | — | — | — | — | 111- ---- |
| 30000Ch | CONFIG7L | — | — | — | — | — | — | EBTR1 | EBTR0 | ---- --11 |
| 30000Dh | CONFIG7H | — | EBTRB | — | — | — | — | — | — | -1-- ---- |
| 3FFFFEh | DEVID1(1) | DEV2 | DEV1 | DEV0 | REV4 | REV3 | REV2 | REV1 | REV0 | xxxx xxxx(2) |
| 3FFFFFh | DEVID2(1) | DEV10 | DEV9 | DEV8 | DEV7 | DEV6 | DEV5 | DEV4 | DEV3 | 0000 1100 |

**Legend:** x = unknown, u = unchanged, - = unimplemented, q = value depends on condition.
Shaded cells are unimplemented, read as '0'.

**Note 1:** Unimplemented in PIC18F2221/4221 devices; maintain these bits set.

**2:** See Register 23-14 for DEVID1 values. DEVID registers are read-only and cannot be programmed by the user.

## 2. Module: CONFIG4L Register

Register 23-5 CONFIG4L: Configuration Register 4 Low (Byte Address 300006h), on Page 258, has been changed to designate Bit 3 of CONFIG4L as unimplemented.

The register is changed as shown.

**REGISTER 23-5: CONFIG4L: CONFIGURATION REGISTER 4 LOW (BYTE ADDRESS 300006h)**

| R/P-1 | R/P-0 | U-0 | U-0 | U-0 | R/P-1 | U-0 | R/P-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{DEBUG}}$ | XINST | BBSIZ1 | BBSIZ0 | — | LVP | — | STVREN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **$\overline{\text{DEBUG}}$:** Background Debugger Enable bit
1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins
0 = Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug

bit 6 **XINST:** Extended Instruction Set Enable bit
1 = Instruction set extension and Indexed Addressing mode enabled
0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)

bit 5-4 **BBSIZ<1:0>:** Boot Block Size Select bits

Feature2 Devices:
1x = 1024 Words
01 = 512 Words
00 = 256 Words

Feature1 Devices:
1x = 512 Words
x1 = 512 Words
00 = 256 Words

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **LVP:** Single-Supply ICSP™ Enable bit
1 = Single-Supply ICSP enabled
0 = Single-Supply ICSP disabled

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **STVREN:** Stack Full/Underflow Reset Enable bit
1 = Stack full/underflow will cause Reset
0 = Stack full/underflow will not cause Reset

## APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (7/2006)

First revision of this document. Silicon issue 1 (MSSP).

Rev B Document (6/2007)

Added silicon issue 2 (10-Bit Analog-to-Digital Converter).

Rev C Document (5/2010)

Converted existing silicon errata and data sheet errata documents to new, combined format. Removed issue 1 (MSSP), making former issue 2 (10-Bit A/D) issue 1. Added silicon issue 2 (MSSP) and removed data sheet clarifications 1-3 and 6-14.

This document replaces these errata documents:

- DS80285B, *"PIC18F2221/2321/4221/4321 Rev. B2 Silicon Errata"* – DS number assumed by this errata
- DS80310G, *"PIC18F2221/2321/4221/4321 Data Sheet Errata"* – Document retired

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