# PIC18F85J90 Family
# Silicon Errata and Data Sheet Clarification

The PIC18F85J90 family devices that you have received conform functionally to the current Device Data Sheet (DS39770**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F85J90 family silicon.

| | |
|---|---|
| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A6**). |

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

| | |
|---|---|
| **Note:** | If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance. |

The DEVREV values for the various PIC18F85J90 family silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | Device ID(1) | Revision ID for Silicon Revision(2) | | | |
|---|---|---|---|---|---|
| | | A3 | A4 | A5 | A6 |
| PIC18F63J90 | 380Xh | 3h | 4h | 5h | 6h |
| PIC18F64J90 | 382Xh | | | | |
| PIC18F65J90 | 386Xh | | | | |
| PIC18F83J90 | 388Xh | | | | |
| PIC18F84J90 | 38AXh | | | | |
| PIC18F85J90 | 38EXh | | | | |

**Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

**2:** Refer to the *"PIC18F6XJXX/8XJXX Family Flash Microcontroller Programming Specification"* (DS39644) for detailed information on Device and Revision IDs for your specific device.

**TABLE 2: SILICON ISSUE SUMMARY**

| Module | Feature | Item Number | Issue Summary | Affected Revisions(1) | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | A3 | A4 | A5 | A6 | |
| Reset | BOR | 1. | BOR and POR may occur the same time | X | X | X | X | |
| MSSP | $I^2C$™ Master | 2. | If the SSPBUF register is not read within a window after the SSPIF interrupt, the module may not receive the correct data. | X | X | X | X | |
| MSSP | $I^2C$ Master | 3. | The Clock may get Narrow if the Slave performs a clock stretch. | X | X | X | X | |
| EUSART | Enable/ Disable | 4. | If interrupts are enabled, disabling and re-enabling the module requires a 2 TCY delay. | X | X | X | X | |
| Timer1/3 | Counter | 5. | Timer1/3 in internal counter mode will not increment in the instruction count where the Timer is disabled. | X | X | X | X | |
| Timer1/3 | Prescale | 6. | Timer1/3 Prescale will take additional count to Switch when prescaler value is changed. | X | X | X | X | |
| EUSART | Synchronous mode | 7. | The TRMT bit may not indicate when the TSR register is empty. | X | X | X | X | |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

## Silicon Errata Issues

| | |
|---|---|
| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**). |

### 1. Module: Reset

When a Brown-out Reset (BOR) occurs and the $\overline{BOR}$ bit is reset, the Power-on Reset ($\overline{POR}$) bit also may be reset. The resulting state matches that of the RCON register following a Power-on Reset event.

Consequently, an application may not be able to detect whether a BOR or POR event has occurred.

**Work around**

None.

**Affected Silicon Revisions**

| A3 | A4 | A5 | A6 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 2. Module: MSSP ($I^2C$™ Slave)

In extremely rare cases when configured for $I^2C$™ slave reception, the MSSP module may not receive the correct data. This occurs only if the Serial Receive/Transmit Buffer register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR<3>) has occurred.

**Work around**

The issue can be resolved in either of these ways:

- Prior to the $I^2C$ slave reception, enable the clock stretching feature. This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPIF bit is set, read the SSPBUF before the first rising clock edge of the next byte being received.

**Affected Silicon Revisions**

| A3 | A4 | A5 | A6 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 3. Module: MSSP ($I^2C$™ Master)

When in $I^2C$ Master mode, if the slave performs clock stretching, the first clock pulse after the slave releases the SCL line may be narrower than the configured clock width. This may result in the slave missing the first clock in the next transmission/reception.

**Work around**

The clock pulse will be the normal width if the slave does not perform clock stretching.

**Affected Silicon Revisions**

| A3 | A4 | A5 | A6 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 4. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations, when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN bit, RCSTA<7> = 0)
- The EUSART is re-enabled (RCSTA<7> = 1)
- A two-cycle instruction is executed

**Work around**

Add a 2 TCY delay after re-enabling the EUSART.

1. Disable receive interrupts (RCIE bit, PIE1<5>) = 0).
2. Disable the EUSART (RCSTA<7> = 0).
3. Re-enable the EUSART (RCSTA<7> = 1).
4. Re-enable receive interrupts (PIE1<5> = 1).

   (This is the first TCY delay.)
5. Execute a NOP instruction.

   (This is the second TCY delay.)

**Affected Silicon Revisions**

| A3 | A4 | A5 | A6 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 5. Module: Timer 1/3

When either Timer1 or Timer3 is configured for the internal clock source (FOSC/4, TxCON<1>(TMRxCS) = 0) and in the 8/16-Bit Counter mode (TxCON<7>(RD16) = 0 or 1), TMRxH and TMRxL will not increment on the instruction that turns off the counter (TxCON<0> (TMRxON) = 0).

**Work around**

None.

**Affected Silicon Revisions**

| A3 | A4 | A5 | A6 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 6. Module: Timer 1/3

When either Timer1 or Timer3 is in the 8/16-Bit Counter mode (TXCON<7> (RD16) = 0 or 1), incrementing the prescale value (TxCON<5:4> (TXCKPS<1:0>)) will take an additional count at the previous value before the prescale value is updated.

For example, changing the prescale value from 1:4 to 1:8 will occur four instruction cycles after the execution of the instruction to update the prescaler.

**Work around**

None.

**Affected Silicon Revisions**

| A3 | A4 | A5 | A6 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 7. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In Synchronous Slave Transmission mode, the TRMT bit (TXSTA<1> may not indicate when the TSR register is empty.

**Work around**

Instead of polling the TRMT bit to determine the status of the EUSART, poll the TXIF flag (PIR1<4>) to determine when new data can be written to the TXREG register.

**Affected Silicon Revisions**

| A3 | A4 | A5 | A6 | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39770**C**):

| | |
|---|---|
| **Note:** | Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity. |

### 1. Module: Guidelines for Getting Started with PIC18FJ Microcontrollers

**Section 2.4 "Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)"** has been replaced with a new and more detailed section. The entire text follows:

## 2.4 Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)

The on-chip voltage regulator enable pin, ENVREG, must always be connected directly to either a supply voltage or to ground. Tying ENVREG to VDD enables the regulator, while tying it to ground disables the regulator. Refer to **Section 23.3.2 "On-Chip Voltage Regulator"** for details on connecting and using the on-chip regulator.

When the regulator is enabled, a low-ESR (< 5Ω) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1 Capacitors with equivalent specification can be used.

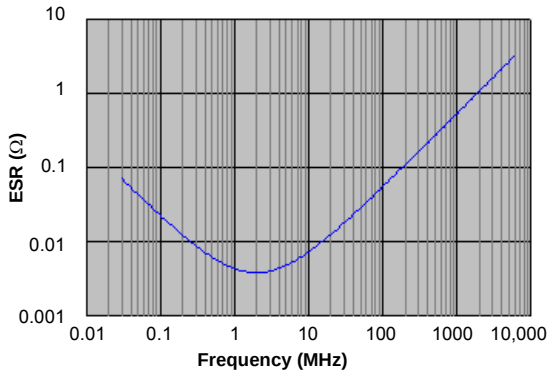
Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 26.0 "Electrical Characteristics"** for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 26.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

Note that the "LF" versions of some low pin count PIC18FJ parts (e.g., the PIC18LF45J10) do not have the ENVREG pin. These devices are provided with the voltage regulator permanently disabled; they must always be provided with a supply voltage on the VDDCORE pin.

**FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP**




**Note:** Typical data measurement at 25°C, 0V DC bias.

**TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS**

| Make | Part # | Nominal Capacitance | Base Tolerance | Rated Voltage | Temp. Range |
|---|---|---|---|---|---|
| TDK | C3216X7R1C106K | 10 µF | ±10% | 16V | -55 to 125ºC |
| TDK | C3216X5R1C106K | 10 µF | ±10% | 16V | -55 to 85ºC |
| Panasonic | ECJ-3YX1C106K | 10 µF | ±10% | 16V | -55 to 125ºC |
| Panasonic | ECJ-4YB1C106K | 10 µF | ±10% | 16V | -55 to 85ºC |
| Murata | GRM32DR71C106KA01L | 10 µF | ±10% | 16V | -55 to 125ºC |
| Murata | GRM31CR61C106KC31L | 10 µF | ±10% | 16V | -55 to 85ºC |

### 2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the VDDCORE voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

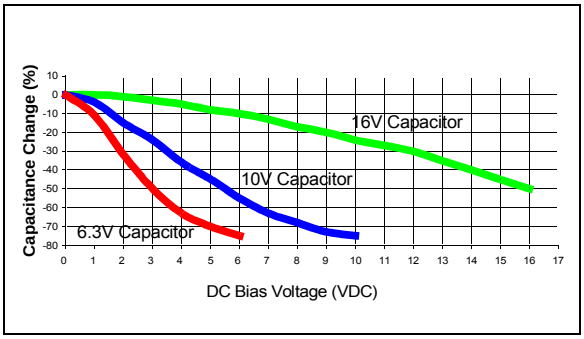
Typical low cost, 10 µF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 µF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum VDDCORE voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the Vddcore regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for X7R type and Y5V type capacitors is shown in Figure 2-4.

**FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS**




When selecting a ceramic capacitor to be used with the VDDCORE voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V VDDCORE voltage. Suggested capacitors are shown in Table 2-1.

## 2. Module: Electrical Characteristics

Changes, shown in bold, have been made to the D005 row in Table 26.1. The updated table is shown below:

**TABLE 26.1 DC Characteristics: Supply Voltage PIC18F85J90 Family (Industrial)**

| PIC18F85J90 Family (Industrial) | | | Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Conditions |
| D001 | VDD | Supply Voltage | VDDCORE<br>2.0 | —<br>— | 3.6<br>3.6 | V<br>V | ENVREG tied to Vss<br>ENVREG tied to VDD |
| D001B | VDDCORE | External Supply for Microcontroller Core | 2.0 | — | 2.70 | V | ENVREG tied to Vss |
| D001C | AVDD | Analog Supply Voltage | VDD – 0.3 | — | VDD + 0.3 | V | |
| D001D | AVSS | Analog Ground Potential | VSS – 0.3 | — | VSS + 0.3 | V | |
| D002 | VDR | RAM Data Retention Voltage(1) | 1.5 | — | — | V | |
| D003 | VPOR | VDD Start Voltage to Ensure Internal Power-on Reset Signal | — | — | 0.7 | V | See Section 5.3 “Power-on Reset (POR)” for details |
| D004 | SVDD | VDD Rise Rate to Ensure Internal Power-on Reset Signal | 0.05 | — | — | V/ms | See Section 5.3 “Power-on Reset (POR)” for details |
| D005 | VBOR(2) | Brown-out Reset Voltage | **1.92** | **2.0** | **2.2** | V | |

**Note 1:** This is the limit to which VDDCORE can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

**2: Device will operate normally until Brown-out Reset occurs, even though VDD may be below VDDMIN.**

## 3. Module: I/O Ports

In **Section 10.1 “I/O Port Pin Capabilities”**, the following changes are made.

### 10.1.1 INPUT PINS AND VOLTAGE CONSIDERATIONS

The voltage tolerance of pins used as device inputs is dependent on the pin’s input function. Most pins that are used as digital only inputs are able to handle DC voltages up to 5.5V, a level typical for digital logic circuits. The digital pins that cannot exceed VDD are RE0, RE1, RE2, RG0, RG2 and RG3.

In contrast, pins that also have analog input functions of any kind can only tolerate voltages up to VDD. On these pins, voltage excursions beyond VDD should be avoided.

Table 10-1 summarizes the input voltage capabilities. The changes are shown in bold. Refer to **Section 26.0 “Electrical Characteristics”** for more details.

**TABLE 10-1: INPUT VOLTAGE TOLERANCE**

| Port or Pin | Tolerated Input | Description |
|---|---|---|
| PORTA<7:0> | VDD | Only VDD input levels are tolerated. |
| PORTC<1:0> | | |
| **PORTE<1:0>** | | |
| PORTF<7:1> | | |
| **PORTG<3:2,0>** | | |
| PORTB<7:0> | 5.5V | Tolerates input levels above VDD; useful for most standard logic. |
| PORTC<7:2> | | |
| PORTD<7:0> | | |
| PORTE<7:3> | | |
| PORTG<4,1> | | |
| PORTH<7:0>(1) | | |
| PORTJ<7:0>(1) | | |

**Note 1:** Not available on 64-pin devices.

**4. Module: I/O Ports**

In **Section 10.6 "PORTE, TRISE and LATE Registers"**, the following changes are made. The changes are shown in bold text.

## 10.6 PORTE, TRISE and LATE Registers

PORTE is a 7-bit wide, bidirectional port. The corresponding Data Direction and Data Latch registers are TRISE and LATE. **All pins on PORTE are digital only. PORTE<7:3> can tolerate voltages up to 5.5V and PORTE<1:0> are only VDD level tolerant.**

**5. Module: I/O Ports**

In **Section 10.8 "PORTG, TRISG and LATG Registers"**, the following changes are made. The changes are shown in bold text.

## 10.8 PORTG, TRISG and LATG Registers

PORTG is a 5-bit wide, bidirectional port. The corresponding Data Direction and Data Latch registers are TRISG and LATG. **All pins on PORTG are digital only. PORTG<4> and PORTG<1> can tolerate voltages up to 5.5V. PORTG<3:2> and PORTG<0> are VDD level tolerant only.**

## APPENDIX A: DOCUMENT REVISION HISTORY

Rev B Document (11/2010)

Initial release of the combined, silicon errata/data sheet clarification document. New data sheet clarifications 1 (Guidelines for Getting Started with PIC18FJ Microcontrollers), 2 (Electrical Characteristics) and 3-5 (I/O Ports).

This document replaces these errata documents:

- DS80312A, *"PIC18F85J90 Family Rev. A3 Silicon Errata"*
- DS80424A, *"PIC18F85J90 Family Rev. A4 Silicon Errata"*
- DS80472A, *"PIC18F85J90 Family Rev. A5 Silicon Errata"*
- DS80488A, *"PIC18F85J90 Family Rev. A6 Silicon Errata"*
- DS80286E, *"PIC18F85J90 Family Data Sheet Errata"*

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