dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Family Silicon Errata and Data Sheet Clarification

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 family devices that you have received conform functionally to the current Device Data Sheet (DS70318**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 14, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A2	A3	A4
dsPIC33FJ06GS101	0x0C00	0x3002	0x3003	0x3004
dsPIC33FJ06GS102	0x0C01			
dsPIC33FJ06GS202	0x0C02			
dsPIC33FJ16GS402	0x0C04			
dsPIC33FJ16GS404	0x0C06			
dsPIC33FJ16GS502	0x0C03			
dsPIC33FJ16GS504	0x0C05			

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A2	A3	A4
PWM	Leading-Edge Blanking	1.	Reading LEBCONx registers, as well as writing individual bits and bytes within these registers, does not work.	X	X	X
PWM	Immediate Updates	2.	PWM Immediate Update mode (IEU = 1) for the Master Duty Cycle register (MDC) is not functional.	X	X	X
PWM	Status Bits	3.	PWM Fault Status bits do not function if the associated PWM Fault interrupts are disabled.	X	X	X
PWM	Clock	4.	PWM output will exhibit jitter with some PWM clock divider settings.	X	X	X
PWM	Faults	5.	If the PWM is in Complementary, Redundant and Push-Pull mode and the Independent Time Base bit (ITB) is set, the Independent Fault mode may not work as expected for the PWMxL pin.	X	X	X
PWM	Independent Time Base	6.	The independent time base PWM outputs may not be synchronized with the Master time base PWM outputs when both modes are used simultaneously.	X	X	X
PWM	Latched Faults	7.	In PWM Latched Fault mode, the PWM outputs may be latched on both the rising as well as the falling edge of the Fault signal regardless of the fault input polarity selection (set with the FCLCONx<FLTPOL> bit setting).	X	X	X
PWM	Faults	8.	A bit write to the CLMOD bit (bit 8) in the FCLCONx register, or consecutive writes to the lower byte and higher byte of the FCLCONx register, causes all other bits of the high byte to be loaded with zeros.	X	X	X
PWM	Sleep Mode	9.	The PWM module fails to wake the CPU from Sleep mode on a PWM fault event.	X	X	X
Comparator	—	10.	For slow input signals, the Comparator module may generate erroneous triggers/interrupts.	X	X	X
ADC	Clock	11.	Selecting the primary FRC (FVCO) as a clock source for the ADC module by setting the SLOWCLK bit (ADCON<12>) to the default setting of '0', does not work.	X	X	X
Auxiliary Clock	Module Disable	12.	When the PWMMD bit in the PMD1 register is set, the Auxiliary Clock to both the ADC and PWM modules is disabled.	X	X	X
Comparator	Interrupts	13.	Comparator interrupts are incorrectly generated when the High-Speed Analog Comparator is configured for an inverted polarity setting (CMPCONx<CMPPOL> = 1).	X	X	X
UART	4x Mode	14.	When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.	X	X	X
UART	IR Interface Operations	15.	The 16x baud clock signal on the BCLK pin is present only when the module is transmitting.	X	X	X
I^2C™	10-bit Addressing Mode	16.	When the I^2C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I^2C devices, the A10 and A9 bits may not work as expected.	X	X	X
PWM	ADC Conversion	17.	The PWM module may fail to trigger a conversion on certain ADC pairs when the primary or secondary PWMx generator is selected as a trigger source.	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A2	A3	A4
PGEC3/ PGED3 Programming Pins	Device Programming	18.	When using the PGEC3/PGED3 pins for device programming, the programming time may be slower as compared to other available PGECx/PGEDx pin pairs.	X	X	X
UART	Break Character Generation	19.	The UART module will not generate back-to-back break characters.	X	X	X
PWM	Current Limit	20.	Cycle-by-cycle current limit operation does not work when the PWM module is configured for Center-Aligned mode.	X	X	X
PWM	Current Reset Mode	21.	Current Reset mode does not work when the current limit source (CLSRC) occurs during and persists past the assertive time interval of the PWM, and leading-edge blanking time is less than the PWM assertive time interval.	X	X	X
UART	IrDA® Encoder/ Decoder and 8-bit Operating Mode	22.	When the UART module is operating in 8-bit mode (PDSEL = 0x) and using the IrDA encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.	X	X	X
UART	UxE Interrupt	23.	The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.	X	X	X
I^2C	10-bit Addressing Mode	24.	When the I^2C module is configured as a 10-bit slave with an address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02.	X	X	X
I^2C	10-bit Addressing Mode	25.	The 10-bit slave does not set the RBF flag or load the I2CxRCV register, on address match if the Least Significant bits (LSbs) of the address are the same as the 7-bit reserved addresses.	X	X	X
PSV Operations	Addressing Modes	26.	An address error trap occurs in certain addressing modes when accessing the first four bytes of any PSV page.	X	X	X
Comparator	Sleep Mode	27.	The Comparator fails to wake the CPU from Sleep mode when the internal voltage reference is used.	X	X	X
PWM	Independent Time Base	28.	When updating the frequency on the fly, Push-Pull PWM outputs may not be synchronized with other PWM output modes.	X	X	X
Analog Comparator	Internal Bandgap Reference Voltage	29.	The Internal Bandgap Reference Voltage (INTREF) for the Analog Comparator does not meet the stated accuracy specifications.	X	X	X
Auxiliary PLL	Input Frequency	30.	For extended temperature devices, the Auxiliary PLL input frequency does not meet the published specification range.	X	X	X
ADC	Current Consumption in Sleep Mode	31.	If the ADC module is in an enabled state when the device enters Sleep Mode, the power-down current (IPD) of the device may exceed the device data sheet specifications.	X	X	X
High Speed PWM	PWM Module Enable	32.	A glitch may be observed on the PWM pins when the PWM module is enabled after assignment of pin ownership to the PWM module.	X	X	X
Reserved	—	33.	—	—		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A2	A3	A4
PWM	Duty Cycle Updates	34.	When the PWM duty cycle update coincides with the PWM period rollover, the PWM output may be corrupted for one PWM period.	X	X	X
JTAG	Active Pull-up	35.	In JTAG mode, the TMS pin will not have an active pull-up as required by the JTAG specification.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: PWM

Reading LEBCONx registers, as well as writing individual bits and bytes within these registers does not work.

Work around

Use a Word write operation to modify LEBCONx registers. For example, to set the PHR bit within the LEBCON1 register, use the following C code:

```
LEBCON1 = 0x8000
```

There is no work around for reading LEBCONx registers.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

2. Module: PWM

If PWM Immediate Update mode is selected (IUE = 1), and the PWM duty cycle is provided via the Master Duty Cycle (MDC) register (MDCS = 1 mode), the updates to the MDC register are synchronized to the PWM time base instead of an immediate update (duty cycle will be updated on the next PWM period).

Work arounds

Work around 1:

Use the Enable Immediate Period Update mode (EIPU = 1) in conjunction with PWM Immediate Update mode (IUE = 1). This will update the period and duty cycle on an immediate basis.

Work around 2:

Use individual duty cycle registers (PDCx) and PWM Immediate Update mode (IUE = 1) to update individual duty cycle registers on an immediate basis.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

3. Module: PWM

If PWM fault interrupts are disabled (FLTIEN = 0 or CLIEN = 0), then associated Status bits (FLTSTAT and CLSTAT) will not function.

Work around

Enable PWM fault interrupts (FLTIEN = 1, CLIEN = 1).

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

4. Module: PWM

The PWM output will exhibit jitter under the following conditions:

When the PWM clock divider has the value of 1, 5 or 6 (PTCON2<PCLKDIV> = 0b001, 0b101 or 0b110), and the three Least Significant bits of the PWM Period Register (PTPER or PHASEx), Duty Cycle Register (MDC or PDCx) or Phase Register (PHASEx) are non-zero.

Work around

Use PWM clock dividers other than 1, 5 or 6.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

5. Module: PWM

When PWM module is operated in Complementary, Redundant and Push-pull output modes, with Independent Time Base (ITB = 1) and Independent Fault mode (IFLTMOD = 1) enabled, the PWMxH and PWMxL outputs should be affected by the Fault and Current Limit events as follows:

- PWMxH is affected by Current-Limit source (FCLCON<CLSRC>) and the Current-Limit should be reset at the end of the primary local time base.
- PWMxL is affected by Fault source (FCLCON<FLTSRC>) and the Fault should be reset at the end of the primary local time base.

On silicon revisions affected by this erratum, the Current-Limit event works correctly for the PWMxH pin. However, the Fault event is reset by the secondary local time base although it is not used to generate the time base value. As a result, the fault event on PWMxL pin may not work as expected. This erratum only applies to the cycle-by-cycle Fault mode (FLTMOD = 0b01).

Work around

If PWM is in Complementary, Redundant or Push-Pull mode and (ITB = 1), set SPHASEx to have the same value as PHASEx. This will ensure that the Fault event on the PWMxL pin is reset at the start of the new PWM period for cycle-by-cycle independent fault operation.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

6. Module: PWM

The independent time base PWM outputs may not be synchronized with the Master time base PWM outputs when both modes are used simultaneously.

Work around

To synchronize the Independent PWM outputs with the Master time base PWM outputs, disable the Immediate Updates bit (IUE = 0), ensure that the three Least Significant bits of the period are zero, and that the duty cycle is between 8 ns and the period minus 0x8.

This work around will not work if the frequency of the PWM module is being updated on the fly.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

7. Module: PWM

In PWM Latched Fault mode, the PWM outputs may be latched on both the rising as well as the falling edge of the Fault signal, regardless of the fault input polarity selection (set with the FCLCONx<FLTPOL> bit setting).

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

8. Module: PWM

A bit write to the CLMOD bit (bit 8) in the FCLCONx register or consecutive writes to the lower byte and higher byte of the FCLCONx register, causes all other bits of the high byte to be loaded with zeros.

Work around

Use Word writes for the FCLCONx register instead of bit or byte writes.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

9. Module: PWM

The PWM module fails to wake the CPU from Sleep mode on a PWM fault event.

Work around

Use the external interrupt pins to wake the CPU from Sleep mode.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

10. Module: Comparator

If the slew rate of the Comparator input signal is lower than 198 mV/µs, the Comparator module generates erroneous triggers/interrupts.

Work around

The Slew rate of Comparator input signal must be higher than 198 mV/µs to avoid multiple triggers/ interrupts.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

11. Module: ADC

Selecting the primary FRC (FVCO) as a clock source for the ADC module by setting the SLOWCLK bit (ADCON<12>) to the default setting of '0', does not work.

Work around

Always set the SLOWCLK bit (ADCON<12>) to '1', which selects the Auxiliary Clock (ACLK) as a clock source for the ADC. Use the Auxiliary Clock Configuration registers to select the primary FRC (FVCO) as a source (if desired) or other clock sources as inputs. See **Section 8.0 "Oscillator Configuration"** of the device data sheet (DS70318) for more information.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

12. Module: Auxiliary Clock

When the PWMMD bit in the PMD1 register is set, the Auxiliary Clock to both the ADC and PWM modules is disabled.

Work around

To disable the Auxiliary clock for the PWM module but not for the ADC module, set the individual PWM generator PMD bits in the PMD6 register.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

13. Module: Comparator

The comparator interrupt should be generated on a rising edge of the comparator output. When using the inverted polarity setting for the analog comparator (CMPCONx<CMPPOL> = 1), the interrupt should be generated when the analog voltage at the comparator input falls below the programmable threshold determined by the CMPDAC register setting. However, with this setting the interrupts may be generated regardless of the state of the comparator.

Work around

When using comparator interrupts, configure the external circuit to use the non-inverted polarity comparator setting (CMPCONx<CMPPOL> = 0).

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

14. Module: UART

When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

This issue does not affect the other UART configurations.

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

15. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = 11), the 16x baud clock signal on the BCLK pin is present only when the module is transmitting. The pin is idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

16. Module: I²C™

If there are two I²C devices on the bus, one of them is acting as the Master receiver and the other as the Slave transmitter. If both devices are configured for 10-bit addressing mode, and have the same value in the A10 and A9 bits of their addresses, then when the Slave select address is sent from the Master, both the Master and Slave acknowledge it. When the Master sends out the read operation, both the Master and the Slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

Work around

In all I²C devices, the addresses as well as bits A10 and A9 should be different.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

17. Module: PWM

When the primary or secondary PWMx generator is selected as a trigger source for ADC convert pairs 3, 4, 5 or 6 and the PWM module is running at the maximum speed, the PWM module may fail to trigger a conversion on these ADC pairs.

Work arounds

Work around 1:

Configure the PWM module to trigger the ADC module per the following steps (see Example 1 for the code used in this work around):

1. Enable the dual trigger mode bit (DTM) in the TRGCONx register.
2. Configure the TRIGx register to the desired trigger point.
3. Configure the STRIGx register to TRIGx + 0x8.
4. Select the PWMx primary trigger as the ADC trigger source for conversion.

If the PWM channel is configured for independent output mode and both channels are operating on the same time base, the phase difference between the two channels must be considered when setting the STRIGx register. This work around will not work for True Independent Time Base mode.

With this work around, the PWMx secondary trigger should not be selected as the trigger source for the ADC convert pair.

Work around 2:

Configure the PWM Input Clock Prescaler bits (PCLKDIV) for divide by 2 or higher.

Work around 3:

Utilize other available trigger sources, such as software or timer triggers, to initiate conversion on the affected ADC convert pairs.

Affected Silicon Revisions

A2	A3	A4					
X							

EXAMPLE 1: USING DUAL TRIGGER MODE

```
TRGCON1bits.DTM = 1;        /* Dual trigger mode (DTM) and STRIG used in combination to generate */
                            /* ADCPx triggers */
TRIG1 = 1224;               /* Configure desired trigger */
STRIG1 = 1232;              /* STRIG1 should be configured for TRIG1 + 8 */
ADCPC2bits.TRGSRC5 = 0x4;  /* PWM1 primary trigger selected as ADC trigger source for ADCP5*/
```

18. Module: PGEC3/PGED3 Programming Pins

When using the PGEC3/PGED3 pins for device programming, the programming time may be slower as compared to other available PGECx/PGEDx pin pairs, because the Enhanced ICSP™ programming algorithm cannot be executed on this pin pair.

Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for additional information on this limitation.

Work around

Use alternate PGECx/PGEDx programming pin pairs.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

19. Module: UART

The UART module will not generate consecutive break characters. Trying to perform a back-to-back break character transmission will cause the UART module to transmit the dummy character used to generate the first break character instead of transmitting the second break character. Break characters are generated correctly if they are followed by non-break character transmission.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

20. Module: PWM

Cycle-by-cycle current limit operation does not work when the PWM module is configured for Center-Aligned mode.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

21. Module: PWM

During normal operation, if Leading-Edge Blanking (LEB) is triggered to start counting at a rising edge of PWM and the PWM module has a blanking time period less than the PWM assertive time (TON time), and the current limit event occurs during the TON period and is still pending after the TON period is over, the current limit event should be ignored during TON time, but should be recognized after the TON time is over.

However, the device fails to recognize the current limit event after Ton time is over, when previously described conditions exist.

Work around

Initialize the LEBCONx register as shown below, which specifies the LEB function for the (CLSRC) input to be triggered on the falling (trailing) edge of PWM, and set the LEB delay to a minimum value of 8 ns:

- PHF bit is set
- CLLEBEN bit is set
- LEB<9:3> bits are set to a minimum value of '1'

If the user application needs LEB to be triggered at a falling edge, make sure that the LEB delay is set for more than the TON time.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

22. Module: UART

When the UART is operating in 8-bit mode (PDSEL = 0x) and using the IrDA encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

23. Module: UART

The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

24. Module: I²C

When the I²C module is configured as a 10-bit slave with and address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02; however, the module acknowledges both address bytes.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

25. Module: I²C

In 10-bit Addressing mode, some address matches do not set the RBF flag or load the receive register I2CxRCV, if the lower address byte matches the reserved addresses. In particular, these include all addresses with the form XX0000XXXX and XX1111XXXX, with the following exceptions:

- 001111000X
- 011111001X
- 101111010X
- 111111011X

Work around

Ensure that the lower address byte in 10-bit Addressing mode does not match any 7-bit reserved addresses.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

26. Module: PSV Operations

An address error trap occurs in certain addressing modes when accessing the first four bytes of an PSV page. This only occurs when using the following addressing modes:

- MOV.D
- Register Indirect Addressing (word or byte mode) with pre/post-decrement

Work around

Do not perform PSV accesses to any of the first four bytes using the above addressing modes. For applications using the C language, MPLAB C30 version 3.11 or higher, provides the following command-line switch that implements a work around for the erratum.

`-merrata=psv_trap`

Refer to the `readme.txt` file in the MPLAB C30 v3.11 tool suite for further details.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

27. Module: Comparator

The Comparator fails to wake the CPU from Sleep mode when the internal voltage reference is used (i.e., EXTREF bit is set to '0').

Work around

Use the external reference source by setting the EXTREF bit to '1'.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

28. Module: PWM

When multiple PWM channels are operating in Independent Time Base mode (ITB = 1) and the frequency is being updated on the fly, PWM channels configured for Push-Pull mode may not remain synchronized with other PWM output modes.

Work around

When multiple PWM channels are operating in Independent Time Base mode, immediate updates to the PWM module (IUE = 1) must be enabled for PWM channels to remain synchronized.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

29. Module: Analog Comparator

The Internal Bandgap Reference Voltage (INTREF) for the Analog Comparator provides the reference to the Analog Comparator if the EXTREF bit (CMPCONx<5>) = 0 and the RANGE bit (CMPCONx<0>) = 0.

The data sheet states that the INTREF voltage should be 1.2V nominal and within +/- 1%. However, the Internal Bandgap Reference Voltage does not meet the accuracy specification as stated in the data sheet. The actual range of voltages for the internal bandgap is 1.25V to 1.41V.

Work arounds

To avoid this issue, implement one of the following two work arounds, depending on the application requirements.

Work around 1:

Use an external voltage reference for the Analog Comparator by setting the EXTREF bit (CMPCONx<5>) = 1 and providing an external reference to the EXTREF pin.

Work around 2:

Use the high-range setting for the internal reference by setting the EXTREF bit (CMPCONx<5>) = 0 and the RANGE bit (CMPCONx<0>) = 1. This setting uses AVDD/2 as the comparator reference voltage.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

30. Module: Auxiliary PLL

For extended temperature devices (designated with the -E suffix in the device part number) with the date code of 09XX, the Auxiliary PLL input frequency does not meet the published specification range at operating temperatures above 85ºC.

Work around

Use the internal FRC oscillator as the input to the Auxiliary PLL, or use the external oscillator with a frequency of 7.37 MHz.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

31. Module: ADC

If the ADC module is in an enabled state when the device enters Sleep mode as a result of executing a PWRSAV #0 instruction, the device power-down current (IPD) may exceed the specifications listed in the device data sheet. This may happen even if the ADC module is disabled by clearing the ADON bit prior to entering Sleep mode.

Work arounds

Work around 1:

In order to remain within the IPD specifications listed in the device data sheet, the user software must completely disable the ADC module by setting the ADC Module Disable bit in the corresponding Peripheral Module Disable register (PMDx), prior to executing a PWRSAV #0 instruction.

Note: The ADC module must be reinitialized by the user application before resuming ADC operation.

Work around 2:

If the ADC module was previously initialized and enabled, before entering Sleep, execute the lines of code provided in Example 2.

Note: Unlike **Work around 1**, the user application does not need to reinitialize the ADC module; however, it is necessary to re-enable the ADC module by setting the ADON bit after waking from Sleep.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

EXAMPLE 2:

```
AD1CON1bits.ADON = 0;              //Disable the ADC module
__asm__ volatile ("REPEAT #50");   //Wait 50 Tcy
__asm__ volatile ("NOP");          //Repeat NOP 51 times
Sleep();                           // Execute PWRSAV #0 and go to Sleep
```

32. Module: High Speed PWM

The PENH and PENL bits in the IOCONx register are used to assign ownership of the pins to either the PWM module or the GPIO module. The correct procedure to configure the PWM module is to first assign pin ownership to the PWM module and then enabling it using the PTEN bit in the PTCON register.

If the PWM module is enabled using the above sequence, then a glitch may be observed on the PWM pins before actual switching of the PWM outputs begins. This glitch may cause momentary turn ON of power MOSFETs that are driven by the PWM pins and may cause damage to the application hardware.

Work around

Follow the given sequence to avoid any glitches from appearing on the PWM outputs at the time of enabling.

1. Configure the respective PWM pins to digital inputs using the TRISx registers. This step will put the PWM pins in a high-impedance state. The PWM outputs must be maintained in a safe state by using pull-up or pull-down resistors.
2. Assign pin ownership to the GPIO module by configuring IOCONx<PENH> = 0 and IOCONx<PENL> = 0.
3. Specify the PWM override state to the desired safe state for the PWM pins using the OVRDAT<1:0> bit-field in the IOCONx register.
4. Override the PWM outputs by setting IOCONx<OVRENH> = 1 and IOCONx<OVRENL> = 1.
5. Enable the PWM module by setting PTCON<PTEN> = 1.
6. Remove the PWM Overrides by making IOCONx<OVRENH> = 0 and IOCONx<OVRENL> = 0.
7. Assign pin ownership to the PWM module by setting IOCONx<PENH> = 1 and IOCONx<PENL> = 1.

The code Example 3 illustrates the use of this work around.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

EXAMPLE 3: CONFIGURE PWM MODULE TO PREVENT GLITCHES ON PWM1H AND PWM1L PINS AT THE TIME OF ENABLING

```
TRISAbits.TRISA4 = 1;    // Configure PWM1H/RA4 as digital input
                         // Ensure output is in safe state using pull-up or
                         // pull-down resistors
TRISAbits.TRISA3 = 1;    // Configure PWM1L/RA3 as digital input
                         // Ensure output is in safe state using pull-up or
                         // pull-down resistors

IOCON1bits.PENH = 0;     // Assign pin ownership of PWM1H/RA4 to GPIO module
IOCON1bits.PENL = 0;     // Assign pin ownership of PWM1L/RA3 to GPIO module

IOCON1bits.OVRDAT = 0;   // Configure override state of the PWM outputs to
                         // desired safe state.

IOCON1bits.OVRENH = 1;   // Override PWM1H output
IOCON1bits.OVRENL = 1;   // Override PWM1L output

PTCONbits.PTEN = 1;      // Enable PWM module

IOCON1bits.OVRENH = 0;   // Remove override for PWM1H output
IOCON1bits.OVRENL = 0;   // Remove override for PWM1L output

IOCON1bits.PENH = 1;     // Assign pin ownership of PWM1H/RA4 to PWM module
IOCON1bits.PENL = 1;     // Assign pin ownership of PWM1L/RA3 to PWM module
```

33. Module: Reserved

The issue in the previous version of the document has been removed.

34. Module: PWM

The High-Speed PWM provides a feature to update the PWM duty cycle at any time during the PWM period. The new duty cycle should take effect:

- On the next PWM period when immediate duty cycle updates are disabled (PWMCONx<IUE> = 0).
- On the same PWM period when immediate duty cycle updates are enabled (PWMCONx<IUE> = 1).

However, when the immediate duty cycle updates are disabled and the duty cycle update coincides with a PWM period roll-over, the PWM output may be corrupted and exhibit a 100% duty cycle for one PWM period. The new duty cycle value will take effect on the next PWM period.

Work around

Enable immediate duty cycle updates by configuring PWMCONx<IUE> = 1.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

35. Module: JTAG

In JTAG mode, the TMS pin will not have an active pull-up as required by the JTAG specification. Instead, the pull-up function will be enabled on the TCK pin.

Note: This issue is only present in the dsPIC33FJ06GS101 device.

Work around

An external pull-up resistor can be connected to the TMS pin to ensure that the signal does not enter a tri-state condition when in JTAG mode.

There is no work around for the wrongly enabled pull-up function on the TCK pin.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70318**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Idle Current (IIDLE)

The typical values for Table 24-6 were stated incorrectly in the data sheet. The correct values are shown in bold type in the following table.

TABLE 24-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended			
Param No.	Typical(1)	Max	Units	Conditions		
Idle Current (IIDLE): Core Off Clock On Base Current(2)						
DC40d	**48**	—	mA	-40°C	3.3V	10 MIPS(3)
DC40a	**48**	—	mA	+25°C		
DC40b	**48**	—	mA	+85°C		
DC40c	**48**	—	mA	+125°C		
DC41d	**60**	—	mA	-40°C	3.3V	16 MIPS(3)
DC41a	**60**	—	mA	+25°C		
DC41b	**60**	—	mA	+85°C		
DC41c	**60**	—	mA	+125°C		
DC42d	**68**	—	mA	-40°C	3.3V	20 MIPS(3)
DC42a	**68**	—	mA	+25°C		
DC42b	**68**	—	mA	+85°C		
DC42c	**68**	—	mA	+125°C		
DC43d	**77**	—	mA	-40°C	3.3V	30 MIPS(3)
DC43a	**77**	—	mA	+25°C		
DC43b	**77**	—	mA	+85°C		
DC43c	**77**	—	mA	+125°C		
DC44d	**86**	—	mA	-40°C	3.3V	40 MIPS
DC44a	**86**	—	mA	+25°C		
DC44b	**86**	—	mA	+85°C		
DC44c	**86**	—	mA	+125°C		

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: Base IIDLE current is measured with core Off, clock On and all modules turned off. Peripheral module Disable SFR registers are zeroed. All I/O pins are configured as inputs and pulled to VSS.

3: These parameters are characterized but not tested in manufacturing.

2. Module: Auxiliary PLL

The Auxiliary PLL Clock Timing Specifications for parameters OS56 (FHPOUT) and OS57 (FHPIN) were stated incorrectly in Table 24-18 of the data sheet. The correct values are shown in bold type in Table 2.

TABLE 24-18: AUXILIARY PLL CLOCK TIMING SPECIFICATIONS (VDD = 3.0V TO 3.6V)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
OS56	FHPOUT	0n-Chip 16x PLL VCO Frequency	**112**	**118**	**120**	MHz	—
OS57	FHPIN	On-Chip 16x PLL Phase Detector Input Frequency	**7.0**	**7.37**	**7.5**	MHz	—

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested in manufacturing.

3. Module: DC Characteristics: I/O Pin Input Specifications

The maximum value for parameter DI19 (VIL specifications for SDAx and SCLx pins) was stated incorrectly in Table 24-9 of the current device data sheet. Also, parameters DI28 and DI29 (VIH specifications for SDAx and SCLx pins) were not stated. The correct values are shown in bold type in Table 3.

TABLE 3: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
	VIL	Input Low Voltage					
DI18		**SDAx, SCLx**	VSS	—	0.3 VDD	V	SMBus disabled
DI19		**SDAx, SCLx**	VSS	—	**0.8**	V	SMBus enabled
	VIH	Input High Voltage					
DI28		**SDAx, SCLx**	**0.7 VDD**	**—**	**5.5**	**V**	**SMBus disabled**
DI29		**SDAx, SCLx**	**2.1**	**—**	**5.5**	**V**	**SMBus enabled**

APPENDIX A: REVISION HISTORY

Rev A Document (3/2009)

Initial release of this document; issued for revision A2 silicon.

Includes silicon issues 1-9 (PWM), 10 (Comparator), 11 (ADC), 12 (Auxiliary Clock), 13 (Comparator), 14-15 (UART) and 16 (I^2C™).

Rev B Document (4/2009)

Added silicon issue 17 (PWM).

Rev C Document (5/2009)

Updated silicon issue 17 (PWM) to clarify which ADC pairs are involved.

Rev D Document (5/2009)

Revised to include revision A3 silicon information. Added silicon issues 18 (PGEC3/PGED3 Programming Pins), 19 (UART) and 20-21 (PWM).

Added data sheet clarification 1 (Idle Current (I_{IDLE})).

Rev E Document (8/2009)

Added silicon issues 22-23 (UART), 24-25 (I^2C), 26 (PSV Operations), 27 (Comparator) and 28 (PWM).

Rev F Document (1/2010)

Added silicon issues 29 (Analog Comparator) and 30 (Auxiliary PLL).

Added data sheet clarification 2 (Auxiliary PLL).

Rev G Document (6/2010)

Added silicon issues 31 (ADC) and 32 (High Speed PWM) and data sheet clarification 3 (DC Characteristics: I/O Pin Input Specifications).

Rev H Document (10/2010)

Added revision A4 silicon information to all tables.

Updated the work arounds for silicon issue 31 (ADC).

Removed silicon issue 33 (PWM) and marked its location as reserved.

Added silicon issues 34 (PWM) and 35 (JTAG).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

ISBN: 978-1-60932-597-8

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung
Tel: 886-7-213-7830
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

08/04/10