PIC16(L)F1946/1947 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1946/1947 family devices that you have received conform functionally to the current Device Data Sheet (DS41414**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1946/1947 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1946/ 1947 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A2	A3	A4
PIC16F1946	`10 0101 000x xxxx`	02h	03h	04h
PIC16LF1946	`10 0101 100x xxxx`	02h	03h	04h
PIC16F1947	`10 0101 001x xxxx`	02h	03h	04h
PIC16LF1947	`10 0101 101x xxxx`	02h	03h	04h

Note 1: The Device ID is located in the last configuration memory space.

2: Refer to the *"PIC16F193X/LF193X and PIC16F194X/LF194X Memory Programming Specification"* (DS41397) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]		
				A2	A3	A4
Oscillator	HS Oscillator	1.1	HS Oscillator min. VDD	X		
ADC	Analog-to-Digital Converter	2.1	ADC conversion does not complete	X		
Brown-out Reset (BOR)	Brown-out Reset	3.1	BOR set without going below BOR level	X	X	X
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	4.1	PWM 0% duty cycle direction change	X		
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	4.2	PWM 0% duty cycle port steering	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Oscillator

1.1 HS Oscillator

The HS oscillator requires a minimum voltage of 3.0 volts (at 65°C or less) to operate at 20 MHz.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X							

2. Module: ADC

2.1 Analog-to-Digital Converter (ADC)

Under certain device operating conditions, the ADC conversion may not complete properly. When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the ADGO/DONE bit does not get cleared and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

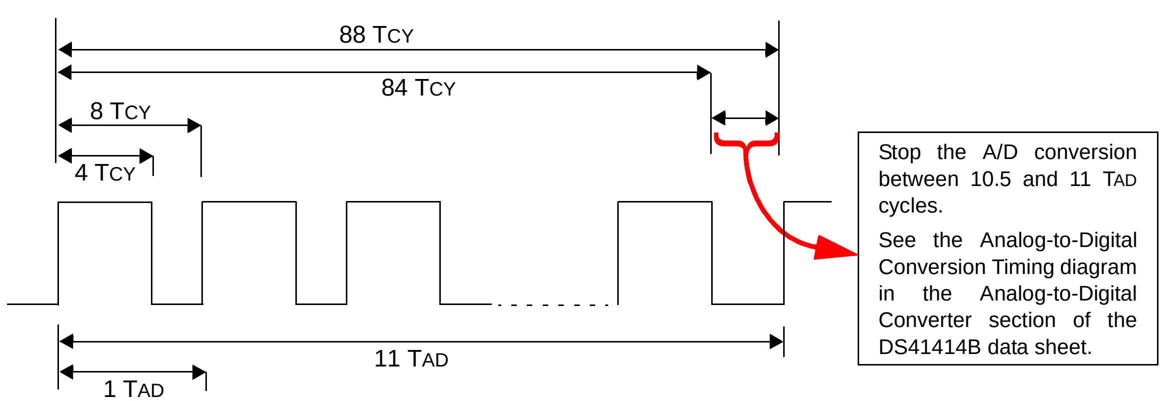
Work around

Method 1: Select the dedicated RC oscillator as the ADC conversion clock source, and perform all conversions with the device in Sleep.

Method 2: Provide a fixed delay in software to stop the A-to-D conversion manually, after all 10 bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/DONE bit in software. The GO/DONE bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE

FOSC = 32 MHz
TCY = 4/32 MHz = 125 nsec
TAD = 1 µsec, ADCS = FOSC/32



See the ADC Clock Period (TAD) vs. Device Operating Frequencies table, in the Analog-to-Digital Converter section of the DS41414B data sheet.

In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of 8 TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

Note:	The exact delay time will depend on the choice of FOSC and the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 3 for the required delay counts for other configurations.

EXAMPLE 1: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF     ADCON0, ADGO    ; Start ADC conversion
                        ; Provide 86
                          instruction cycle
                          delay here
BCF     ADCON0, ADGO    ; Terminate the
                          conversion manually
MOVF    ADRESH, W       ; Read conversion
                          result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to Table 3.

TABLE 3: INSTRUCTION CYCLE DELAY COUNTS FOR OTHER FOSC AND TAD COMBINATIONS

FOSC	TAD	Instruction Cycle Delay Counts
32 MHz	FOSC/64	172
	FOSC/32	86
16 MHz	FOSC/64	172
	FOSC/32	86
	FOSC/16	43
8 MHz	FOSC/32	86
	FOSC/16	43

Affected Silicon Revisions

A2	A3	A4					
X							

3. Module: Brown-out Reset (BOR)

3.1 Brown-out Reset

If $\overline{MCLR}$ is used to wake the device, while the BOR is set to Sleep and the part is in Sleep, the BOR bit of the PCON register will be cleared without VDD dropping below the BOR level.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

4. Module: Enhanced Capture Compare PWM (ECCP)

4.1 Enhanced PWM

When the PWM is configured for Full-Bridge mode and the duty cycle is set to 0%, writing the PxM<1:0> bits to change the direction has no effect on PxA and PxC outputs.

Work around

Increase the duty cycle to a value greater than 0% before changing directions.

Affected Silicon Revisions

A2	A3	A4					
X							

4.2 Enhanced PWM

In PWM mode, when the duty cycle is set to 0% and the STRxSYNC bit is set, writing the STRxA, STRxB, STRxC and the STRxD bits to enable/ disable steering to port pins has no effect on the outputs.

Work around

Increase the duty cycle to a value greater than 0% before enabling/disabling steering to port pins.

Affected Silicon Revisions

A2	A3	A4					
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41414**B**):

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (4/2010)

Initial release of this document.

Rev B Document (9/2010)

Updated errata to new format; Added Silicon Revision A3.

Rev C Document (12/2010)

Updated errata to add Silicon Revision A4.

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