



# MICROCHIP

# PIC16F707/PIC16LF707

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## 40-Pin, 8-Bit Flash mTouch™ Microcontroller with 32 Capacitive Touch Channels

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### High-Performance RISC CPU:

- Only 35 Single-Word Instructions to learn:
  - All single-cycle instructions except branches
- Operating Speed:
  - DC – 20 MHz clock input
  - DC – 200 ns instruction cycle
- 8K x 14 Words of Flash Program Memory
- 363 Bytes of Data Memory (SRAM)
- Interrupt Capability
- 8-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes
- Processor Read Access to Program Memory
- Pinout Compatible to other 40-pin PIC16CXXX and PIC16FXXX Microcontrollers

### Special Microcontroller Features:

- Precision Internal Oscillator:
  - 16 MHz or 500 kHz operation
  - Factory calibrated to  $\pm 1\%$ , typical
  - Software selectable  $\div 1$ ,  $\div 2$ ,  $\div 4$  or  $\div 8$  divider
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - 3 crystal/resonator modes up to 20 MHz
  - 3 external clock modes up to 20 MHz
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-Up Timer (OST)
- Brown-out Reset (BOR):
  - Selectable between two trip points
  - Disabled in Sleep option
- Watchdog Timer (WDT)
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Multiplexed Master Clear with Pull-up/Input Pin
- Industrial and Extended Temperature Range
- High-Endurance Flash Cell:
  - 1,000 Write Flash Endurance (typical)
  - Flash Retention: >40 years
  - Power-Saving Sleep mode
- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF707)
  - 1.8V to 5.5V (PIC16F707)

### Analog Features:

- A/D Converter:
  - 8-bit resolution and up to 14 channels
  - Conversion available during Sleep
  - Selectable 1.024V/2.048V/4.096V voltage reference
- On-chip 3.2V Regulator (PIC16F707 device only)

### Extreme Low-Power Management PIC16LF707 with nanoWatt XLP:

- Sleep Mode: 20 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Timer1 Oscillator: 600 nA @ 1.8V, typical @ 32 kHz

### mTouch™ Features:

- Up to 32 channels
- Two Capacitive Sensing Modules:
  - Acquire 2 samples simultaneously
- Multiple Power Modes:
  - Operation during Sleep
  - Proximity sensing with ultra low  $\mu\text{A}$  current
- Adjustable waveform min. and max. for optimal noise performance
- 1.8V to 5.5V operation (3.6V max. for PIC16LF707)

### Peripheral Features:

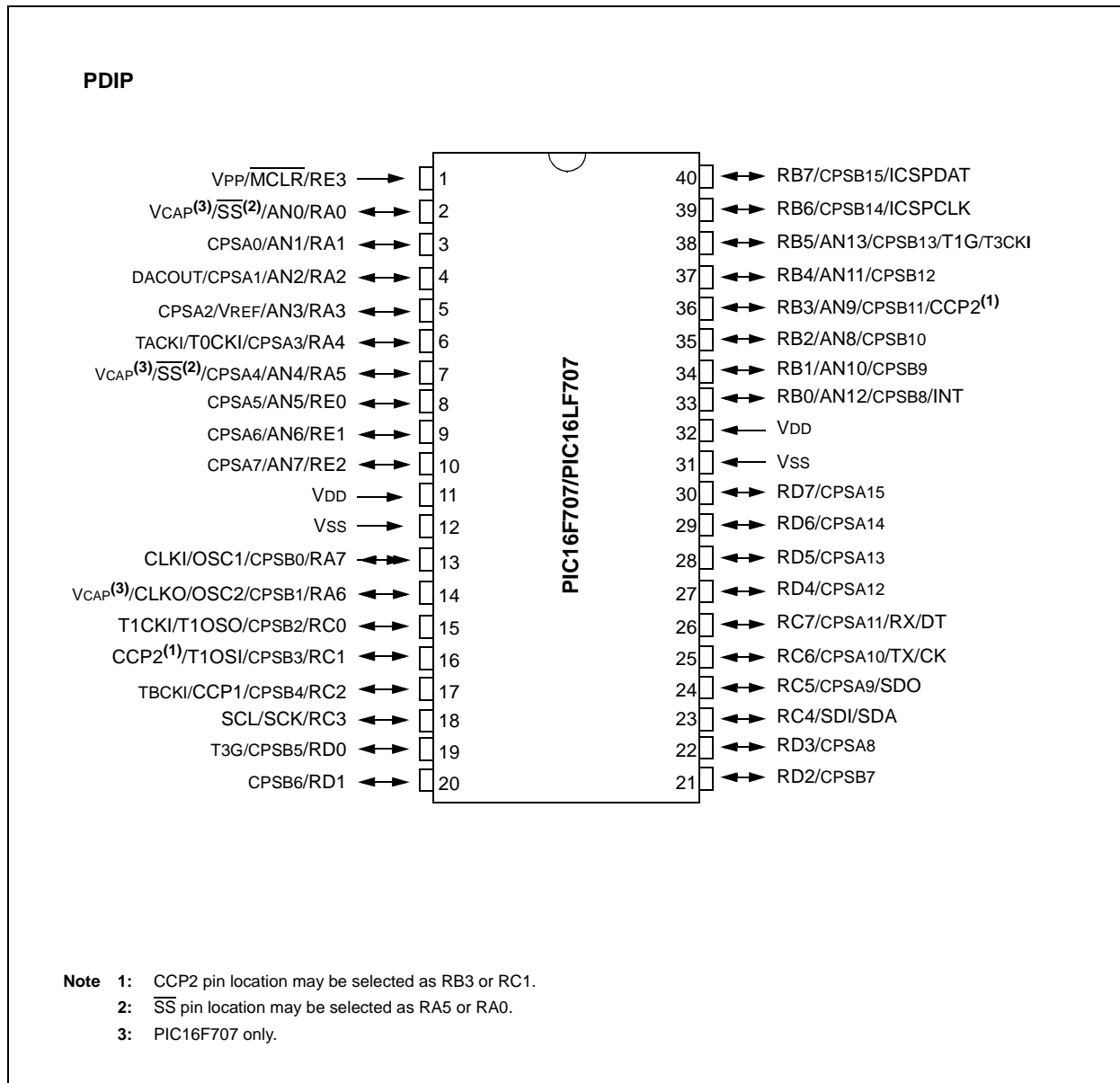
- Up to 35 I/O Pins and 1 Input-only Pin:
  - High current source/sink for direct LED drive
  - Interrupt-on-pin change
  - Individually programmable weak pull-ups
- Timer0/A/B: 8-Bit Timer/Counter with 8-Bit Prescaler
- Enhanced Timer1/3:
  - Dedicated low-power 32 kHz oscillator driver
  - 16-bit timer/counter with prescaler
  - External Gate Input mode with toggle and single shot modes
  - Interrupt-on-gate completion
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two Capture, Compare, PWM modules (CCP):
  - 16-bit Capture, max. resolution 12.5 ns
  - 16-bit Compare, max. resolution 200 ns
  - 10-bit PWM, max. frequency 20 kHz
- Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART)
- Synchronous Serial Port (SSP):
  - SPI (Master/Slave)
  - I<sup>2</sup>C™ (Slave) with Address Mask
- Voltage Reference module:
  - Fixed voltage reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - 5-bit rail-to-rail resistive DAC with positive reference selection

# PIC16F707/PIC16LF707

**TABLE 1: PIC16F707/PIC16LF707 FAMILY TYPES**

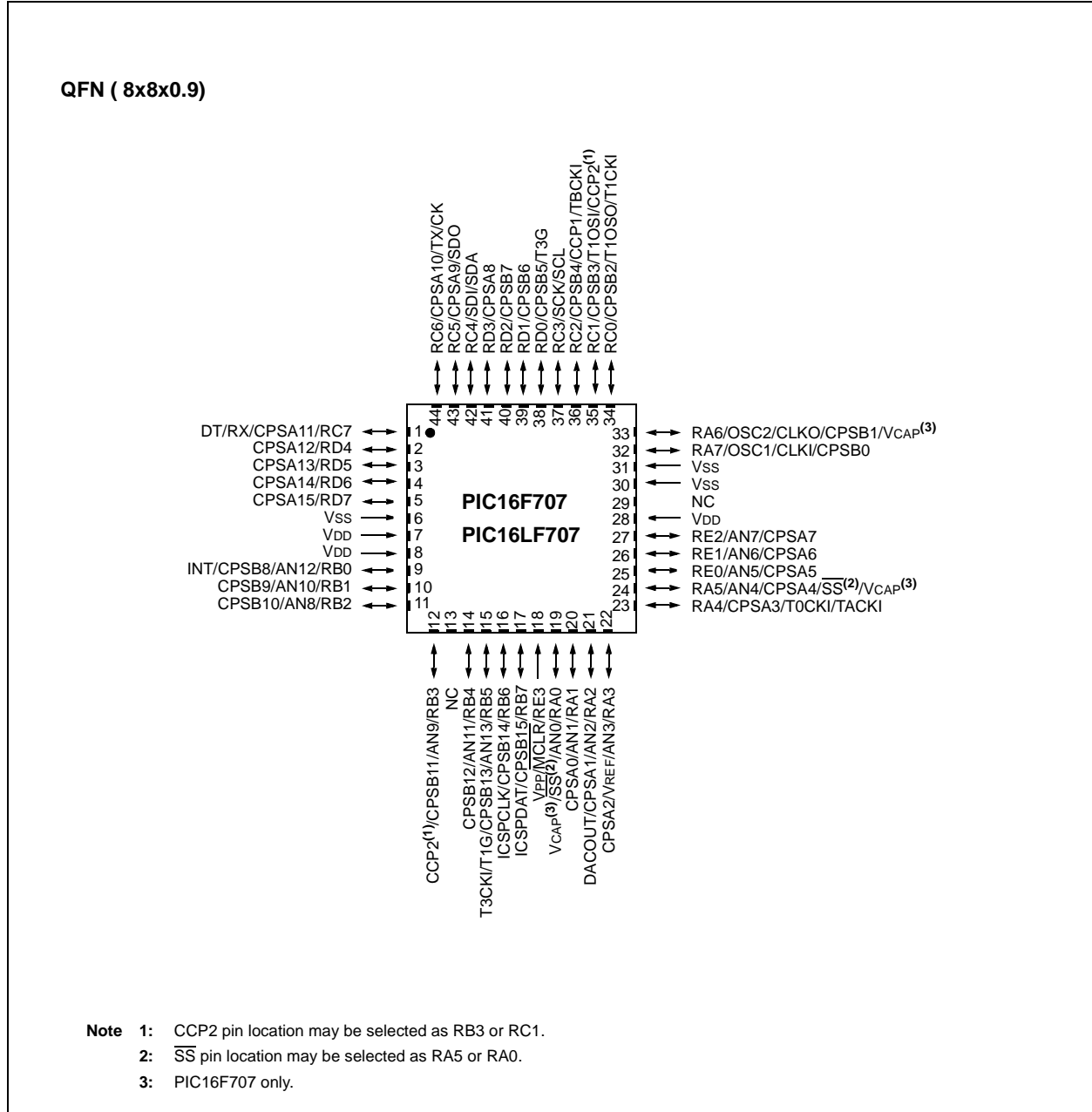
Device	Program Memory Flash (words)	SRAM (bytes)	I/Os	Capacitive Touch Channels	8-bit A/D (ch)	AUSART	CCP	Timers 8/16-bit
PIC16F707	8192	363	36	32	14	Yes	2	4/2
PIC16LF707	8192	363	36	32	14	Yes	2	4/2

**FIGURE 1: 40-PIN DIAGRAM FOR PIC16F707 AND PIC16LF707**



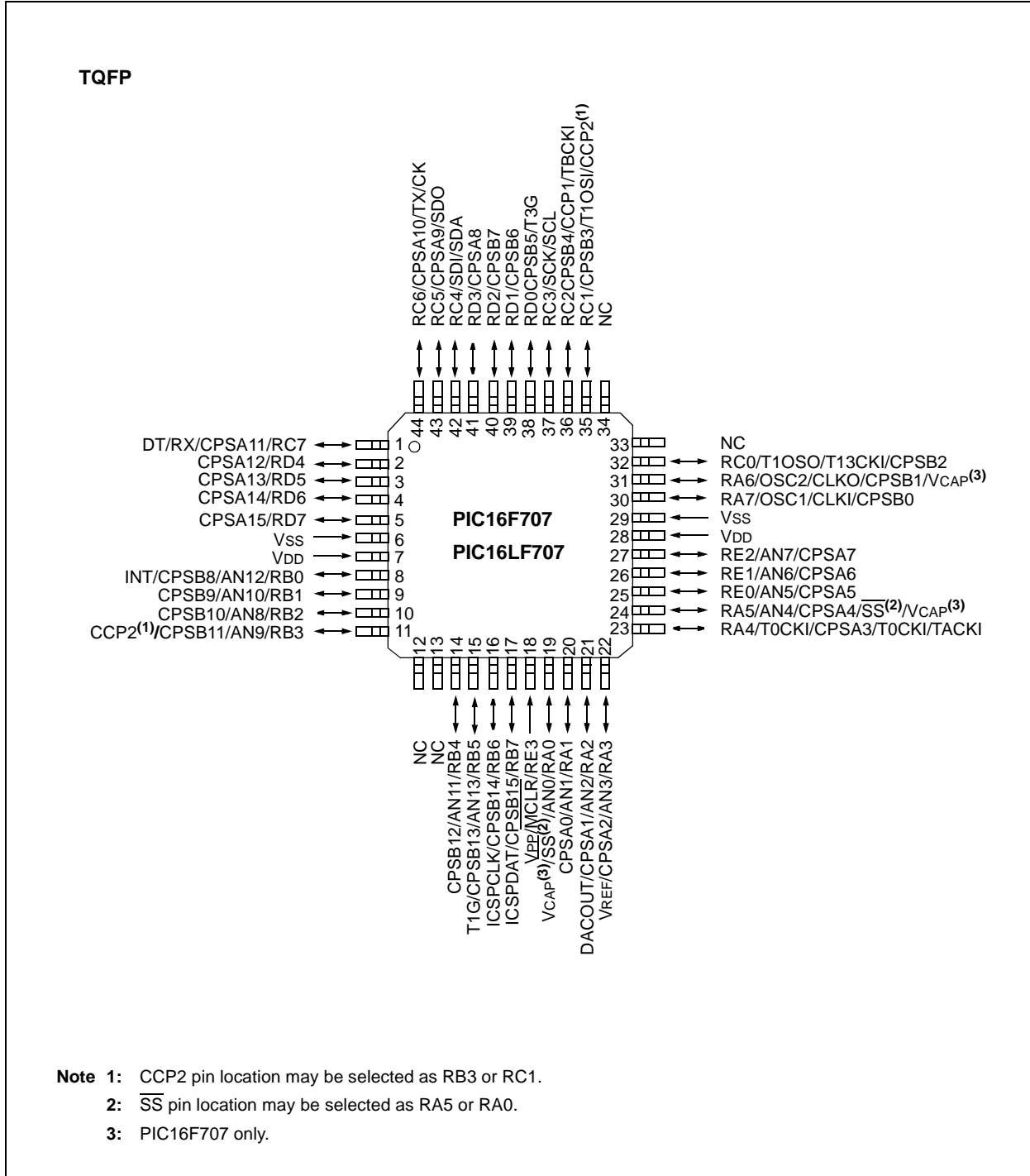
# PIC16F707/PIC16LF707

FIGURE 2: 44-PIN DIAGRAM FOR PIC16F707 AND PIC16LF707



# PIC16F707/PIC16LF707

FIGURE 3: 44-PIN DIAGRAM FOR PIC16F707 AND PIC16LF707



# PIC16F707/PIC16LF707

**TABLE 2: 40/44-PIN ALLOCATION TABLE FOR PIC16F707/PIC16LF707**

I/O	40-Pin PDIP	44-Pin TQFP	44-Pin QFN	ANSEL	A/D	DAC	Cap Sensor	Timers	CCP	AUSART	SSP	Interrupt	Pull-up	Basic
RA0	2	19	19	Y	AN0	—	—	—	—	—	SS <sup>(3)</sup>	—	—	VCAP <sup>(4)</sup>
RA1	3	20	20	Y	AN1	—	CPSA0	—	—	—	—	—	—	—
RA2	4	21	21	Y	AN2	DACOUT	CPSA1	—	—	—	—	—	—	—
RA3	5	22	22	Y	AN3/ VREF	VREF	CPSA2	—	—	—	—	—	—	—
RA4	6	23	23	Y	—	—	CPSA3	T0CKI/ TACKI	—	—	—	—	—	—
RA5	7	24	24	Y	AN4	—	CPSA4	—	—	—	SS <sup>(3)</sup>	—	—	VCAP <sup>(4)</sup>
RA6	14	31	33	Y	—	—	CPSB1	—	—	—	—	—	—	OSC2/ CLKO/ VCAP <sup>(4)</sup>
RA7	13	30	32	Y	—	—	CPSB0	—	—	—	—	—	—	OSC1/ CLKI
RB0	33	8	9	Y	AN12	—	CPSB8	—	—	—	—	IOC/INT	Y	—
RB1	34	9	10	Y	AN10	—	CPSB9	—	—	—	—	IOC	Y	—
RB2	35	10	11	Y	AN8	—	CPSB10	—	—	—	—	IOC	Y	—
RB3	36	11	12	Y	AN9	—	CPSB11	—	CCP2 <sup>(2)</sup>	—	—	IOC	Y	—
RB4	37	14	14	Y	AN11	—	CPSB12	—	—	—	—	IOC	Y	—
RB5	38	15	15	Y	AN13	—	CPSB13	T1G/ T3CKI	—	—	—	IOC	Y	—
RB6	39	16	16	Y	—	—	CPSB14	—	—	—	—	IOC	Y	ICSPCLK/ ICDCLK
RB7	40	17	17	Y	—	—	CPSB15	—	—	—	—	IOC	Y	ICSPDAT/ ICDDAT
RC0	15	32	34	Y	—	—	CPSB2	T1OSO/ T1CKI	—	—	—	—	—	—
RC1	16	35	35	Y	—	—	CPSB3	T1OSI	CCP2 <sup>(2)</sup>	—	—	—	—	—
RC2	17	36	36	Y	—	—	CPSB4	TBCKI	CCP1	—	—	—	—	—
RC3	18	37	37	—	—	—	—	—	—	—	SCK/SCL	—	—	—
RC4	23	42	42	—	—	—	—	—	—	—	SDI/SDA	—	—	—
RC5	24	43	43	Y	—	—	CPSA9	—	—	—	SDO	—	—	—
RC6	25	44	44	Y	—	—	CPSA10	—	—	TX/CK	—	—	—	—
RC7	26	1	1	Y	—	—	CPSA11	—	—	RX/DT	—	—	—	—
RD0	19	38	38	Y	—	—	CPSB5	T3G	—	—	—	—	—	—
RD1	20	39	39	Y	—	—	CPSB6	—	—	—	—	—	—	—
RD2	21	40	40	Y	—	—	CPSB7	—	—	—	—	—	—	—
RD3	22	41	41	Y	—	—	CPSA8	—	—	—	—	—	—	—
RD4	27	2	2	Y	—	—	CPSA12	—	—	—	—	—	—	—
RD5	28	3	3	Y	—	—	CPSA13	—	—	—	—	—	—	—
RD6	29	4	4	Y	—	—	CPSA14	—	—	—	—	—	—	—
RD7	30	5	5	Y	—	—	CPSA15	—	—	—	—	—	—	—
RE0	8	25	25	Y	AN5	—	CPSA5	—	—	—	—	—	—	—
RE1	9	26	26	Y	AN6	—	CPSA6	—	—	—	—	—	—	—
RE2	10	27	27	Y	AN7	—	CPSA7	—	—	—	—	—	—	—
RE3	1	18	18	—	—	—	—	—	—	—	—	—	Y <sup>(1)</sup>	MCLR/ VPP
VDD	11, 32	7, 28	7, 8, 28	—	—	—	—	—	—	—	—	—	—	VDD
VSS	12, 31	6, 29	6, 30, 31	—	—	—	—	—	—	—	—	—	—	VSS

- Note**
- 1: Pull-up activated only with external MCLR configuration.
  - 2: RC1 is the default pin location for CCP2. RB3 may be selected by changing the CCP2SEL bit in the APFCON register.
  - 3: RA5 is the default pin location for SS. RA0 may be selected by changing the SSSEL bit in the APFCON register.
  - 4: PIC16F707 only. VCAP functionality is selectable by the VCAPEN bits in Configuration Word 2.

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NOTES:

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