# PIC18F26K20/46K20 Rev. A4 Through A5 Silicon/Data Sheet Errata

The PIC18F26K20/46K20 parts you have received conform functionally to the Device Data Sheet (DS41303**C**) and the Programming Specification (DS41297**D**), except for the anomalies described below.

All problems listed here will be addressed in future revisions of the PIC18F26K20/46K20 silicon.

### 1. Module: ECCP

Changing the CCP1M<3:0> bits of CCP1CON may cause the CCPR1H and CCPR1L registers to capture the value of Timer1.

**Work around**

Halt Timer1 before changing ECCP mode. Reload Timer1 with desired value after ECCP is setup and before Timer1 is restarted.

### 2. Module: ECCP

Changing direction in Full-Bridge mode does not insert dead time between changing the active drivers in common legs of the bridge.

**Work around**

None.

### 3. Module: MSSP I²C™

Slew rate is slower than $I^2C$ specifications when the SLRCON<2> bit is set.

**Work around**

Clear SLRCON<2> bit when using the $I^2C$ peripheral.

### 4. Module: ADC

Offset error is 3 LSb typical, 7 LSb maximum, including an acquisition time dependent component (~2 LSb).

**Work around**

The time dependent error is insignificant when the time between conversions is less than 100 ms. When the time since the previous conversion is greater than 100 ms then take two ADC conversions and discard the first.

### 5. Module: MSSP I²C

If a new address byte is received while the BF flag is set, the SSPOV bit is set and an ACK is not generated, both of which are proper operation. If only the SSPOV bit is set (BF flag was cleared) and a matching address is clocked in, that received byte will be loaded into the SSPBUF register and an ACK will be generated, both of which are improper operation.

**Work around**

None.

### 6. Module: MSSP I²C

In Master $I^2C$ mode, when a slave device releases the clock after holding it low (clock stretching), the pulse width of the first high clock cycle may be shorter than half the clock period.

**Work around**

None.

### 7. Module: MSSP I²C

In Master $I^2C$ mode, baud rates obtained by setting SSPADD to a value less than 0x03 will cause unexpected operation.

**Work around**

Ensure SSPADD is set to a value greater than or equal to 0x04.

### 8. Module: MSSP SPI

When the SPI clock is configured for Timer2 output/2 (SSPCON1<3:0> = `0011`), the first SPI high time may be short.

**Work around**

Option 1: Ensure TMR2 value rolls over to zero immediately before writing to SSPBUF.

Option 2: Turn Timer2 off and clear TMR2 before writing SSPBUF. Enable TMR2 after SSPBUF is written.

### 9. Module: MSSP SPI

In SPI Master mode, when the CKE bit is cleared and the SMP bit is set, the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

**Work around**

None.

### 10. Module: MSSP SPI

In SPI Master mode, when CKE bit is set, the SSPBUF will reload the SSPSR output shift register on every high-to-low transition of the $\overline{SS}$ pin.

**Work around**

Avoid using the $\overline{SS}$ pin when the CKE bit is set and the MSSP is configured for SPI Master mode.

### 11. Module: MSSP SPI

When SPI is enabled in Master mode with CKE = 1 and CKP = 0, a 1/FOSC wide pulse will occur on the SCK pin.

**Work around**

Configure the SCK pin as an input until after the MSSP is setup.

### 12. Module: EUSART

In Synchronous Master mode, when the SPBRG is set to an odd number, the duty cycle of the CK output will be skewed by one baud clock count.

**Work around**

High values of SPBRG will minimize the effect of this anomaly.

### 13. Module: EUSART

In Synchronous Master mode, when the SPBRG is set to 3 and the TXREG is written while the previous character is still in the TX shift register, the LS bit of the TXREG character may be corrupted during transmission.

**Work around**

When SPBRG is set to 3, wait until the TRMT bit of the TXSTA register is set before loading TXREG with the next character to be transmitted.

### 14. Module: EUSART

In Synchronous Master mode, if the SPBRG register is equal to 0, when the TXEN bit is set, then writing to TXREG will properly start transmission. However, the clock will be improperly out of phase with the data bits and the clock will not stop at the end of the character transmission.

**Work around**

Set SPBRG register to non-zero value before setting the TXEN bit.

### 15. Module: System Clocks

HFINTOSC output frequency is 16 MHz ± 3%, 25°C to 85°C.

**Work around**

None.

### 16. Module: POR/BOR

The POR rearm voltage may be below the low end of the BOR range causing unexpected code execution below the BOR range.

**Work around**

Use external power monitor to hold device in Reset below 1.1 Volts.

### 17. Module: POR

The POR may release around 0.8 volts (below the POR rearm voltage of 1.2V nominal) when VDD rises from below either 0.60V when BOR is not enabled, or 0.33V when BOR is enabled.

**Work around**

Use Power-up Timer when operating with the EC, EXTRC or HFINTOSC oscillator modes. Ensure that VDD rise time is less than the Power-up Timer time.

### 18. Module: POR

The part may hang in the Reset state when VDD falls to the POR rearm threshold of approximately 1.2 volts then rises at a rate faster than 7500 volts per second to the operating range. Recovery from the hung state is possible only by first lowering VDD to below the POR rearm threshold followed by raising VDD to the operating range.

**Work around**

Slow VDD rise time by adding series resistance between the voltage supply and the VDD pin. VDD bypassing should remain on the pin side of the series resistor.

### 19. Module: Clocks

EC Mode operation is limited to a maximum of 48 MHz.

**Work around**

Use HS Clock mode for external clocking above 48 MHz.

### 20. Module: Comparators

Comparator input offset voltage is ± 25 mV and may degrade over the lifetime of the part accelerated by high temperature. The offset voltage increases as the common-mode voltage decreases with the following characteristics: Offset is ± 25 mV when the common-mode voltage is $V_{DD}$; The offset is up to ± 50 mV when the common-mode voltage is $V_{DD}/2$; The offset is greater than ± 50 mV when the common-mode voltage is 0V.

**Work around**

None.

### 21. Module: Comparators

When the CxON bit is clear, the output from the comparator will be properly forced to zero, but the CxPOL bit will improperly have no effect on the CxOUT bit. This prevents presetting the comparator change-on-interrupt mismatch latches as described in the data sheet.

**Work around**

Configure one of the unused comparator input channels as a digital output. Use that digital output to manipulate the comparator output to the desired CxOUT non-interrupt level. When the comparator is then set to the desired inputs, the mismatch latches will be preset to the non-interrupt level and the CxIF flag can then be cleared.

### 22. Module: Data EEPROM Memory

The write/erase endurance of Data EE Memory is limited to 10K cycles.

**Work around**

Use error correction method that stores data in multiple locations.

### 23. Module: Program Flash Memory

The write/erase endurance of the PFM is limited to 1K cycles when $V_{DD}$ is above 3V. Endurance degrades when $V_{DD}$ is below 3V.

**Work around**

For data tables in program Flash memory, use the error correction method that stores data in multiple locations.

### 24. Module: Input/Output (PIC18F26K20 only)

Reading PORTE bit 3 always returns 0.

**Work around**

None.

### 25. Module: Timer 1

In Asynchronous Counter mode, a false interrupt may occur on the first rising T1CKI clock edge after writing the TMR1H or TMR1L register.

**Work around**

Examine the TMR1H:TMR1L register pair in the Interrupt Service Routine (ISR). If the TMR1H:TMR1L register pair is less than the preset value then service the interrupt. Otherwise, disregard the interrupt and only clear the Timer1 interrupt flag.

### Clarifications/Corrections to the Data Sheet:

None.

## APPENDIX A: REVISION HISTORY

Rev. A Document (5/12/08)

First revision of this document.

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