PIC18F1XK50/PIC18LF1XK50 Silicon Errata and Data Sheet Clarification

The PIC18F1XK50/PIC18LF1XK50 family devices that you have received conform functionally to the current Device Data Sheet (DS41350**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F1XK50/PIC18LF1XK50 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A8**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F1XK50/PIC18LF1XK50 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Silicon Revision ID		
		A6	A7	A8
PIC18LF13K50	4700h	06h	07h	08h
PIC18LF14K50	4720h	06h	07h	08h
PIC18F13K50	4740h	06h	07h	08h
PIC18F14K50	4760h	06h	07h	08h

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]		
				A6	A7	A8
ADC (Analog-to-Digital Converter)	Conversions	1.1	INL error and acquisition time.	X	X	
ADC (Analog-to-Digital Converter)	Conversions	1.2	May fail in RUN mode.	X		
ADC (Analog-to-Digital Converter)	Conversions	1.3	High pin leakage.	X	X	X
ADC (Analog-to-Digital Converter)	Conversions	1.4	Offset error.	X	X	
ADC (Analog-to-Digital Converter)	Conversions	1.5	ADC conversion does not complete.	X	X	
MSSP (Master Synchronous Serial Port)	—	2.	SPI and I^2C™ clock and bit issues.	X	X	X
System Clocks	HFINTOSC	3.1	Frequency instability.	X	X	
System Clocks	HFINTOSC	3.2	Frequency shift on Reset.	X		
Timer1	—	4.	Operational temperature.	X	X	X
EUSART	Receive mode	5.1	RCIDL bit issue.	X		
EUSART	OERR flag	5.2	Cannot clear the OERR flag.	X	X	
EUSART	Asynchronous mode	5.3	TX/CK improperly driven.	X	X	X
CPU	Sleep	6.	Reset on Wake-up.	X	X	
Timer1 Oscillator	Operations	7.	Fails to operate above 90°C.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A8**).

1. Module: ADC (Analog-to-Digital Converter)

1.1 Offset error is 3 LSb typical, 7 LSb maximum, including an acquisition time dependent component (~2 LSb).

Work around

The time dependent error is insignificant when the time between conversions is less than 100 ms. When the time since the previous conversion is greater than 100 ms, take two ADC conversions and discard the first.

Affected Silicon Revisions

A6	A7	A8					
X	X						

1.2 When the ADC is configured to operate with the internal FRC oscillator (ADCON2<2:0> = `X11`) and the device is not in Sleep, then the ADC may fail to complete the conversion which is indicated by the GO/$\overline{\text{DONE}}$ bit of the ADCON0 register remaining in the GO state indefinitely. This condition can be cleared by a device Reset or by clearing the ADON bit of the ADCON0 register.

Work around

1. Select a clock source that is not FRC.
2. Set the ADIE bit of the PIE1 register and clear the ADIF bit of the PIR1 register, then put the part to Sleep immediately after setting the GO/$\overline{\text{DONE}}$ bit of the ADCON0 register. The device will perform the conversion during Sleep and Wake at the completion.

Affected Silicon Revisions

A6	A7	A8					
X							

1.3 ADC conversion on AN3/OSC2 will have large INL error up to approximately 8 LSb.

Work around

None for the AN3 pin. For better accuracy, use another analog pin.

Affected Silicon Revisions

A6	A7	A8					
X	X	X					

1.4 The offset error incorrectly exceeds the data sheet specifications if time between conversions is longer than 10 ms. If the time between conversions is greater than 10 ms, the offset error is 1 LSB typical and 3.3 LSB maximum.

Work around

The time dependent error is insignificant when the time between conversions is less than 10 ms. When the time between conversions is greater than 10 ms, take two back-to-back ADC conversions and discard the results of the first conversion.

Affected Silicon Revisions

A6	A7	A8					
X	X						

1.5 Under certain device operating conditions, the ADC conversion may not complete properly. When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the ADGO/$\overline{\text{DONE}}$ bit does not get cleared, and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

Work around

Select the dedicated RC oscillator as the ADC conversion clock source and perform all conversions with the device in Sleep.

Affected Silicon Revisions

A6	A7	A8					
X	X						

2. Module: MSSP (Master Synchronous Serial Port)

When the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011), the first SPI high time may be short.

Work around

Option 1: Ensure TMR2 value rolls over to zero immediately before writing to SSPBUF.

Option 2: Turn Timer2 off and clear TMR2 before writing SSPBUF. Enable TMR2 after SSPBUF is written.

Affected Silicon Revisions

A6	A7	A8					
X	X	X					

3. Module: System Clocks

3.1 Frequency Instability

HFINTOSC output frequency may have up to 1% short term frequency instability.

Work around

Use the HS, XT or EC clock modes.

Affected Silicon Revisions

A6	A7	A8					
X	X						

3.2 Frequency Shift on Reset

The internal oscillator module may experience a ±1% frequency shift after a Reset. The frequency shift is not consistent and could cause the oscillator to operate outside of the 2% specification.

Work around

To minimize the chances of experiencing the frequency shift, the following steps should be taken:

1. Operate the internal oscillator at 8 MHz or 2 MHz.
2. Use an external pull-up on $\overline{\text{MCLR}}$ or use internal $\overline{\text{MCLR}}$ mode.
3. Disable the Power Reset Timer (PWRT).
4. The bypass capacitor and Voltage Regulator Capacitor (VCAP) should be used appropriately to minimize noise in the device.

Affected Silicon Revisions

A6	A7	A8					
X							

4. Module: Timer1

At minimum VDD (1.8V) Timer1 will work, but only up to 100°C, not above.

Work around

None.

Affected Silicon Revisions

A6	A7	A8					
X	X	X					

5. Module: EUSART

5.1 RCIDL Bit

In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when the RX input goes low at the leading edge of a Start bit. If the RX input stays low for less than 1/8th of a bit time, then the Start bit is invalid and the RCIDL should go high. However, the RCIDL bit will stay low improperly until a valid Start bit is received.

Work around

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time, then restore the RCIDL bit by resetting the EUSART module. The EUSART module is reset when the SPEN bit of the RCSTA register is cleared.

Affected Silicon Revisions

A6	A7	A8					
X							

5.2 OERR Bit

The OERR flag of the RCSTA register is reset only by clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

Work around

Clear the OERR flag by clearing the CREN bit instead of clearing the SPEN bit.

Affected Silicon Revisions

A6	A7	A8					
X	X						

5.3 Asynchronous Mode

In Asynchronous mode when TXEN = 0, the TX/CK output is improperly driven. All mid-range parts tri-state the TX/CK pin when TXEN = 0 in Asynchronous mode.

Work around

None.

Affected Silicon Revisions

A6	A7	A8					
X	X	X					

6. Module: CPU

6.1 Reset on Wake-up

If a wake from Sleep event occurs during the execution of a Sleep command, the device may reset. This Reset will be seen as a Power-on Reset to the device.

Work around

1. Disable all asynchronous interrupt before going to Sleep.
2. Make sure the timing of an asynchronous interrupt will not happen during the execution of the SLEEP instruction.

Affected Silicon Revisions

A6	A7	A8					
X	X						

7. Module: Timer1 Oscillator

7.1 Operation above 90°C

The Timer1 oscillator does not operate above 90°C.

Work around

None.

Affected Silicon Revisions

A6	A7	A8					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41350**D**):

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2008)

Initial release of this document

Rev B Document (8/2009)

Updated Errata to new format; minor edits.

Data Sheet Clarifications:

Added Modules 1-8 to add QFN package information to data sheet.

Rev C Document (05/2010)

Removed ‘Rev. A6’ from the title; Added A7 and A8 silicon revisions to Table 1 and Table 2; Removed Note 2 from Table 1; Updated Module 1.4; Added Module 1.5; Removed Table 3; Removed Modules 2.2, 2.3, 2.4, 2.5, 2.6; Added Modules 3.1 and 3.2; Updated Module 4; Added Modules 5.1, 5.2, 5.3, 6 and 7; Updated the Affected Silicon Revision section adding A7 and A8.

Data Sheet Clarifications:

Removed Modules 1 to 8. Data Sheet updated.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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Printed on recycled paper.

ISBN: 978-1-60932-215-1

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