PIC16F/LF1933 Silicon Errata and Data Sheet Clarification

The PIC16F/LF1933 devices that you have received conform functionally to the current Device Data Sheet (DS41364**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16F/LF1933 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16F/LF1933 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			
		A1	A2	A3	A4
PIC16F1933	10 0011 001x xxxx	1	2	3	4
PIC16LF1933	10 0100 001x xxxx	1	2	3	4

Note 1: The Device ID is located in the last configuration memory space.

2: Refer to the *"PIC16F193X/LF193X and PIC16F194X/LF194X Memory Programming Specification"* (DS41397) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: PIC16F1933 SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A1	A2	A3	A4
Data EE Memory	Memory Endurance	1.1	Erase/Write endurance limited.	X			
Data EE Memory	Writes	1.2	Min. VDD for writes.	X	X	X	X
Program Flash Memory (PFM)	Endurance	2.1	Erase/Write endurance limited.	X			
Program Flash Memory (PFM)	Writes	2.2	Min. VDD for writes.	X	X	X	X
Timer1	Timer0 Gate Source	3.1	Toggle mode works improperly.	X	X		
Timer1	Timer1 Gate Toggle mode	3.2	T1 Gate flip-flop does not clear.	X	X	X	
Electrical Specifications	RA6/OSC2 Pin Input Leakage Current	4.1	Input leakage current ranges.	X	X	X	
EUSART	16-Bit High-Speed Asynchronous mode	5.1	Works improperly at maximum rate.	X	X	X	X
Resets	Power-on Reset (POR)	6.1	Reset under low power conditions.	X	X		
ADC	ADC Conversion	7.1	ADC conversion may not complete.	X	X	X	
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	8.1	PWM 0% duty cycle direction change.	X	X	X	X
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	8.2	PWM 0% duty cycle port steering.	X	X	X	X
In-Circuit Serial Programming™ (ICSP™)	Low-Voltage Programming	9.1	Bulk Erase not available with LVP.	X	X	X	
LDO	Minimum VDD above 85°C	10.1	Minimum operating VDD for the PIC16F1933 devices at TA > 85°C.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 3: PIC16LF1933 SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A1	A2	A3	A4
Data EE Memory	Memory Endurance	1.1	Erase/Write endurance limited.	X			
Data EE Memory	Writes	1.2	Min. VDD for writes.	X	X	X	X
Program Flash Memory (PFM)	Endurance	2.1	Erase/Write endurance limited.	X			
Program Flash Memory (PFM)	Writes	2.2	Min. VDD for writes.	X	X	X	X
Timer1	Timer0 Gate Source	3.1	Toggle mode works improperly.	X	X		
Timer1	Timer1 Gate Toggle mode	3.2	T1 Gate flip-flop does not clear.	X	X	X	
Electrical Specifications	RA6/OSC2 Pin Input Leakage Current	4.1	Input leakage current ranges.	X	X	X	
EUSART	16-Bit High-Speed Asynchronous mode	5.1	Works improperly at maximum rate.	X	X	X	X
ADC	ADC Conversion	7.1	ADC conversion may not complete.	X	X	X	
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	8.1	PWM 0% duty cycle direction change.	X	X	X	X
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	8.2	PWM 0% duty cycle port steering.	X	X	X	X
In-Circuit Serial Programming™ (ICSP™)	Low-Voltage Programming	9.1	Bulk Erase not available with LVP.	X	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Data EE Memory

1.1 Data EE Memory Endurance

The typical write/erase endurance of the Data EE Memory is limited to 10k cycles.

Work around

Use error correction method that stores data in multiple locations.

Affected Silicon Revisions

A1	A2	A3	A4				
X							

1.2 Data EE Write at Min. VDD

The minimum voltage required for a Data EE write operation is 2.0 volts.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

2. Module: Program Flash Memory (PFM)

2.1 Program Flash Memory Endurance

The typical write/erase endurance of the PFM is limited to 1k cycles when VDD is above 3.0 volts.

Work around

Use an error correction method that stores data in multiple locations.

Affected Silicon Revisions

A1	A2	A3	A4				
X							

2.2 Program Flash Memory writes at Min. VDD

The minimum voltage required for a PFM write operation is 2.0V.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

3. Module: Timer1

3.1 Timer1 Gate Toggle mode with Timer0 as Gate Source

Timer1 Gate Toggle mode provides unexpected results when Timer0 overflow is selected as the Timer1 gate source. We do not recommend using Timer0 overflow as the Timer1 gate source while in Timer1 Gate Toggle mode or when Toggle mode is used in conjunction with Timer1 Gate Single-Pulse mode.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X						

3.2 Timer1 Gate Toggle mode

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal. To perform this function, the Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the gate signal. Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When working properly, clearing either the T1GTM bit or the TMR1ON bit would also clear the output value of this flip-flop, and hold it clear. This is done in order to control which edge is being measured. The issue that exists is that clearing the TMR1ON bit does not clear the output value of the flip-flop and hold it clear.

Work around

Clear the T1GTM bit in the T1GCON register to clear and hold clear the output value of the flip-flop.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X					

4. Module: Electrical Specifications

4.1 RA6/OSC2 Pin Leakage Range

The Input Leakage Currents on the RA6/OSC2 pin are as follows:

Characteristic	Min.	Typ†	Max.	Units	Conditions	Operating Temperature
RA6/OSC2 Input Leakage Current	—	±5	1500	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at High-Impedance	$-40°C \le T_A \le +85°C$
RA6/OSC2 Input Leakage Current	—	±5	5000	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at High-Impedance	$-40°C \le T_A \le +125°C$

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X					

5. Module: EUSART

5.1 16-Bit High-Speed Asynchronous Mode

The EUSART provides unexpected operation when the 16-Bit High-Speed Asynchronous mode is selected and the Baud Rate Generator Data Register values are loaded with zero (0). We do not recommend using this configuration for EUSART communication. The configuration is shown below in the following table:

Configuration Bits			BRG Data Registers	
SYNC	BRG16	BRGH	SPBRGH Value	SPBRGL Value
0	1	1	00000000	00000000

Work around

Ensure that the SPBRGH or the SPBRGL register is loaded with a non-zero value.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

6. Module: Resets

6.1 Reset under Low-Power Conditions

This issue pertains to the PIC16F1933 product only. The PIC16LF1933 product is not affected by this issue in any way.

When employing any one of the low-power oscillators, (ECL mode, LP Mode, LFINTOSC, or Timer1 Oscillator) while, at the same time, the source voltage supplied to the VDD pin drops below 2.7 volts, the device will experience a Power-on Reset (POR).

Also, when the source voltage supplied to the VDD pin is below 2.7 volts and a SLEEP instruction is executed, the device will experience a Power-on Reset (POR) upon entering Sleep mode, regardless of the type of clock source being used or which power-managed mode is being employed.

Work around

There are three separate work-arounds available to avoid this Reset condition. Employing any one of these work-arounds will avoid this Reset condition.

- Enabling the Brown-out Reset (BOR) circuitry.
- Enabling the Fixed Voltage Reference (FVR) module.
- Maintaining a source voltage (VDD) to the device above 2.7 volts.

The 'Affected Silicon Revisions' below refers only to PIC16F1933.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X						

7. Module: ADC

7.1 Analog-to-Digital Conversion

An ADC conversion may not complete under these conditions:

1. When FOSC is greater than 8 MHz and it is the clock source used for the ADC converter.
2. The ADC is operating from its dedicated internal FRC oscillator and the device is not in Sleep mode (any FOSC frequency).

When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the GO/DONE bit does not get cleared, and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

Work around

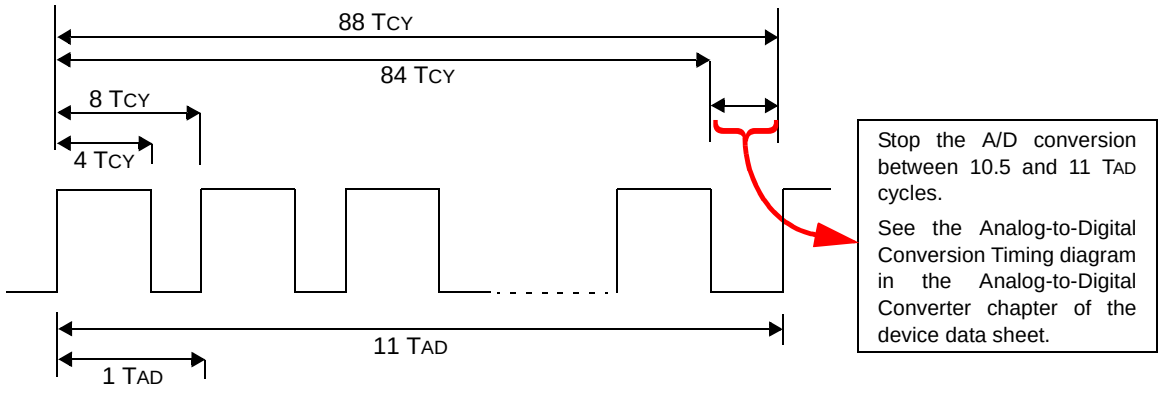
Method 1: Select the system clock, FOSC, as the ADC clock source and reduce the FOSC frequency to 8 MHz or less when performing ADC conversions.

Method 2: Select the dedicated FRC oscillator as the ADC conversion clock source and perform all conversions with the device in Sleep.

Method 3: This method is provided if the application cannot use Sleep mode and requires continuous operation at frequencies above 8 MHz. This method requires early termination of an ADC conversion. Provide a fixed time delay in software to stop the A-to-D conversion manually, after all 10 bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/DONE bit in software. The GO/DONE bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE

FOSC = 32 MHz
TCY = 4/32 MHz = 125 nsec
TAD = 1 µsec, ADCS = FOSC/32



See the ADC Clock Period (TAD) vs. Device Operating Frequencies table, in the Analog-to-Digital Converter section of the device data sheet.

In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of 8 TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

Note: The exact delay time will depend on the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 4 for the required delay counts for other configurations.

EXAMPLE 1: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF    ADCON0, ADGO   ; Start ADC conversion
                      ; Provide 86
                        instruction cycle
                        delay here
BCF    ADCON0, ADGO   ; Terminate the
                        conversion manually
MOVF   ADRESH, W      ; Read conversion
                        result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to Table 4.

TABLE 4: INSTRUCTION CYCLE DELAY COUNTS BY TAD SELECTION

TAD	Instruction Cycle Delay Counts
FOSC/64	172
FOSC/32	86
FOSC/16	43

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X					

8. Module: Enhanced Capture Compare PWM (ECCP)

8.1 Enhanced PWM

When the PWM is configured for Full-Bridge mode and the duty cycle is set to 0%, writing the PxM<1:0> bits to change the direction has no effect on PxA and PxC outputs.

On the A4 revision products only, ECCP1 no longer exhibits this problem.

Work around

Increase the duty cycle to a value greater than 0% before changing directions.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

8.2 Enhanced PWM

In PWM mode, when the duty cycle is set to 0% and the STRxSYNC bit is set, writing the STRxA, STRxB, STRxC and the STRxD bits to enable/disable steering to port pins has no effect on the outputs.

Work around

Increase the duty cycle to a value greater than 0% before enabling/disabling steering to port pins.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

9. Module: In-Circuit Serial Programming™ (ICSP™)

9.1 Bulk Erase Feature not available with Low-Voltage Programming mode

A bulk erase of the program Flash memory or data memory cannot be executed in Low-Voltage Programming mode.

Work around

Method 1: If ICSP Low-Voltage Programming mode is required, use row erases to erase the program memory, as described in the Program/Verify mode section of the Programming Specification. Data memory must be over-written with the desired values.

Method 2: Use ICSP High-Voltage Programming mode if a bulk erase is required.

Note:	Only the bulk erase feature will erase program or data memory if code or data protection is enabled. Method 2 must be used if code or data protection is enabled.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X					

10. Module: LDO

10.1 Minimum V_{DD} above 85°C

The minimum voltage required for the PIC16F1933 devices is 3.5 volts for temperatures above 85°C.

Note:	This issue only applies to the PIC16F1933 devices operating in the Extended temperature range. The PIC16LF1933 devices are not affected.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41364**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Oscillator Module

In Section 5.2.2.6, 32 MHz Internal Oscillator Frequency Selection, the following entry should be added to the existing bullet list, describing the necessary selections for using the 32 MHz clock source:

- The SCS bits in the OSCCON register must be cleared to the clock determined by FOSC<2:0> in Configuration Word 1 selection (SCS<1:0> = 00).

2. Module: EUSART Module

In Register 24-3, BAUDCON: Baud Rate Control Register, the pin descriptions for the Asynchronous mode of the SCKP Synchronous Clock Parity Select bit should have the RB7 port pin designator removed for both bit states. The statement should only refer to the TX/CK pin.

3. Module: Electrical Specifications

In Table 29-2, Oscillator Parameters, the HFINTOSC and MFINTOSC internal calibrated oscillator frequency tolerances should be +/- 3.0% when VDD is equal to, and above 2.5V and when temperatures are equal to, and above 60°C, yet still equal to, or below 85°C, as shown below.

TABLE 29-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	**Sym.**	**Characteristic**	**Freq. Tolerance**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency(2)	±2%	—	16.0	—	MHz	0°C ≤ TA ≤ **+60°C**, VDD ≥ 2.5V
			±3.0%	—	**16.0**	—	**MHz**	**60°C ≤ TA ≤ 85°C, VDD ≥ 2.5V**
			±5%	—	16.0	—	MHz	-40°C ≤ TA ≤ +125°C
OS08A	MFOSC	Internal Calibrated MFINTOSC Frequency(2)	±2%	—	500	—	kHz	0°C ≤ TA ≤ **+60°C**, VDD ≥ 2.5V
			±3.0%	—	**500**	—	**kHz**	**60°C ≤ TA ≤ 85°C, VDD ≥ 2.5V**
			±5%	—	500	—	kHz	-40°C ≤ TA ≤ +125°C
OS10*	TIOSC ST	HFINTOSC Wake-up from Sleep Start-up Time	—	—	5	8	µs	
		MFINTOSC Wake-up from Sleep Start-up Time	—	—	20	30	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

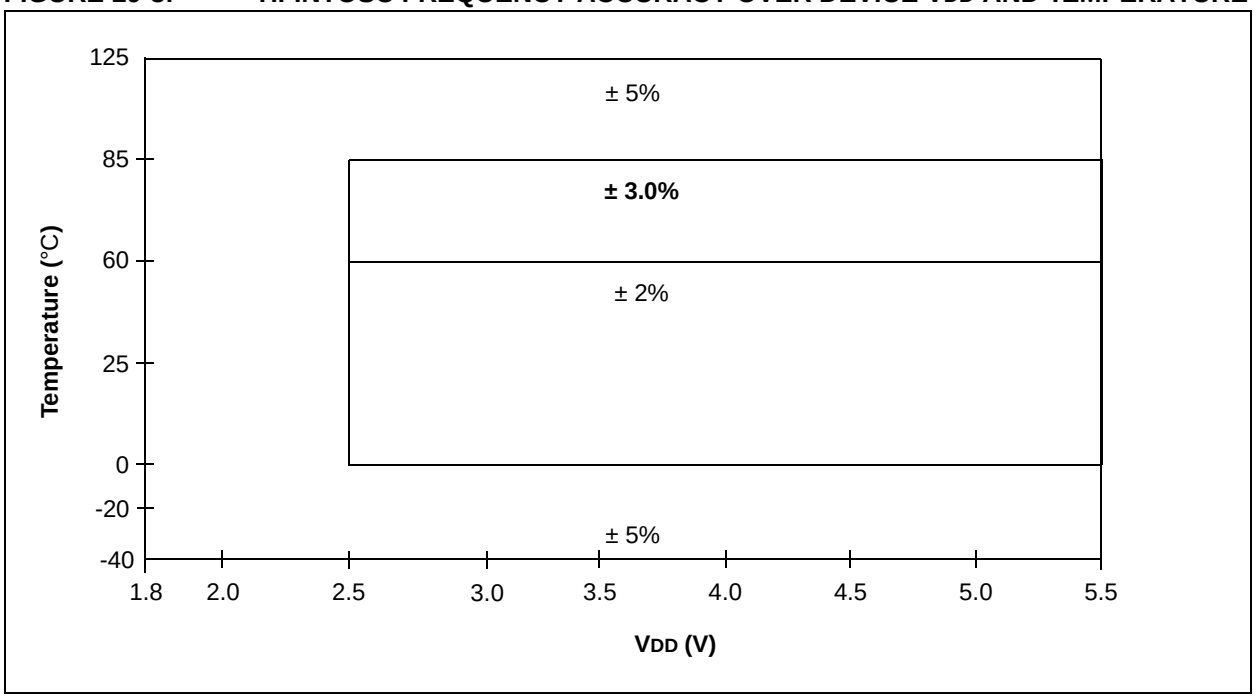
2: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

3: By design.

4. Module: Electrical Specifications

In Figure 29-3, HFINTOSC Frequency Accuracy Over Device VDD and Temperature, the oscillator accuracy should be +/- 3.0% when VDD is equal to, and above 2.5V and when temperatures are equal to, and above 60°C, yet still equal to, or below 85°C, as shown below.

FIGURE 29-3: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2009)

Initial release of this document.

Rev B Document (02/2010)

Added PIC16F1933 device to this errata; Added Rev. A2 for PIC16F/LF1933 (Table 2); Added Table 3.

Added Module 6 to Silicon Errata Issues section.

Data Sheet Clarifications: Added Modules 1 and 2.

Rev C Document (05/2010)

Added Revision A3 to Tables 1, 2 and 3; Added Modules 7, 8.

Data Sheet Clarifications: Added Modules 3 and 4.

Rev D Document (07/2010)

Added Module 3.2; Revised Module 7.1; Added Module 9.1; Other minor corrections.

Rev E Document (08/2010)

Updated errata to the new format; Revised Table below Module 4.1, changing the Max. values; Updated Table 4; Revised Note above Example 1; Other minor corrections.

Rev F Document (10/2010)

Added Silicon Revision A4; Added Module 10: LDO, to Table 2.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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82-2-558-5934

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