PIC18F1XK22/LF1XK22 Family Silicon Errata and Data Sheet Clarification

The PIC18F1XK22/LF1XK22 family devices that you have received conform functionally to the current Device Data Sheet (DS41365**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F1XK22/LF1XK22 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F1XK22/ LF1XK22 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID	Revision ID for Silicon Revision(1)		
		A3	A7	A8
PIC18F14K22	4F20h	03h	07h	08h
PIC18F13K22	4F40h	03h	07h	08h
PIC18LF14K22	4F60h	03h	07h	08h
PIC18LF13K22	4F80h	03h	07h	08h

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory. They are shown in hexadecimal in the format "DEVID:DEVREF".

2: Refer to the *"PIC18F1XK22/LF1XK22 Flash Memory Programming Specification"* (DS41357) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A3	A7	A8
ADC (Analog-to-Digital Converter)	ADC Conversion	1.1	Large INL error on AN3.	X	X	X
ADC (Analog-to-Digital Converter)	ADC Conversion	1.2	ADC conversion does not complete.	X	X	
ECCP	Full Bridge mode	2.	Delay time with direction change.	X	X	X
EUSART	—	3.1	Unreliable RCIDL bit.	X	X	X
EUSART	—	3.2	Clear the OERR flag.	X	X	
EUSART	—	3.3	RX and TX are unavailable for output.	X	X	X
EUSART	—	3.4	Unexpected results.	X	X	X
MSSP (Master Synchronous Serial Port)	—	4.	I^2C™ mode and SPI mode.	X	X	X
In-Circuit Serial Programming™ (ICSP™)	—	5.	ICSP™ works only at V_{DD}>2V.	X	X	X
Oscillator	Clock Switching	6.	FCMEN Configuration bit.	X	X	X
PORTB Interrupt-on-Change	IOCB	7.	Interrupt-on-change.	X	X	X
Resets	Power-on Reset (POR)	8.	Low-power conditions.	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A8**).

1. Module: ADC (Analog-to-Digital Converter)

1.1 ADC conversion on AN3/OSC2 will have large INL error up to approximately 8 LSb.

Work around

None for the AN3 pin. For better accuracy, use another analog pin.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

1.2 An ADC conversion may not complete under these conditions:

1. When FOSC is greater than 8 MHz and is the clock source used for the ADC converter.
2. The ADC is operating from its dedicated internal FRC oscillator and the device is not in Sleep mode (an FOSC frequency).

When this occurs, the ADC Interrupt Fag (ADIF) does not get set, the GO/DONE bit does not get cleared, and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

Work around

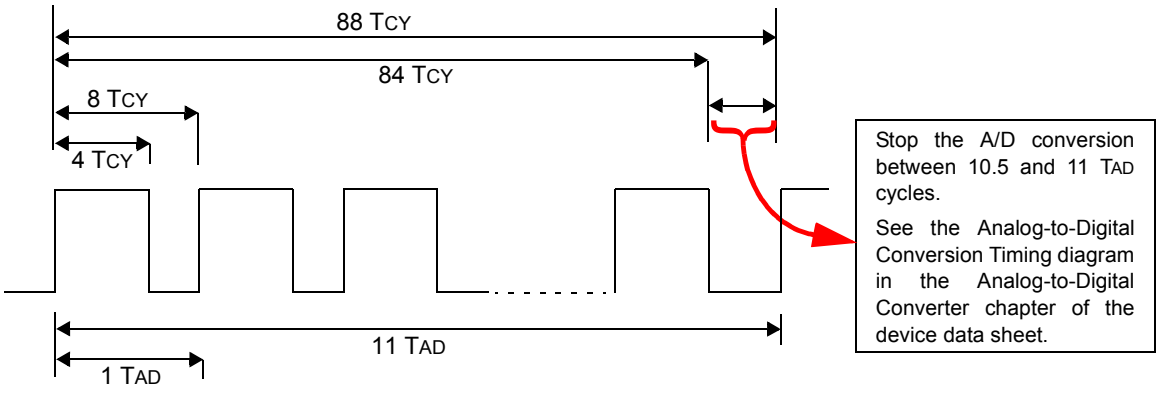
Method 1: Select the system clock, FOSC, as the ADC clock source and reduce the FOSC frequency to 8 MHz or less when performing ADC conversions.

Method 2: Select the dedicated FRC oscillator as the ADC conversion clock source and perform all conversions with the device in Sleep.

Method 3: Method 3 is provided if the application cannot use Sleep mode and requires continuous operation at frequencies above 8 MHz. This method requires early termination of an ADC conversion. Provide a fixed time delay in software to stop the A-to-D conversion manually, after all 10 bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/DONE bit in software. The GO/DONE bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE

FOSC = 32 MHz
TCY = 4/32 MHz = 125 nsec
TAD = 1 µsec, ADCS = FOSC/32



See ADC Clock Period (TAD) vs. Device Operating Frequencies Table, in the Analog-to-Digital Converter chapter of the device data sheet.

In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of 8 TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

Note:	The exact delay time will depend on the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 3 for the required delay counts for other configurations.

EXAMPLE 1: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF    ADCON0, GO     ; Start ADC conversion
                      ; Provide 86
                        instruction cycle
                        delay here
BCF    ADCON0, GO     ; Terminate the
                        conversion manually
MOVF   ADRESH, W      ; Read conversion
                        result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to Table 3.

TABLE 3: INSTRUCTION CYCLE DELAY COUNT VS. TAD

TAD	Instruction Cycle Delay Counts
FOSC/64	172
FOSC/32	86
FOSC/16	43

Affected Silicon Revisions

A3	A7	A8			
X	X				

2. Module: ECCP

2.1 Changing direction in Full-Bridge mode inserts a dead band time of 4/FOSC * TMR2 Prescale instead of 1/FOSC * TMR2 Prescale as specified in the data sheet.

Work around

None.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

2.2 In Full-Bridge mode, when PR2 = CCPR1L, DC1B<1:0> = 00, and the direction is changed, then the dead time before the modulated output starts is compromised. The modulated signal improperly starts immediately with the direction change and stays on for TOSC * TMR2 Prescale * DC1B<1:0>.

Work around

Avoid changing direction when the duty cycle is within three least significant steps of 100% duty cycle. Instead, clear the DC1B<1:0> bits before the direction change and then set them to the desired value after the direction change is complete.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

3. Module: EUSART

3.1 In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when a low pulse greater than 1/16th of a bit time is received on the RX input. The RCIDL bit will then improperly go high if a low pulse less than 1/16 bit time occurs on the RX input within one bit period, after the falling edge of the first pulse. This erratum affects only users monitoring the RCIDL bit as a part of their serial protocol.

Work around

None.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

3.2 The OERR flag of the RCSTA register is reset only by either clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

Work around

Clear the OERR flag by clearing the CREN bit in lieu of clearing the SPEN bit.

Affected Silicon Revisions

A3	A7	A8			
X	X				

3.3 When the SPEN bit of the RCSTA register is set and the CREN bit of the RCSTA register is clear, the RX pin is not available for general purpose output. Likewise, when the SPEN bit of the RCSTA register is set and the TXEN bit of the TXSTA register is clear, the TX pin is not available for general purpose output. However, both the RX and TX pins can be read regardless of the state of the RCSTA and TXSTA control registers.

Work around

None.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

3.4 Unexpected results occur if the EUSART is disabled and then re-enabled with the EUSART receive interrupt and global interrupts enabled, then a single cycle instruction is followed by a 2 cycle instruction.

Work around

Always execute at least 2 single-cycle instructions, immediately following setting the SPEN bit to '1'.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

4. Module: MSSP (Master Synchronous Serial Port)

4.1 In I^2C™ Master mode, baud rates obtained by setting SSPADD to a value less than 0x03 will cause unexpected operation.

Work around

Ensure SSPADD is set to a value greater than or equal to 0x03.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

4.2 In SPI Master mode, when the CKE bit is cleared and the SMP bit is set, the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

Work around

None.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

4.3 When SPI is enabled in Master mode with CKE = 1 and CKP = 0, a 1/FOSC wide pulse will occur on the SCK pin.

Work around

Configure the SCK pin as an input until after the MSSP is setup.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

4.4 In I^2C Master mode, SSPADD values of 0x00, 0x01, 0x02 are invalid. The current I^2C Baud Rate Generator (BRG) is not set up to generate a clock signal for these values.

Work around

None.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

4.5 In I^2C Master mode, the RCEN bit is not cleared by hardware if improper Stop is received on the bus.

Work around

Reset the module via clearing and setting the SSPEN bit of SSPCON1.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

4.6 In SPI Master mode, when the SPI clock is configured for Timer2/2 (SSPCON1 <3:0> = 0011), the first SPI high time may be short.

Work around

Option 1: Ensure TMR2 value rolls over to zero immediately before writing to SSPBUF.

Option 2: Turn Timer2 off and clear TMR2 before writing SSPBUF. Enable TMR2 after SSPBUF is written.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

4.7 In any SPI Master mode, SCK = TMR2/2, if SSPBUF is written to while shifting out data, a ninth SCK pulse is incorrectly generated. At that point, the module locks the user from writing to the SSPBUF register, but a write attempt will still cause 8 or 9 more SCK pulses to be generated.

Work around

The WCOL bit of the SSPCON register is correctly set to indicate that there was a write collision. Any time this bit is set, the module must be disabled and enabled (toggle SSPEN) to return to the correct operation. The bus will remain out of synchronization.

Affected Silicon Revisions.

A3	A7	A8			
X	X	X			

5. Module: In-Circuit Serial Programming™ (ICSP™)

The device cannot be programmed using ICSP when the device V_{DD} is less than 2.0V.

Work around

Ensure that the device voltage is 2.0V or higher when programming the device.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

6. Module: Oscillator

6.1 Clock Switching

6.2 When the FCMEN Configuration bit is set and the IESO Configuration bit is not set, then a clock failure during Sleep will not be detected.

Work around

The IESO Configuration bit must also be set when the FCMEN Configuration bit is set.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

7. Module: PORTB Interrupt-on-Change

Setting a PORTB interrupt-on-change enable bit of the IOCB register while the corresponding PORTB input is high will cause an RBIF interrupt.

Work around

Set the IOCB bits to the desired configuration, then read PORTB to clear the mismatch latches. Finally, clear the RBIF bit before setting the RBIE bit.

Affected Silicon Revisions

A3	A7	A8			
X	X	X			

8. Module: Resets

8.1 Reset under Low Power Conditions

Note:	This issue pertains only to the F product versions, PIC18F14K22/13K22. The LF product versions, PIC18LF14K22/13K22, are not affected by this issue in any way.

When employing any one of the low-power oscillators (ECL mode, LP mode, LFINTOSC or Timer1 Oscillator) at temperatures of -20°C or colder, while at the same time the source voltage supplied to the VDD pin drops below 2.4 volts, the device may experience a Power-on Reset (POR). Also, when the source voltage supplied to the VDD pin is below 2.4 volts, at temperatures of -20°C or colder, and a SLEEP instruction is executed, the device may experience a Power-on Reset (POR) upon entering Sleep mode, regardless of the type of clock source being used or which power-managed mode is being employed.

Work around

There are four work arounds available to avoid this Reset condition:

1. Enabling the Brown-out Reset (BOR) circuitry.
2. Enabling the Fixed Voltage Reference (FVR) module.
3. Maintaining a source voltage (VDD) to the device above 2.4 volts when operating at temperatures of -20°C or colder.
4. Use the LF product version (PIC18LF14K22/13K22) where the operational VDD requirement is between 1.8V and 3.6V.

Affected Silicon Revisions

A3	A7	A8			
X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41365**D**).

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev. A Document (3/2009)

Initial release of this document.

Rev. B Document (5/2009)

Revised Table 1; Added Table 2; Added Module 8: Internal Oscillator.

Added Data Sheet Clarifications Module 1: Electrical Specifications and Module 2: Device Overview.

Rev. C Document (4/2010)

Updated Table 1 and Table 2 adding revisions A7 and A8; Added Module 1.2; Added Module 3.4; Added Module 9: PORTB Interrupt-on-Change.

Data Sheet Clarifications:

Removed Modules 1 and 2.

Rev. D Document (7/2010)

Deleted Module 5, Module 6 and renumbered modules; Added Module 8 (Resets).

Note the following details of the code protection feature on Microchip devices:

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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