PIC16F1934/1936/1937 and PIC16LF1934/1936/1937

PIC16F1934/1936/1937 and PIC16LF1934/1936/1937 Family Silicon Errata and Data Sheet Clarification

The PIC16F1934/1936/1937 and PIC16LF1934/1936/1937 family devices that you have received conform functionally to the current Device Data Sheet (DS41364**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16F1934/1936/1937 and PIC16LF1934/1936/1937 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A6**).

Data Sheet clarifications and corrections start on page 8, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16F1934/1936/1937 and PIC16LF1934/1936/1937 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			
		A2	A3	A5	A6
PIC16F1934	10 0011 010x xxxx	2	3	5	6
PIC16LF1934	10 0100 010x xxxx	2	3	5	6
PIC16F1936	10 0011 011x xxxx	2	3	5	6
PIC16LF1936	10 0100 011x xxxx	2	3	5	6
PIC16F1937	10 0011 100x xxxx	2	3	5	6
PIC16LF1937	10 0100 100x xxxx	2	3	5	6

Note 1: The Device ID is located in the last configuration memory space.

2: Refer to the *"PIC16F193X/LF193X and PIC16F194X/LF194X Memory Programming Specification"* (DS41397) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A2	A3	A5	A6
EEPROM	Memory Endurance	1.1	Erase/Write Endurance Limited.	X	X	X	
EEPROM	Writes	1.2	Min. VDD for Writes.	X	X	X	X
Prog. Mem.	Endurance	2.1	Erase/Write Endurance Limited.	X	X	X	
Prog. Mem.	Writes	2.2	Min. VDD for Writes.	X	X	X	X
CCP	PWM Dead Band Delay	3.1	Unpredictable Waveforms.	X	X	X	X
CCP	ECCP2 Switching	3.2	PWM Outputs.	X	X	X	X
CCP	ECCP2 Changing Direction	3.3	Outputs will Improperly go Active.	X	X	X	X
CCP	Capture mode	3.4	Capture will be triggered.	X	X	X	X
CCP	ECCPx Dead Time Delay	3.5	Dead Band Delay.	X	X	X	X
CCP	PWM with Pulse Steering	3.6	PWM Output.	X	X	X	X
CCP	Capture mode	3.7	Capture will be triggered.	X	X	X	X
BOR	Threshold	4.1	Voltage Level.	X			
ADC	ADC Conversion	5.1	ADC Conversion may not complete.	X	X	X	
Oscillator	HS Oscillator	6.1	HS Oscillator min. VDD.	X	X	X	X
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	7.1	PWM 0% Duty Cycle Direction Change.	X	X	X	X
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	7.2	PWM 0% Duty Cycle Port Steering.	X	X	X	X
Timer1	Timer0 Gate Source	8.1	Toggle Mode works Improperly.	X	X	X	X
Timer1	Timer1 Gate Toggle mode	8.2	T1 Gate Flip-Flop does not clear.	X	X	X	X
LDO	Minimum VDD above 85°C	9.1	Minimum operating VDD for the PIC16F193X devices at TA > 85°C.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**).

1. Module: Data EE Memory

1.1 Data EE Memory Endurance

The typical write/erase endurance of the Data EE Memory is limited to 10k cycles.

Work around

Use error correction method that stores data in multiple locations.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X					

1.2 Data EE Write at Min. VDD

The minimum voltage required for a Data EE write operation is 2.0 volts.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

2. Module: Program Flash Memory (PFM)

2.1 Program Flash Memory Endurance

The typical write/erase endurance of the PFM is limited to 1k cycles when VDD is above 3.0 volts. Endurance degrades when VDD is below 3V.

Work around

Use an error correction method that stores data in multiple locations.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X					

2.2 Program Flash Memory writes at Min. VDD

The minimum voltage required for a PFM write operation is 2.0V.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

3. Module: Capture Compare PWM (CCP)

3.1 Dead Band Delay

With the ECCP configured for PWM half-bridge mode and a dead-band delay greater than or equal to the PWM duty cycle; unpredictable wave forms will result.

Work around

Make sure the dead-band delay is always less than the PWM duty cycle.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

3.2 ECCP2 Switching Between Single, Half-Bridge and Full-Bridge PWM modes

Switching PWM mode during the current PWM cycle by modifying the P2M[1:0] bits in the CCP2CON register will cause the PWM outputs to switch immediately and not on the start of the next PWM cycle.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

3.3 ECCP2 Changing Direction in Full-Bridge PWM modes

When changing direction the active and modulated outputs will improperly go active at the same time and the dead time does not occur which can lead to large shoot-through currents.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

3.4 Capture mode Selected while CCPx Pin is Held High

If the module is configured to capture on the first rising edge and the CCPx pin is high at this time, a capture will be triggered.

Work around

Clear the CCP interrupt flag (`CCPxIF = 0`) immediately after configuring the module for a capture event.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

3.5 ECCPx Dead Time Delay in Half-Bridge mode

In Half-Bridge mode the dead band delay is 1 TOSC longer than calculated for the first PWM cycle and 1.5 TOSC for following cycles.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

3.6 PWM with Pulse Steering

Disabling a PWM output during a PWM cycle will cause the output to end one TOSC time earlier than expected.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

3.7 Capture mode Selected while CCPx Pin is Held Low

If the module is configured to capture on the first falling edge and the CCPx pin is low at this time, a capture will be triggered.

Work around

Clear the CCP interrupt flag (`CCPxIF = 0`) immediately after configuring the module for a capture event.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

4. Module: Brown-Out Reset (BOR)

4.1 Brown-Out Threshold

Configuring the BOR for 2.5V operation, the reset will typically occur at 2.7V.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6				
X							

5. Module: ADC

5.1 Analog-to-Digital Conversion

An ADC conversion may not complete under these conditions:

1. When FOSC is greater than 8 MHz and it is the clock source used for the ADC converter.
2. The ADC is operating from its dedicated internal FRC oscillator and the device is not in Sleep mode (any FOSC frequency).

   When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the GO/DONE bit does not get cleared, and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

   Work around

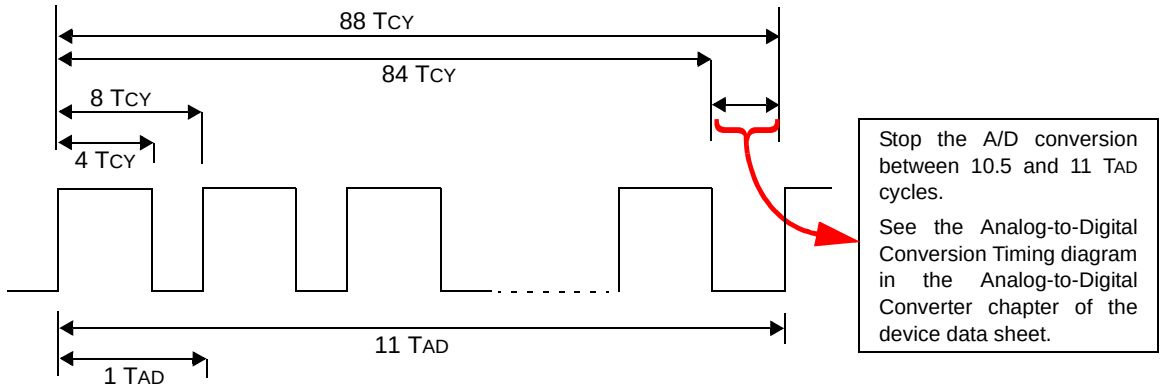
   Method 1: Select the system clock, FOSC, as the ADC clock source and reduce the FOSC frequency to 8 MHz or less when performing ADC conversions.

   Method 2: Select the dedicated FRC oscillator as the ADC conversion clock source and perform all conversions with the device in Sleep.

   Method 3: This method is provided if the application cannot use Sleep mode and requires continuous operation at frequencies above 8 MHz. This method requires early termination of an ADC conversion. Provide a fixed time delay in software to stop the A-to-D conversion manually, after all 10 bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/DONE bit in software. The GO/DONE bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE

FOSC = 32 MHz
TCY = 4/32 MHz = 125 nsec
TAD = 1 µsec, ADCS = FOSC/32



See the ADC Clock Period (TAD) vs. Device Operating Frequencies table, in the Analog-to-Digital Converter chapter of the device data sheet.

In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of 8 TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

Note: The exact delay time will depend on the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 3 for the required delay counts for other configurations.

EXAMPLE 1: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF    ADCON0, ADGO   ; Start ADC conversion
                      ; Provide 86
                        instruction cycle
                        delay here
BCF    ADCON0, ADGO   ; Terminate the
                        conversion manually
MOVF   ADRESH, W      ; Read conversion
                        result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to Table 3.

TABLE 3: INSTRUCTION CYCLE DELAY COUNTS BY TAD SELECTION

TAD	Instruction Cycle Delay Counts
FOSC/64	172
FOSC/32	86
FOSC/16	43

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X					

6. Module: Oscillator

6.1 HS Oscillator

The HS oscillator requires a minimum voltage of 3.0 volts (at 65°C or less) to operate at 20 MHz.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

7. Module: Enhanced Capture Compare PWM (ECCP)

7.1 Enhanced PWM

When the PWM is configured for Full-Bridge mode and the duty cycle is set to 0%, writing the PxM<1:0> bits to change the direction has no effect on PxA and PxC outputs.

Work around

Increase the duty cycle to a value greater than 0% before changing directions.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

7.2 Enhanced PWM

In PWM mode, when the duty cycle is set to 0% and the STRxSYNC bit is set, writing the STRxA, STRxB, STRxC and the STRxD bits to enable/disable steering to port pins has no effect on the outputs.

Work around

Increase the duty cycle to a value greater than 0% before enabling/disabling steering to port pins.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

8. Module: Timer1

8.1 Timer1 Gate Toggle mode with Timer0 as Gate Source

Timer1 Gate Toggle mode provides unexpected results when Timer0 overflow is selected as the Timer1 gate source. We do not recommend using Timer0 overflow as the Timer1 gate source while in Timer1 Gate Toggle mode or when Toggle mode is used in conjunction with Timer1 Gate Single-Pulse mode.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

8.2 Timer1 Gate Toggle mode

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal. To perform this function, the Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the gate signal. Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When working properly, clearing either the T1GTM bit or the TMR1ON bit would also clear the output value of this flip-flop, and hold it clear. This is done in order to control which edge is being measured. The issue that exists is that clearing the TMR1ON bit does not clear the output value of the flip-flop and hold it clear.

Work around

Clear the T1GTM bit in the T1GCON register to clear and hold clear the output value of the flip-flop.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

9. Module: LDO

9.1 Minimum V_{DD} above 85°C

The minimum voltage required for the PIC16F193X devices is 3.5 volts for temperatures above 85°C.

Note: This issue only applies to the PIC16F193X devices operating in the Extended temperature range. The PIC16LF193X devices are not affected.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6				
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41364**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Specifications

In Table 29-2, Oscillator Parameters, the HFINTOSC and MFINTOSC internal calibrated oscillator frequency tolerances should be +/- 3.0%, when VDD is equal to, and above 2.5V and when temperatures are equal to, and above 60°C, yet still equal to, or below 85°C, as shown below.

TABLE 29-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	**Sym.**	**Characteristic**	**Freq. Tolerance**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency(2)	±2%	—	16.0	—	MHz	0°C ≤ TA ≤ **+60°C**, VDD ≥ 2.5V
			±3.0%	—	**16.0**	—	**MHz**	**60°C ≤ TA ≤ 85°C, VDD ≥ 2.5V**
			±5%	—	16.0	—	MHz	-40°C ≤ TA ≤ +125°C
OS08A	MFOSC	Internal Calibrated MFINTOSC Frequency(2)	±2%	—	500	—	kHz	0°C ≤ TA ≤ **+60°C**, VDD ≥ 2.5V
			±3.0%	—	**500**	—	**kHz**	**60°C ≤ TA ≤ 85°C, VDD ≥ 2.5V**
			±5%	—	500	—	kHz	-40°C ≤ TA ≤ +125°C
OS10*	TIOSC ST	HFINTOSC Wake-up from Sleep Start-up Time	—	—	5	8	µs	
		MFINTOSC Wake-up from Sleep Start-up Time	—	—	20	30	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

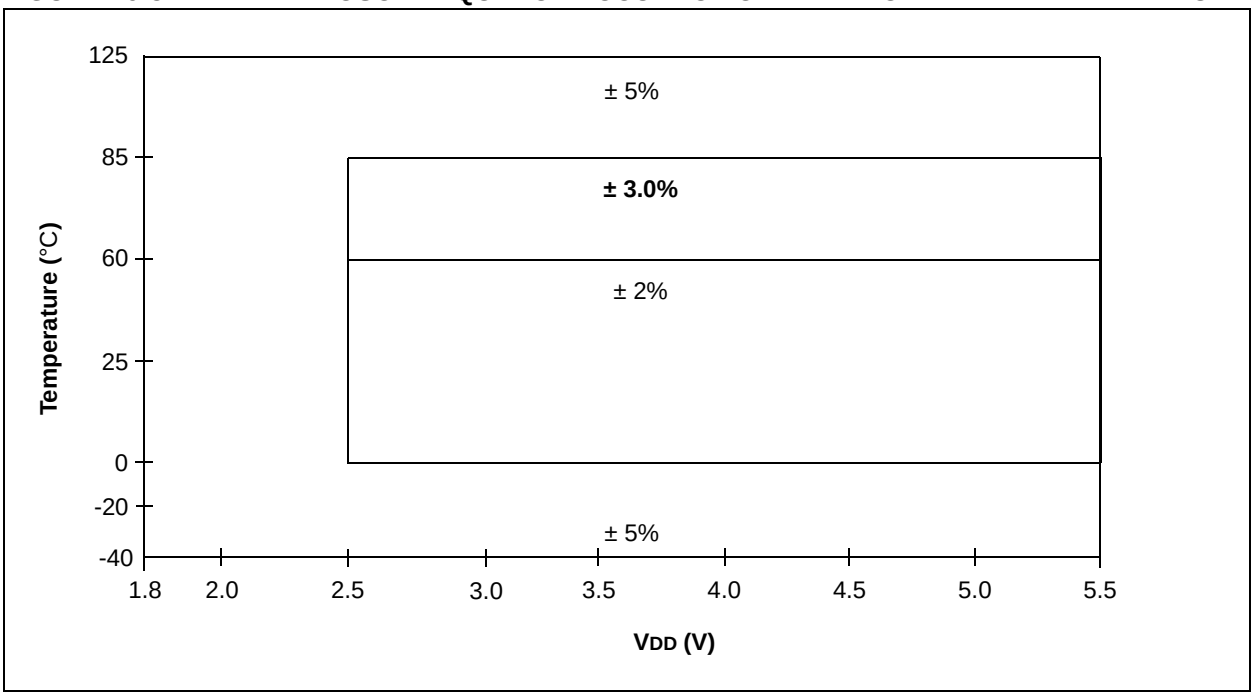
2: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

3: By design.

2. Module: Electrical Specifications

In Figure 29-3, HFINTOSC Frequency Accuracy Over Device VDD and Temperature, the oscillator accuracy should be +/- 3.0% when VDD is equal to, and above 2.5V and when temperatures are equal to, and above 60°C, yet still equal to, or below 85°C, as shown below.

FIGURE 29-3: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (9/2009)

Initial release of this document.

Rev B Document (1/2010)

Added silicon revision A5.

Rev C Document (5/2010)

Added Modules 5, 6, 7 and 8.

Data Sheet Clarifications: Added Modules 1 and 2.

Rev D Document (6/2010)

Added Silicon Revision A6.

Rev E Document (7/2010)

Revised Module 5.1; Added Module 8.2; Other minor corrections.

Rev F Document (9/2010)

Added Module 9, LDO.

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Printed on recycled paper.

ISBN: 978-1-60932-559-6

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