# PIC18F24K20/25K20/44K20/45K20 Silicon Errata and Data Sheet Clarification

The PIC18F24K20/25K20/44K20/45K20 family devices that you have received conform functionally to the current Device Data Sheet (DS41303**G**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F24K20/25K20/44K20/45K20 silicon.

**Note 1:** This document summarizes all silicon errata issues from all specified revisions of silicon.

**2:** Shaded areas in Table 1 and Table 2 are for older device revisions that are no longer in production.

Data Sheet clarifications and corrections start on page 11, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

**Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F24K20/25K20/44K20/45K20 silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | Device ID(1) (11-bit) | Revision ID for Silicon Revision(2) (5-bit) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | A4 | A7 | A9 | AB | A4 | A7 | A8 | AE |
| PIC18F24K20 | 105h | 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
| PIC18F25K20 | 103h | 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
| PIC18F44K20 | 104h | 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
| PIC18F45K20 | 102h | 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |

**Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID:DEVREV".

**2:** Refer to the *"PIC18F2XK20/4XK20 Flash Memory Programming Specification"* (DS41297) for detailed information on Device and Revision IDs for your specific device.

**3:** Shaded cells in this table indicate older device revisions that are no longer in production.

**TABLE 2: SILICON ISSUE SUMMARY**

| Module | Feature | Item Number | Issue Summary | Affected Revisions(1) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | A4 | A7 | A9 | AB | A4 | A7 | A8 | AE |
| | | | | 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
| ECCP | CCP1CON | 1. | Changing CCP1M bits may cause capture of Timer1 value. | X | X | X | X | | | | |
| ECCP | Full-Bridge mode | 2. | Direction change issue. | X | X | X | X | | | | |
| MSSP SPI | SPI Clock | 3. | Shortened SPI high time. | X | X | X | X | | | | |
| MSSP $I^2C$™ | Slew Rate | 4. | Slow slew rate when SLRCON<2> is set. | X | X | X | X | | | | |
| ADC | Offset | 5. | Time dependent on offset. | X | X | X | X | | | | |
| MSSP $I^2C$ | Receiving | 6. | Address may be received as data. | X | X | X | X | | | | |
| MSSP $I^2C$ | Master mode | 7. | Master mode not functional. | X | | | | | | | |
| MSSP SPI | SPI Master | 8. | Improper sampling of last bit. | X | X | X | X | | | | |
| MSSP SPI | SPI Master | 9. | $\overline{SS}$PBUF improperly reloads on $\overline{SS}$ pin transitions. | X | X | X | X | | | | |
| MSSP SPI | SPI Master | 10. | Improper extra pulse on SCK pin. | X | X | X | X | | | | |
| EUSART | Synchronous Master mode | 11. | Duty cycle of CK output is skewed when SPBRG is odd. | X | X | X | X | | | | |
| EUSART | Synchronous Master mode | 12. | LS bit corruption during transmission when SPBRG = 3. | X | X | X | X | | | | |
| EUSART | Synchronous Master mode | 13. | Clock fails to stop at end of character transmission when SPBRG = 0. | X | X | X | X | | | | |
| Internal Fixed Voltage Reference (FVR) | — | 14. | FVRST bit activates prematurely. | X | X | | | | | | |
| High Low Voltage Detect (HLVD) | — | 15. | IVRST bit activates prematurely. | X | X | | | | | | |
| BOR | FVR | 16. | Unexpected BOR occurrence. | X | X | | | | | | |
| System Clocks | — | 17. | HFINTOSC output accuracy. | X | X | X | X | | | | |
| POR/BOR | — | 18. | Unexpected code execution at low $V_{DD}$. | X | X | X | X | | | | |
| POR | — | 19. | Premature POR release. | X | X | X | X | | | | |
| POR | — | 20. | POR may become stuck. | X | X | X | X | | | | |
| Clocks | EC mode | 21. | 48 MHz maximum frequency. | X | X | | | | | | |
| Comparators | Interrupt-on-Change | 22. | Presetting interrupt-on-change issue. | X | X | X | X | | | | |
| Data EEPROM Memory | Endurance | 23. | Endurance is limited to 10K cycles. | X | X | X | X | X | X | X | |
| Program Flash Memory | Endurance | 24. | Endurance is limited to 1K cycles. | X | X | X | X | X | X | X | |
| Configuration Bits | CONFIG3H | 25. | HFOFST bit erases to '0' instead of '1'. | X | X | X | X | | | | |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

**2:** Shaded cells in this table indicate older device revisions that are no longer in production.

**TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)**

| Module | Feature | Item Number | Issue Summary | Affected Revisions[1] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | A4 | A7 | A9 | AB | A4 | A7 | A8 | AE |
| | | | | 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
| EUSART | Asynchronous Receive mode | 26. | RCIDL bit may stay low improperly. | X | X | X | X | | | | |
| PORTB Interrupts | Interrupt-on-Change | 27. | False interrupt when setting interrupt enable. | X | X | X | X | X | X | X | X |
| ADC | ADC Conversion | 28. | ADC conversion may be limited to half scale. | X | X | X | X | X | X | X | |
| ECCP | Full-Bridge mode | 29. | Wrong dead-band time. | | | | | X | X | X | X |
| ECCP | Full-Bridge mode | 30. | Wrong signal start time. | | | | | X | X | X | X |
| MSSP SPI | SPI Clock | 31. | Improper SCK output. | | | | | X | X | X | X |
| MSSP SPI | SPI Master | 32. | Improper sampling of last bit. | | | | | X | X | X | X |
| MSSP SPI | SPI Master | 33. | Improper handling of write collision. | | | | | X | X | X | X |
| MSSP $I^2C$™ | $I^2C$™ Master | 34. | Improper handling of Stop event. | | | | | X | X | X | X |
| EUSART | OERR Flag | 35. | Clearing SPEN bit does not clear OERR flag. | | | | | X | X | X | X |
| EUSART | BAUDCTL | 36. | RCIDL bit may stay low improperly. | | | | | X | X | X | X |
| PORTB Interrupts | Interrupt-on-Change | 37. | False interrupt when waking from Sleep. | | | | | X | X | X | X |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

**2:** Shaded cells in this table indicate older device revisions that are no longer in production.

## Silicon Errata Issues

**Note 1:** This document summarizes all silicon errata issues from all specified revisions of silicon.

**2:** Shaded cells in this section indicate latest silicon in production.

### 1. Module: ECCP

Changing the CCP1M<3:0> bits of CCP1CON may cause the CCPR1H and CCPR1L registers to capture the value of Timer1.

**Work around**

Halt Timer1 before changing ECCP mode. Reload Timer1 with desired value after ECCP is setup and before Timer1 is restarted.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 2. Module: ECCP

Changing direction in Full-Bridge mode does not insert dead time between changing the active drivers in common legs of the bridge.

**Work around**

None.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 3. Module: MSSP SPI

When the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011), the first SPI high time may be short.

**Work around**

Option 1: Ensure TMR2 value rolls over to zero immediately before writing to SSPBUF.

Option 2: Turn Timer2 off and clear TMR2 before writing SSPBUF. Enable TMR2 after SSPBUF is written.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 4. Module: MSSP I²C™

Slew rate is slower than I²C specifications when the SLRCON<2> bit is set.

**Work around**

Clear SLRCON<2> bit when using the I²C peripheral.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 5. Module: ADC

Offset error is 3 LSb typical, 7 LSb maximum, including an acquisition time-dependent component (~2 LSb).

**Work around**

The time dependent error is insignificant when the time between conversions is less than 100 ms. When the time since the previous conversion is greater than 100 ms then take two ADC conversions and discard the first.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 6. Module: MSSP I²C

If a new address byte is received while the BF flag is set, the SSPOV bit is properly set and an ACK is not properly generated. If only the SSPOV bit is set (BF flag was cleared) and a matching address is clocked in, that received byte will be improperly loaded into the SSPBUF register and an ACK will be improperly generated.

**Work around**

None.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 7. Module: MSSP I²C

I²C Master mode is not functional (Rev. A4 only).

**Work around**

Use software to emulate Master mode.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 8. Module: MSSP SPI

In SPI Master mode, when the CKE bit is cleared and the SMP bit is set, the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

**Work around**

None.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 9. Module: MSSP SPI

In SPI Master mode, when CKE bit is set, the SSPBUF will reload the SSPSR output shift register on every high-to-low transition of the $\overline{SS}$ pin.

**Work around**

Avoid using the $\overline{SS}$ pin when the CKE bit is set and the MSSP is configured for SPI Master mode.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 10. Module: MSSP SPI

When SPI is enabled in Master mode with CKE = 1 and CKP = 0, a 1/FOSC wide pulse will occur on the SCK pin.

**Work around**

Configure SCK pin as an input until after the MSSP is setup.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 11. Module: EUSART

In Synchronous Master mode, when the SPBRG is set to an odd number, the duty cycle of the CK output will be skewed by one baud clock count.

**Work around**

High values of SPBRG will minimize the effect of this anomaly.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 12. Module: EUSART

In Synchronous Master mode, when the SPBRG is set to 3 and the TXREG is written while the previous character is still in the TX shift register, the LS bit of the TXREG character may be corrupted during transmission.

**Work around**

When SPBRG is set to 3, wait until the TRMT bit of the TXSTA register is set before loading TXREG with the next character to be transmitted.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 13. Module: EUSART

In Synchronous Master mode, if the SPBRG register is equal to 0 when the TXEN bit is set, then writing to TXREG will properly start transmission. However, the clock will be improperly out of phase with the data bits and the clock will not stop at the end of the character transmission.

**Work around**

Set SPBRG register to non-zero value before setting the TXEN bit.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 14. Module: Internal Fixed Voltage Reference (FVR)

The FVRST bit of the CVRCON2 register activates prematurely (Rev. A4 and A7 only).

**Work around**

Wait an additional 20 µs after FVRST is sensed high before using the fixed voltage reference. Enable the FVR by setting the FVREN bit of the CVRCON2 register before activating any peripheral that automatically enables the FVR. Peripherals that automatically enable the FVR include the Brown-out Reset, the High/Low Voltage Detect, and the HFINTOSC.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 15. Module: High Low Voltage Detect (HLVD)

The IVRST bit of the HLVDCON register activates prematurely (Rev. A4 and A7 only).

**Work around**

Wait an additional 20 µs after IVRST is sensed high before using the fixed voltage reference. Enable the FVR by setting the FVREN bit of the CVRCON2 register before activating any peripheral that automatically enables the FVR. Peripherals that automatically enable the FVR include the Brown-out Reset, the High/Low Voltage Detect, and the HFINTOSC.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 16. Module: BOR

An unexpected Brown-out Reset may occur when the fixed voltage reference is inactive and BOR is activated, thereby activating the fixed voltage reference simultaneously. This error is caused by a premature FVRST stable flag (Rev. A4 and A7 only).

**Work around**

Enable the FVR by setting the FVREN bit of the CVRCON2 register and then wait an additional 20 µs after FVRST is sensed high before enabling BOR. Brown-out disable in Sleep mode with automatic enable on wake-up cannot be used.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 17. Module: System Clocks

HFINTOSC output frequency is 16 MHz ±3%, 25°C to 85°C.

**Work around**

None.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 18. Module: POR/BOR

The POR rearm voltage may be below the low end of the BOR range, causing unexpected code execution below the BOR range.

**Work around**

Use external power monitor to hold the device in Reset below 1.1V.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 19. Module: POR

The POR may release around 0.8V (below the POR rearm voltage of 1.2V, nominal) when VDD rises from below 0.60V (when BOR is not enabled) or 0.33V (when BOR is enabled).

**Work around**

Use Power-up Timer when operating with the EC, EXTRC or HFINTOSC oscillator modes. Ensure that VDD rise time is less than the Power-up Timer time.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 20. Module: POR

The part may hang in the Reset state when VDD rises to the operating range at a rate faster than 7500V per second. Recovery from the hung state is possible only by first lowering VDD to below 0.3V, followed by raising VDD to the operating range.

**Work around**

Slow VDD rise time by adding series resistance between the voltage supply and the VDD pin and increasing the VDD bypass capacitance. VDD bypassing should remain on the pin side of the series resistor.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 21. Module: Clocks

EC mode operation is limited to a maximum of 48 MHz (Rev. A4 and A7 only).

**Work around**

Divide external clock by 4 and use HS-PLL Clock mode for external clocking above 48 MHz.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 22. Module: Comparators

When the CxON bit is clear, the output from the comparator will be properly forced to zero, but the CxPOL bit will improperly have no effect on the CxOUT bit. This prevents presetting the comparator change-on-interrupt mismatch latches as described in the data sheet.

**Work around**

Configure one of the unused comparator input channels as a digital output. Use that digital output to manipulate the comparator output to the desired CxOUT non-interrupt level. When the comparator is then set to the desired inputs, the mismatch latches will be preset to the non-interrupt level and the CxIF flag can then be cleared.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 23. Module: Data EEPROM Memory

The write/erase endurance of Data EE Memory is limited to 10K cycles.

**Work around**

Use error correction method that stores data in multiple locations.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | |

### 24. Module: Program Flash Memory

The write/erase endurance of the PFM is limited to 1K cycles when VDD is above 3V. Endurance degrades when VDD is below 3V.

**Work around**

For data tables in program Flash memory use error correction method that stores data in multiple locations.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | |

### 25. Module: Configuration Bits

Bit 3 of CONFIG3H defaults to '0' after a Bulk Erase instead of '1' as specified in the data sheet.

**Work around**

Program the HFOFST bit to the desired state after a Bulk Erase. All MPLAB® IDE programming tools currently perform this way.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 26. Module: EUSART

In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when an invalid Start bit less than 1/8th of a bit time is received. The RCIDL bit will then stay low improperly until a valid Start bit is received.

**Work around**

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time, then restore the RCIDL bit by resetting the EUSART module. The EUSART module is reset when the SPEN bit of the RCSTA register is cleared.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | |

### 27. Module: PORTB

Setting a PORTB interrupt-on-change enable bit of the IOCB register while the corresponding PORTB input is high will cause an RBIF interrupt.

**Work around**

Set the IOCB bits to the desired configuration, then read PORTB to clear the mismatch latches. Finally, clear the RBIF bit before setting the RBIE bit.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X |

### 28. Module: ADC

After extended stress, the Most Significant bit (MSb) of the ADC conversion result can become stuck at '0'. Conversions resulting in code 511 or less are still accurate, but conversions that should result in codes greater than 511 are, instead, pinned at 511.

The potential for failures is a function of several factors:

- The potential for failures increases over the life of the part. No failures have ever been seen for accelerated stress estimated to be equivalent to 34 years at room temperature. The failure rate after accelerated stress estimated to be equivalent to 146 years at room temperature can be as high as 10% for $V_{DD}$ = 1.8V. The time to failure will decrease as the operating temperature increases.
- The potential for failures is highest at low $V_{DD}$ and decreases as $V_{DD}$ increases.

**Work around**

1. Restrict the input voltage to less than 1/2 of the ADC voltage reference so that the expected result is always a code less than or equal to 511.
2. Use manual acquisition time (ACQT<2:0> = 000) and put the part to Sleep after each conversion.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | |

### 29. Module: ECCP

Changing direction in Full-Bridge mode inserts a dead-band time of 4/FOSC * TMR2 Prescale instead of 1/FOSC * TMR2 Prescale as specified in the data sheet.

**Work around**

None.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| | | | | X | X | X | X |

### 30. Module: ECCP

ECCP – In Full-Bridge mode when PR2 = CCPR1L and DC1B[1:0] <>'00' and the direction is changed, then the dead time before the modulated output starts is compromised. The modulated

signal improperly starts immediately with the direction change and stays on for TOSC * TMR2 Prescale * DC1B[1:0].

**Work around**

Avoid changing direction when the duty cycle is within three Least Significant steps of 100% duty cycle. Instead, clear the DC1B[1:0] bits before the direction change and then set them to the desired value after the direction change is complete.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| | | | | X | X | X | X |

### 31. Module: MSSP SPI

When the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011) and the CKE bit of the SSPSTAT register is '1', then when SSPBUF is written, the SCK output is improperly immediately driven to the non-Idle state together with the MSb value of the SSPBUF. The duration at which SDO and SCK remain at these levels may be shorter than a full half-bit period. The remaining bits in the byte are output properly.

**Work around**

None.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| | | | | X | X | X | X |

### 32. Module: MSSP SPI

In SPI Master mode, when the CKE bit of the SSPSTAT register is cleared and the SMP bit of the SSPSTAT register is set, then the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

**Work around**

None.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| | | | | X | X | X | X |

### 33. Module: MSSP SPI

In SPI Master mode, if the SSPBUF register is written while a byte is actively being transmitted, an extra clock pulse will be improperly generated at the end of the transmission. Further writes to the SSPBUF register will be inhibited although 8 or 9 clock pulses will be generated for each attempted write. The WCON bit of the SSPCON register is properly set indicating that a write collision occurred. However, the write collision condition can only be cleared by resetting the MSSP module. Clear the MSSP by clearing the SSPEN bit of the SSPCON1 register.

**Work around**

Use the SSPIF bit of the PIR1 register or the BF bit of the SSPSTAT register to determine that the transmission is complete before writing the SSPBUF register. In the event that a write collision does occur, use the slave select feature to resynchronize the slave clock.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| | | | | X | X | X | X |

### 34. Module: MSSP I²C™

In Master I²C Receive mode if a Stop condition occurs in the middle of an address or data reception, then the SCL clock stream will continue endlessly and the RCEN bit of the SSPCON2 register will remain set improperly. If a Start condition occurs after the improper Stop condition then 9 additional clocks will be generated followed by the RCEN bit going low.

**Work around**

Use low-impedance pull-ups on the SDA line to reduce the possibility of noise glitches which may trigger an improper Stop event. Use a time-out event timer to detect the unexpected Stop condition and resulting stuck RCEN bit. Clear the stuck RCEN bit by clearing the SSPEN bit of SSPCON1.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| | | | | X | X | X | X |

### 35. Module: EUSART

The OERR flag of the RCSTA register is reset only by clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

**Work around**

Clear the OERR flag by clearing the CREN bit instead of clearing the SPEN bit.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| | | | | X | X | X | X |

### 36. Module: EUSART

In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when an invalid Start bit less than 1/16th of a bit time is received. The RCIDL bit will then properly go high 1/8th of a bit time later. However, if another invalid Start bit occurs less than 1 bit time after the leading edge of the first invalid Start bit, then the RCIDL bit will improperly stay high then improperly go low one bit time later. The RCIDL bit will then stay low improperly until a valid Start bit is received.

**Work around**

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time, then restore the RCIDL bit by resetting the EUSART module. The EUSART module is reset when the SPEN bit of the RCSTA register is cleared.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| | | | | X | X | X | X |

### 37. Module: Interrupt-on-Change

When any interrupt-on-change is enabled and the corresponding input is high, then waking from Sleep by a source other than interrupt-on-change may cause the RBIF interrupt flag bit to become set improperly.

**Work around**

1. Use the INTx interrupt in lieu of interrupt-on-change.

Or

2. Store the state of the PORTB inputs before entering Sleep. Upon waking, if an RBIF is detected, then compare the PORTB levels with those stored. If they are the same, then clear and ignore the RBIF interrupt.

**Affected Silicon Revisions**

| 0xA | 0xC | 0xE | 0x11 | 0x16 | 0x18 | 0x19 | 0x1B |
|---|---|---|---|---|---|---|---|
| | | | | X | X | X | X |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41303**G**):

None.

## APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (12/2008)

Initial release of this document.

Rev B Document (05/2009)

Updated Errata to new format; Added Module 11: PORTB and Module 12: ADC; minor edits.

Clarifications/Corrections to the Data Sheet: Added Module 1: MSSP; Module 2: Electrical Specifications; Module 3: Electrical Specifications.

Rev C Document (06/2009)

Clarifications/Corrections to the Data Sheet:

Deleted Module 1: MSSP: Figure 17-17 Baud Rate Generator Block Diagram, updating subsequent numbering. Added Module 3 MSSP: Register 17-3 SSPADD; Added Module 4 MSSP: Section 17.4.2 Operation; Added Module 5 MSSP: Figure 17-16 MSSP Block Diagram; Added Module 6 MSSP: Sections 17.4.7.1, 17.4.8, 17.4.9, 17.4.17.1, 17.4.17.2, 17.4.17.3: SSPADD, changing <6:0> to <7:0>.

Rev D Document (11/2009)

Updated to add revision 0x1B.

Data Sheet Clarifications: Deleted Modules 1, 2, 3, 4, 5, 6.

Rev E Document (04/2010)

Updated to include early revisions of silicon, revision IDs 0xA through 0x11. These early revisions were described in DS80366 errata, which is now obsolete.

Rev F Document (05/2010)

Updated Table 1.

Rev G Document (07/2010)

Removed ADC Work around #2 and changed #3 to #2 (Module 28).

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