

Quad bidirectional Transil™ array for ESD protection

Features

- 4 Bidirectional Transil functions
- ESD Protection: IEC 61000-4-2 level 4
- Stand off voltage: 12 V Min.
- Low leakage current < 1 μ A
- 50 W Peak pulse power (8/20 μ s)

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards

Complies with the following standards

- IEC 61000-4-2
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- MIL STD 883F- Method 3015-7: class3
 - 25 kV (human body model)

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems and cellular phones
- Video equipment

Description

The ESDA14V2-4BF2 is a monolithic array designed to protect up to 4 lines (bidirectional) against ESD transients.

This device is particularly adapted to the protection of symmetrical signals.

The device is ideal for situations where board space saving is requested.

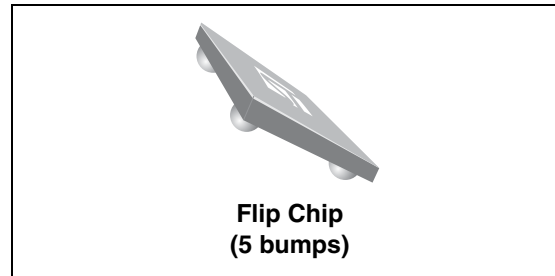


Figure 1. Device configuration

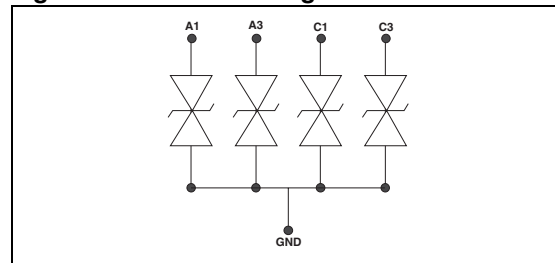
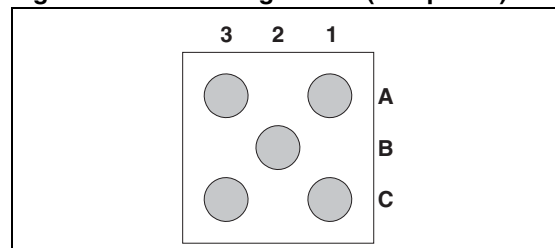


Figure 2. Pin configuration (bump side)



TM: Transil is a trademark of STMicroelectronics.

1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter		Value	Unit
V _{PP}	ESD discharge	MIL STD 883E - Method 3015-7 IEC61000-4-2 air discharge IEC61000-4-2 contact discharge	± 25 ± 15 ± 8	kV
P _{PP}	Peak pulse power (8/20 μs)		50	W
T _j	Junction temperature		125	°C
T _{stg}	Storage temperature range		-55 to +150	°C
T _L	Lead solder temperature (10 seconds duration)		260	°C
T _{op}	Operating temperature range		-40 to +125	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter							
V _{RM}	Stand-off voltage							
V _{BR}	Breakdown voltage							
V _{CL}	Clamping voltage							
I _{RM}	Leakage current @ V _{RM}							
I _{PP}	Peak pulse current							
C	Capacitance							
R _d	Dynamic resistance							
Types	V _{BR} @ I _R			I _{RM} @ V _{RM}		R _d	αT	C
	min.	max.		max.		typ. ⁽¹⁾	max. ⁽²⁾	typ. 0 V bias
	V	V	mA	μA	V	Ω	10 ⁻⁴ /C	pF
ESDA6V1SC5	14.2	18	1	1 0.1	12 3	3.2	10	15

1. Square pulse, I_{pp} = 3 A, tp = 2.5 μs.
2. Δ V_{BR} = αT * (T_{amb} -25 °C) * V_{BR} (25 °C)

Figure 3. Clamping voltage versus peak pulse current (T_j initial = 25 °C) (Rectangular waveform, $t_p = 2.5 \mu s$)

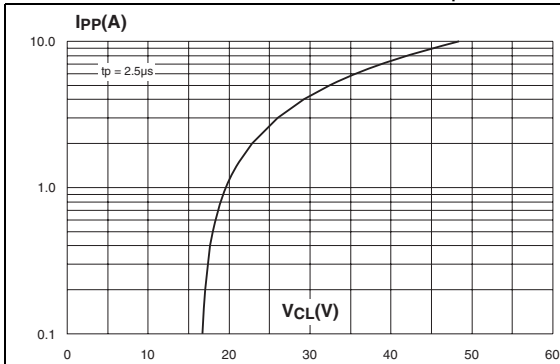


Figure 4. Capacitance versus reverse applied voltage (typical values)

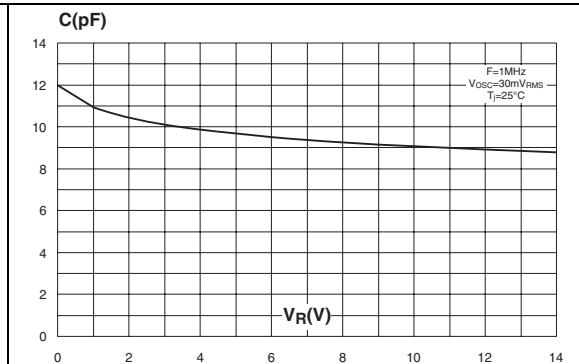


Figure 5. Relative variation of leakage current versus junction temperature (typical values)

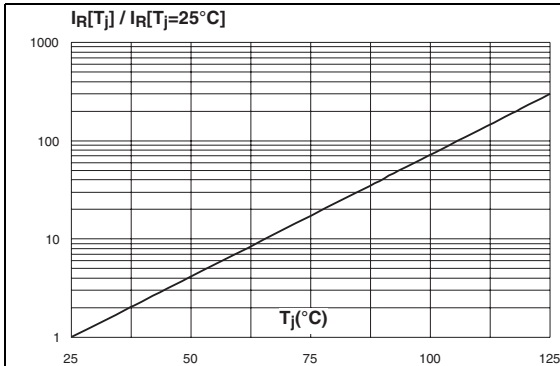


Figure 6. ESD response to IEC 61000-4-2 (+15 kV air discharge)

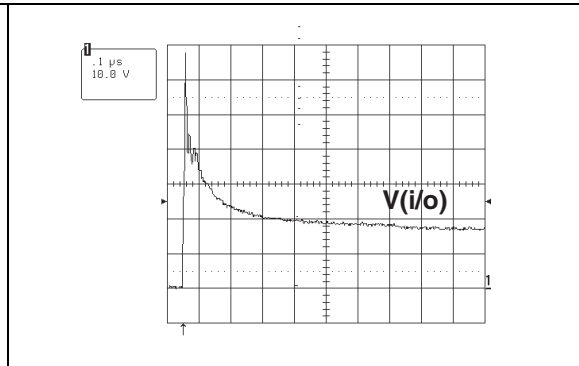


Figure 7. ESD response to IEC 61000-4-2 (-15 kV air discharge)

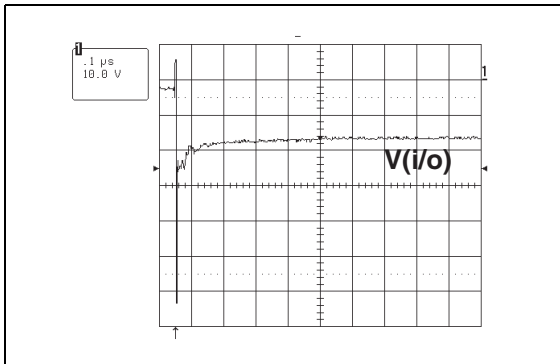


Figure 8. Analog crosstalk

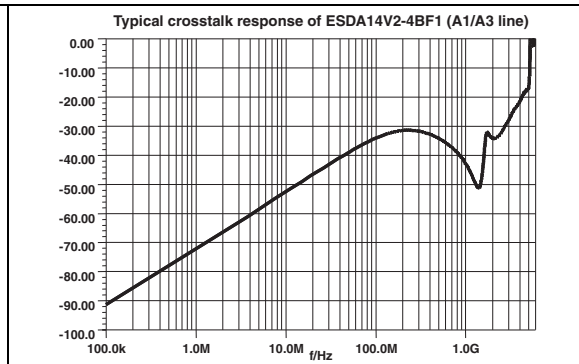
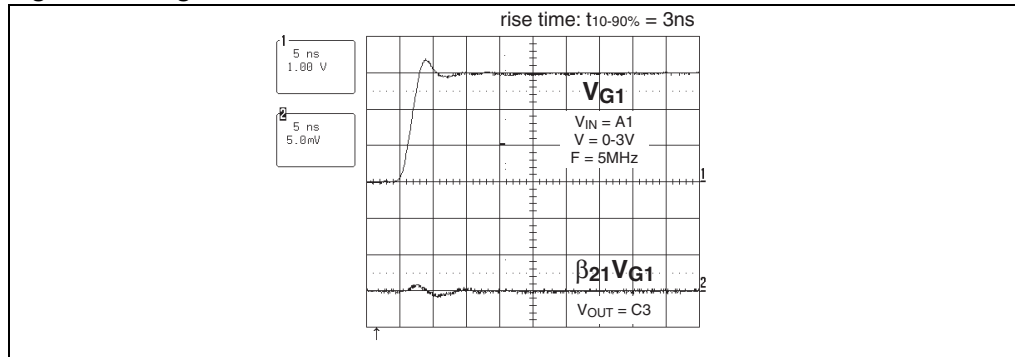


Figure 9. Digital crosstalk



2 Application information

Figure 10. Application example

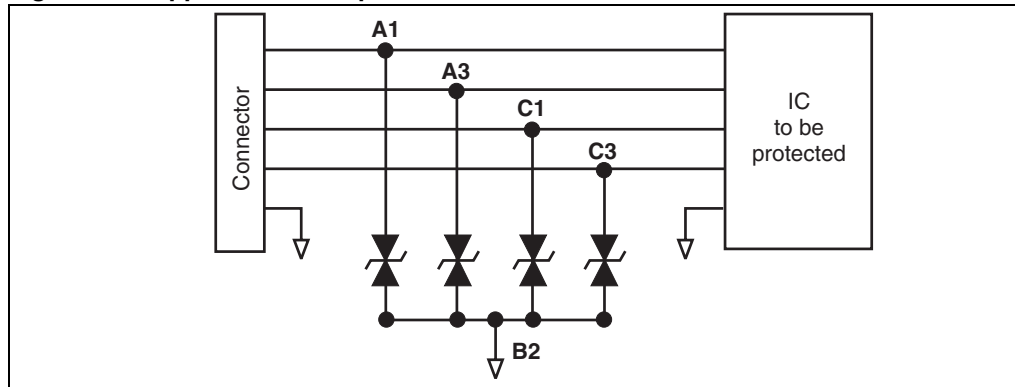
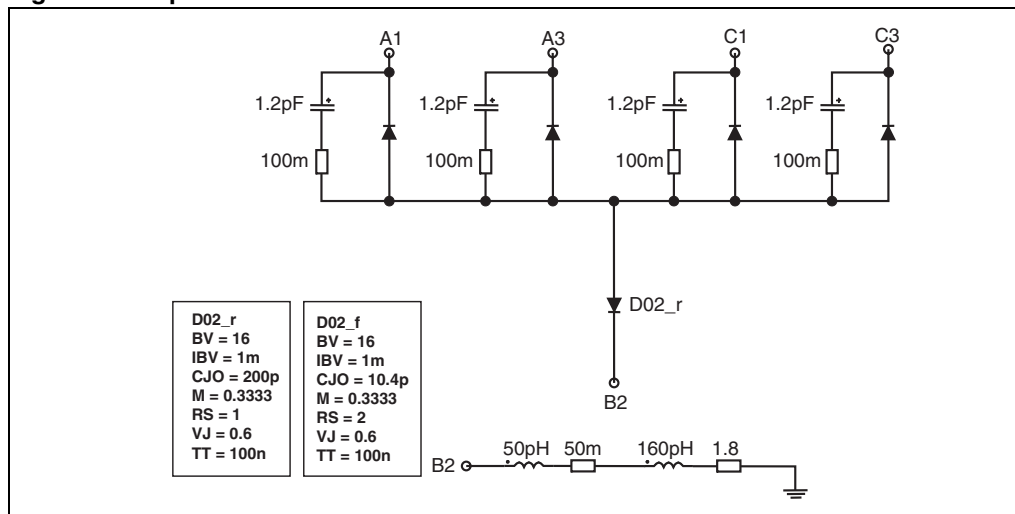
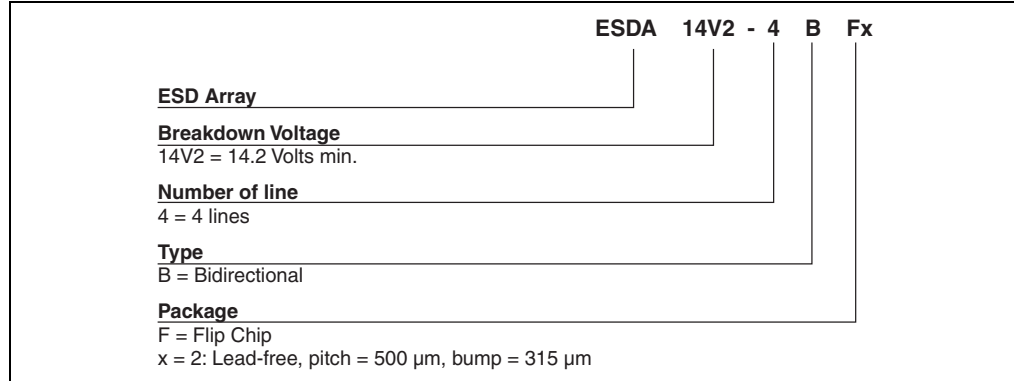


Figure 11. Aplac model



3 Ordering information scheme

Figure 12. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 13. Flip Chip package mechanical data

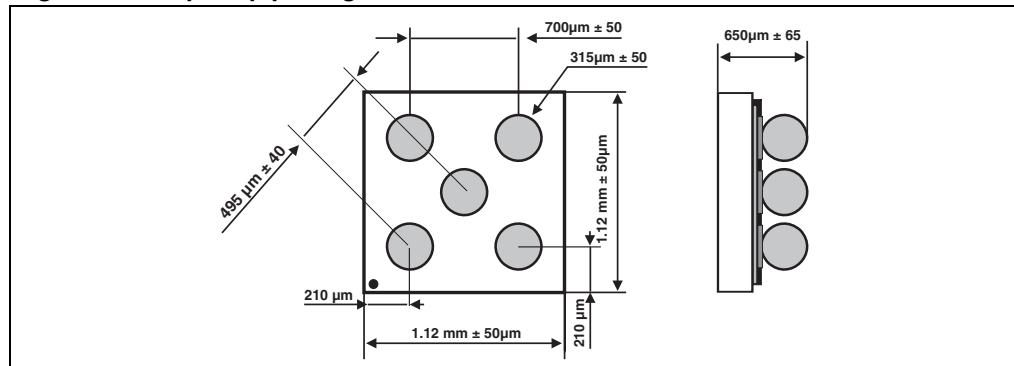


Figure 14. Foot print recommendations Figure 15. Marking

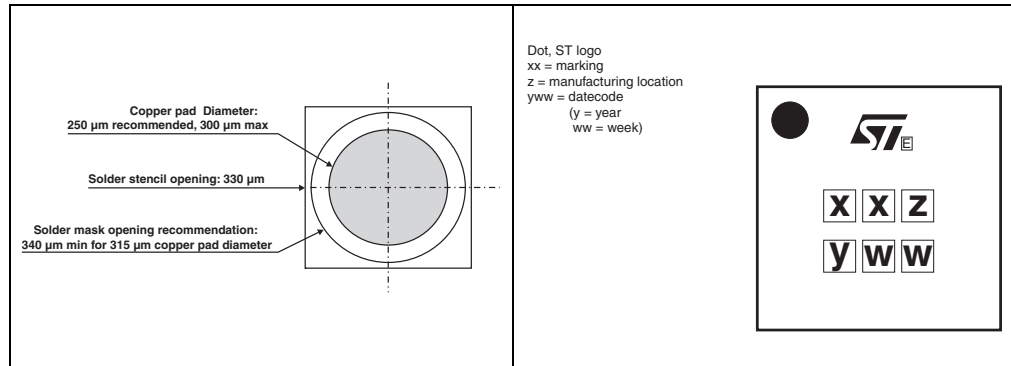
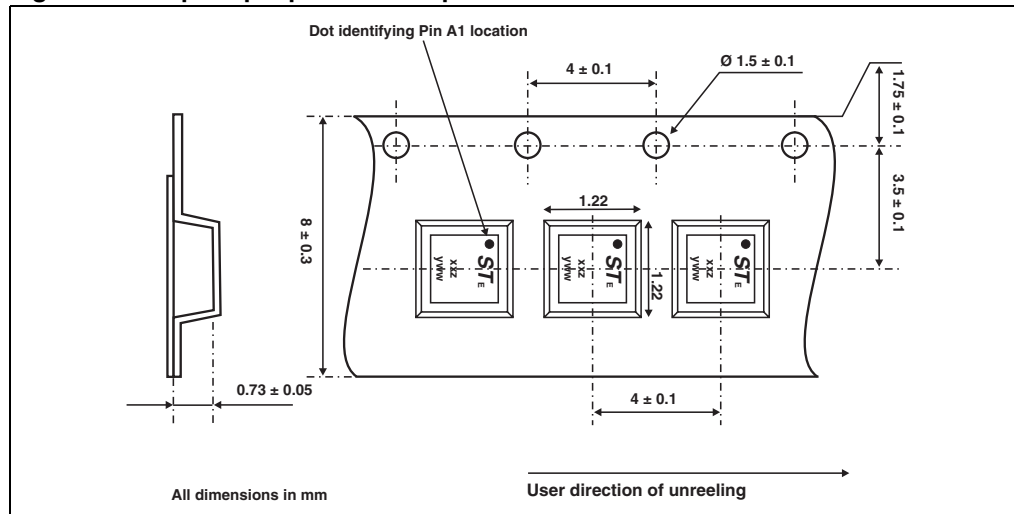


Figure 16. Flip Chip tape and reel specification



5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDA14V2-4BF2	EA	Flip Chip	2.1 mg	5000	Tape and reel 7"

Note: More information is available in the application notes:
 AN1235: "Flip Chip: Package description and recommendations for use"
 AN1751: "EMI filters: Recommendations and measurements"

6 Revision history

Table 4. Document revision history

Date	Revision	Description of changes
14-Mar-2005	1	First issue.
18-Oct-2005	2	Dimension from center bump to corner bump changed in Figure 16 . to indicate diagonal instead of perpendicular measurement. No values changed. ECOPACK statement added.
04-Jun-2007	3	Reformatted to current standard.
16-Apr-2008	4	Updated ECOPACK statement. Updated Figure 12 , Figure 13 and Figure 16 . Reformatted to current standards.

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