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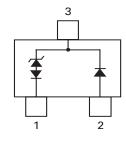
GREEN

F RoHS

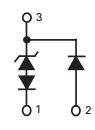
SPLV2.8 Series 2.8V 50A TVS Array



Pinout



Functional Block Diagram



Description

The SPLV2.8 was designed to protect low voltage, CMOS devices from ESD and lightning induced transients. There is a compensating diode in parallel with the low voltage TVS to protect one unidirectional line or a high speed data pair when two devices are paired together. These robust structures can safely absorb repetitive ESD strikes at ± 30 kV (contact discharge) per the IEC61000-4-2 standard and each structure can safely dissipate up to 40A (IEC61000-4-5, t_p=8/20µs) with very low clamping voltages.

Features

- ESD, IEC61000-4-2, ±30kV contact, ±30kV air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 40A (8/20µs)

Applications

- 10/100/1000 Ethernet
- Analog Inputs
 - Base Stations

Low capacitance of 2pF

• Low leakage current of

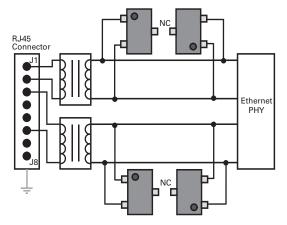
per line (Pin 2 to 1)

1µA (MAX) at 2.8V • Small SOT23-3 package

saves board space

- WAN/LAN EquipmentSwitching Systems
- Desktops, Servers, and Notebooks

Application Example



See Application Example Detail section on page 135 for more information

SPLV2.8

Electrical Characteristics (T _{op} = 25°C)						
Parameter	Symbol	Test Conditions Min		Тур	Max	Units
Reverse Standoff Voltage	V _{RVVM}	I _R ≤1µA			2.8	V
Reverse Breakdown Voltage	V _{BR}	I _τ =2μA	3.0			V
Snap Back Voltage	Back Voltage V _{SB} I _T =50mA 2.8				V	
Reverse Leakage Current	ILEAK	V _R =2.8V (Pin 2 or 3 to 1)			1	μA
Clamping Voltage ¹		I _{PP} =5A, t _P =8/20μs (Pin 3 to 1)		5.7	7.0	V
Clamping Voltage ¹		I _{pp} =24A, t _p =8/20μs (Pin 3 to 1)		8.3	12.5	V
Clamping Voltage ¹	V _c	I _{PP} =5A, t _P =8/20μs (Pin 2 to 1)		7.0	8.5	V
Clamping Voltage ¹		I _{pp} =24A, t _p =8/20μs (Pin 2 to 1)		13.9	15.0	V
Dynamic Resistance	R _{DYN}	$(V_{_{C2}} - V_{_{C1}})$ / $(I_{_{PP2}} - I_{_{PP1}})$ (Pin 2 to 1)		0.4		Ω
ESD Withstand Voltage ¹		IEC61000-4-2 (Contact)	±30			kV
	V _{ESD}	IEC61000-4-2 (Air)	±30			kV
Diode Capacitance ¹	C _D	V _R =0V, f=1MHz (Pin 2 to 1)		2.0	2.5	pF

Note: ¹Parameter is guaranteed by design and/or device characterization.

Absolute Maximum Ratings

Parameter	Rating	Units
Peak Pulse Power (t _p =8/20µs)	600	W
Peak Pulse Current (t _P =8/20µs)	40	А
Operating Temperature	-40 to 85	°C
Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Figure 1: Capacitance vs. Reverse Voltage

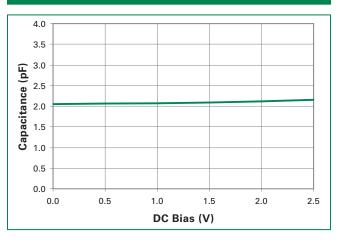


Figure 3: Pulse Waveform

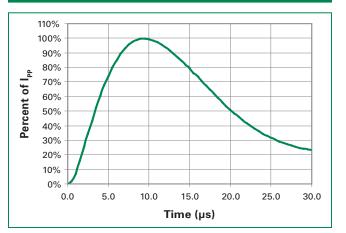
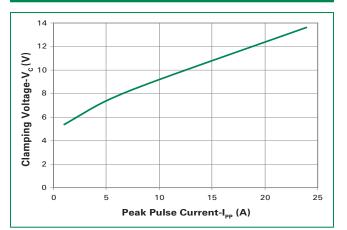


Figure 2: Clamping Voltage vs. I



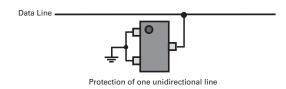
SPLV2.8 Series

TVS Diode Arrays (SPA[™] Family of Products)

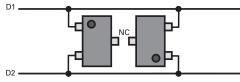
Lightning Surge Protection - SPLV2.8 Series



Application Example Detail

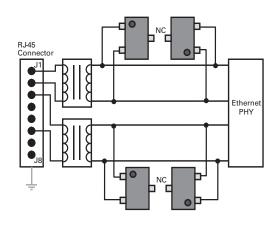


Protection of one unidirectional data line is realized by connecting pin 3 to the protected line, and pins 1 and 2 to GND. In this configuration, the device presents a maximum loading capacitance of tens of picofarads. During positive transients, the internal TVS diode will conduct and steer current from pin 3 to 1 (GND), clamping the data line at or below the specified voltages for the device (see Electrical Characteristics section). For negative transients, the internal compensating diode is forward biased, steering the current from pin 2 (GND) to 3.



Low capacitance protection of one high speed data pair

Low capacitance protection of a high-speed data pair is realized by connecting two devices in antiparallel. As shown, pin 1 of the first device is connected to D1 and pin 2 is connected to D2. Additionally, pin 2 of the second device is connected to D1 and pin 1 is connected to D2. Pin 3 must be NC (or not connected) for both devices. When the potential on D1 exceeds the potential on D2 (by the rated standoff voltage), pin 2 on the second device will steer current into pin 1. The compensating diode will conduct in the forward direction steering current into the avalanching TVS diode which is operating in the reverse direction. For the opposite transient, the first device will behave in the same manner. In this two device arrangement, the total loading capacitance is two times the rated capacitance from pin 2 to pin 1 which will typically be much less than 10pF making it suitable for highspeed data pair such as 10/100/1000 Ethernet.



Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes

1. All dimensions are in millimeters 2.

Dimensions include solder plating. Dimensions are exclusive of mold flash & metal burr.

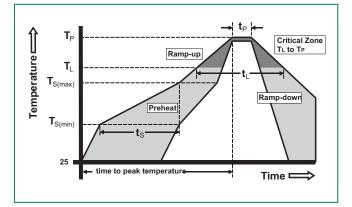
З. All specifications comply to JEDEC SPEC MO-203 Issue A 4.

Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form. 5.

Package surface matte finish VDI 11-13

Soldering Parameters

Reflow Condition		Pb – Free assembly	
	-Temperature Min (T _{s(min)})	150°C	
Pre Heat	-Temperature Max (T _{s(max)})	200°C	
	-Time (min to max) (t _s)	60 – 180 secs	
Average ra (T _L) to pea	amp up rate (Liquidus) Temp k	3°C/second max	
T _{S(max)} to T _L	- Ramp-up Rate	3°C/second max	
Reflow	-Temperature (T _L) (Liquidus)	217°C	
nellow	-Temperature (t _L)	60 – 150 seconds	
Peak Temperature (T _P)		250 ^{+0/-5} °C	
Time within 5°C of actual peak Temperature (t _p)		20 – 40 seconds	
Ramp-down Rate		6°C/second max	
Time 25°C to peak Temperature (T _P)		8 minutes Max.	
Do not exceed		260°C	



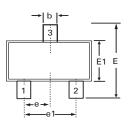
SPLV2.8

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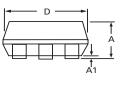


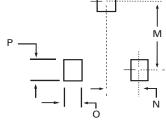
TVS Diode Arrays (SPA^M Family of Products) Lightning Surge Protection - SPLV2.8 Series

Package Dimensions – SOT-23



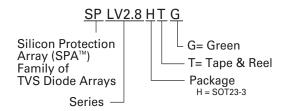
Recommended Pad Layout





Package	SOT23-3				
Pins	3				
JEDEC	TO-236				
	Millin	netres	Inches		
	Min	Max	Min	Max	
Α	0.89	1.12	0.035	0.044	
A1	0.01	0.1	0.0004	0.004	
b	0.3	0.5	0.012	0.020	
С	0.08	0.2	0.003	0.008	
D	2.8	3.04	0.110	0.120	
E	2.1	2.64	0.083	0.104	
E1	1.2	1.4	0.047	0.055	
е	0.95 BSC		0.038	0.038 BSC	
e1	1.90 BSC		0.075 BSC		
L1	0.54 REF		0.021 REF		
М		2.29		.90	
Ν		0.95		0.038	
0		0.78		0.30 TYP	
Р		0.78		0.30 TYP	

Part Numbering System



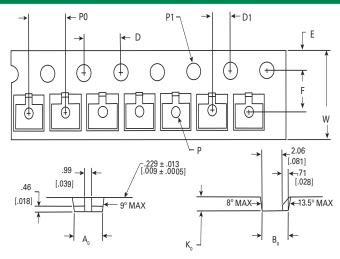
Part Marking System



Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SPLV2.8HTG	SOT23-3	U2.8	3000

Embossed Carrier Tape & Reel Specification – SOT23-3 Package



O weak at	Millim	netres	Inches	
Symbol	Min	Max	Min	Max
A0	3.05	3.25	0.12	0.128
B0	2.67	2.87	0.105	0.113
D	3.9	4.1	0.153	0.161
D1	1.95	2.05	0.788	0.792
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.136	0.14
К0	1.12	1.32	0.476	0.484
Р	0.95	1.05	0.037	0.041
P0	3.9	4.1	0.153	0.161
P1		1.6		0.063
W	7.9	8.3	0.311	0.327

SPLV2.8 Series