19-3855; Rev 1; 4/06

# 2-/4-/6-/8-Channel, ±30kV ESD Protectors in µDFN



## General Description

The MAX13202E/MAX13204E/MAX13206E/MAX13208E low-capacitance ±30kV ESD-protection diode arrays are designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steer ESD current pulses to $V_{CC}$ or GND.

The MAX13202E/MAX13204E/MAX13206E/MAX13208E protect against ESD pulses up to ±15kV Human Body Model (HBM) and ±30kV Air-Gap Discharge, as specified in IEC 61000-4-2. These devices have a 6pF on-capacitance per channel, making them ideal for use on high-speed data I/O interfaces.

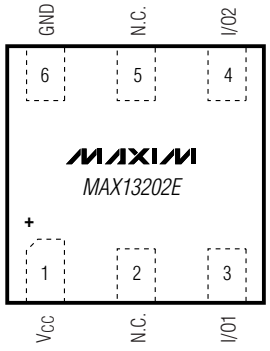
The MAX13204E is a quad-ESD structure designed for Ethernet and FireWire® applications. The MAX13202E/MAX13206E/MAX13208E are 2-channel, 6-channel, and 8-channel devices. They are designed for cell-phone connectors and SVGA video connections.

These devices are available in 6-, 8-, and 10-pin µDFN packages and are specified over the -40°C to +125°C automotive operating temperature range.

## Applications

| | |
|---|---|
| USB | Ethernet |
| USB 2.0 | Video |
| PDAs | Cell Phones |
| FireWire | |

## Pin Configurations




µDFN
(1mm x 1.5mm)

*Pin Configurations continued at end of data sheet.*

## Features

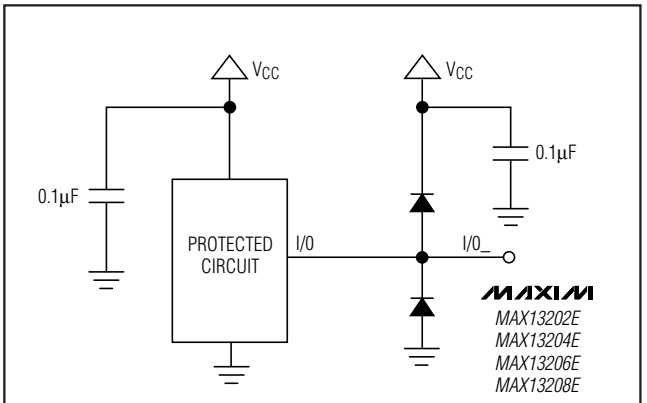
- **High-Speed Data-Line ESD Protection**
  - **±15kV—Human Body Model**
  - **±30kV—IEC 61000-4-2, Air-Gap Discharge**
- **Tiny µDFN Package**
  - **MAX13202E (1mm x 1.5mm)**
  - **MAX13204E (2mm x 2mm)**
  - **MAX13206E (2mm x 2mm)**
  - **MAX13208E (2mm x 2mm)**
- **Low 6pF Input Capacitance**
- **Low 1nA (max) Leakage Current**
- **+0.9V to +16V Supply Voltage Range**

## Ordering Information

| PART | PIN-PKG | PROTECTED I/O PORTS | TOP MARK | PKG CODE |
|---|---|---|---|---|
| **MAX13202EALT+** | 6 µDFN | 2 | BV | L611-1 |
| **MAX13204EALT+** | 6 µDFN | 4 | AAO | L622-1 |
| **MAX13206EALA+** | 8 µDFN | 6 | AAL | L822-1 |
| **MAX13208EALB+** | 10 µDFN | 8 | AAD | L1022-1 |

***Note:*** *All devices are specified over the -40°C to +125°C automotive operating temperature range.*
*+Denotes lead-free package*

## Typical Operating Circuit




*FireWire is a registered trademark of Apple Computer, Inc.*

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to GND .....-0.3V to +18V
I/O_ to GND .....-0.3V to ($V_{CC}$ + 0.3V)
Continuous Power Dissipation ($T_A$ = +70°C)
6-Pin, 1mm x 1.5mm µDFN (derate 2.1mW/°C above +70°C).....168mW
6-Pin, 2mm x 2mm µDFN (derate 4.5mW/°C above +70°C).....358mW
8-Pin, 2mm x 2mm µDFN (derate 4.8mW/°C above +70°C).....381mW
10-Pin, 2mm x 2mm µDFN (derate 5.0mW/°C above +70°C).....403mW

Operating Temperature Range .....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +5V ±5%, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$ = +5V and $T_A$ = +25°C.) (Note 1)

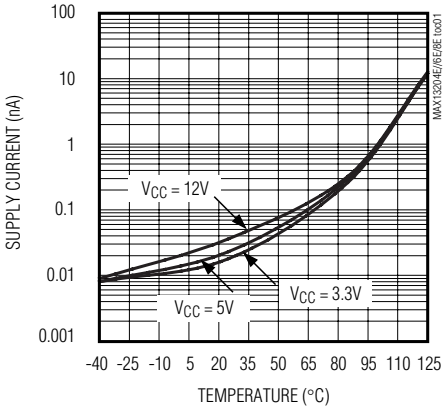
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | | 0.9 | | 16.0 | V |
| Supply Current | $I_{CC}$ | | | | 1 | 100 | nA |
| Diode Forward Voltage | $V_F$ | $I_F$ = 10mA | | 0.65 | | 0.95 | V |
| Channel Clamp Voltage (Note 2) | $V_C$ | $T_A$ = +25°C, ±15kV, Human Body Model, $I_F$ = 10A | Positive transients | | | $V_{CC}$ + 25 | V |
| | | | Negative transients | | | -25 | |
| | | $T_A$ = +25°C, ±14kV, Contact Discharge (IEC 61000-4-2), $I_F$ = 42A | Positive transients | | | $V_{CC}$ + 80 | |
| | | | Negative transients | | | -80 | |
| | | $T_A$ = +25°C, ±30kV, Air-Gap Discharge (IEC 61000-4-2), $I_F$ = 90A | Positive transients | | | $V_{CC}$ + 120 | |
| | | | Negative transients | | | -120 | |
| Channel Leakage Current (Note 3) | | $T_A$ = -40°C to +50°C | | -1 | | +1 | nA |
| | | $T_A$ = -40°C to +125°C | | -1 | | +1 | µA |
| Channel Input Capacitance | | $V_{CC}$ = 5V, bias of $V_{CC}$/2, f = 1MHz (Note 3) | | | 6 | 7 | pF |
| **ESD PROTECTION** | | | | | | | |
| Human Body Model | | | | | ±15 | | kV |
| IEC 61000-4-2 Contact Discharge | | MAX13204E/MAX13206E/MAX13208E | | | ±14 | | kV |
| | | MAX13202E | | | ±12 | | |
| IEC 61000-4-2 Air-Gap Discharge | | | | | ±30 | | kV |

**Note 1:** Limits over temperature are guaranteed by design, not production tested.
**Note 2:** Idealized clamp voltages (L1 = L2 = L3 = 0) (Figure 1); see the *Applications Information* section for more information.
**Note 3:** Guaranteed by design. Not production tested.

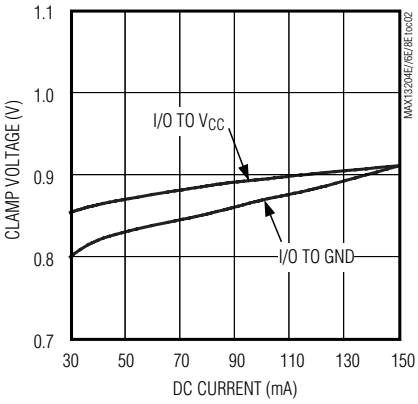
## Typical Operating Characteristics

($V_{CC}$ = +5V, $T_A$ = +25°C, unless otherwise noted.)

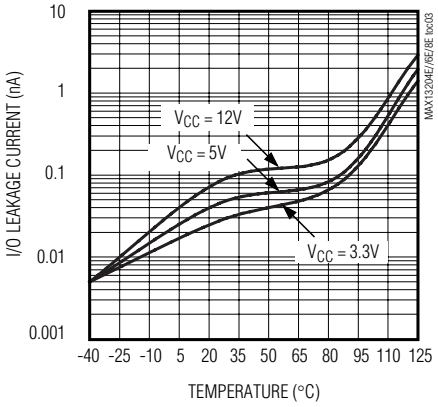
**SUPPLY CURRENT vs. TEMPERATURE**



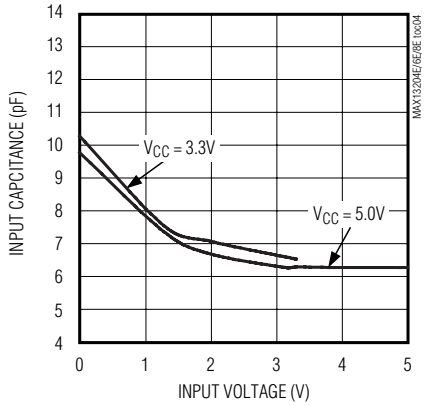

**CLAMP VOLTAGE vs. DC CURRENT**



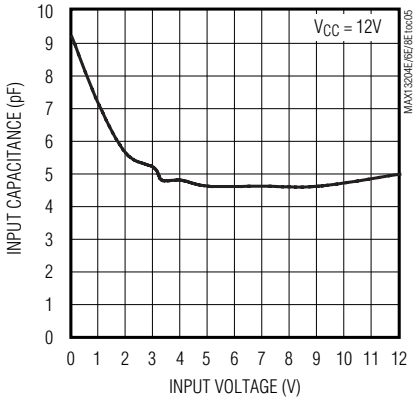

**I/O LEAKAGE CURRENT vs. TEMPERATURE**




**INPUT CAPACITANCE vs. INPUT VOLTAGE**




**INPUT CAPACITANCE vs. INPUT VOLTAGE**




## Pin Description

| PIN | | | | NAME | FUNCTION |
|---|---|---|---|---|---|
| MAX13202E | MAX13204E | MAX13206E | MAX13208E | | |
| 1 | 1 | 1 | 1 | $V_{CC}$ | Power-Supply Input. Bypass $V_{CC}$ to GND with a 0.1µF ceramic capacitor. Place the capacitor as close as possible to the device. |
| 2, 5 | — | — | — | N.C. | No Connection. Not internally connected. |
| 3, 4 | 2–5 | 2–7 | 2–9 | I/O_ | ESD-Protected Channel |
| 6 | 6 | 8 | 10 | GND | Ground |

## Detailed Description

The MAX13202E/MAX13204E/MAX13206E/MAX13208E are diode arrays designed to protect sensitive electronics against damage resulting from ESD conditions or transient voltages. The low input capacitance makes these devices ideal for high-speed data lines. The MAX13202E/MAX13204E/MAX13206E/MAX13208E protect two, four, six, and eight channels, respectively.

The MAX13202E/MAX13204E/MAX13206E/MAX13208E are designed to work in conjunction with a device's intrinsic ESD protection. The MAX13202E/MAX13204E/MAX13206E/MAX13208E limit the excursion of the ESD event to below ±25V peak voltage when subjected to the Human Body Model waveform. When subjected to the IEC 61000-4-2 waveform, the peak voltage is limited to ±80V (Contact Discharge) and ±120V (Air-Gap Discharge). The device that is being protected by the MAX13202E/MAX13204E/ MAX13206E/MAX13208E must be able to withstand these peak voltages plus any additional voltage generated by the parasitic board.

## Applications Information

### Design Considerations

Maximum protection against ESD damage results from proper board layout (see the *Layout Recommendations* section and Figure 2). A good layout reduces the parasitic series inductance on the ground line, supply line, and protected signal lines.

The MAX13202E/MAX13204E/MAX13206E/MAX13208E ESD diodes clamp the voltage on the protected lines during an ESD event and shunt the current to GND or $V_{CC}$. In an ideal circuit, the clamping voltage, $V_C$, is defined as the forward voltage drop, $V_F$, of the protection diode plus any supply voltage present on the cathode.

For positive ESD pulses:

$$V_C = V_{CC} + V_F$$

For negative ESD pulses:

$$V_C = -V_F$$

In reality, the effect of the parasitic series inductance on the lines must also be considered (Figure 1).

For positive ESD pulses:

$$V_C = V_{CC} + V_{F(D1)} + \left(L1 \times \frac{d(I_{ESD})}{dt}\right) + \left(L2 \times \frac{d(I_{ESD})}{dt}\right)$$

For negative ESD pulses:

$$V_C = -\left(V_{F(D2)} + \left(L1 \times \frac{d(I_{ESD})}{dt}\right) + \left(L3 \times \frac{d(I_{ESD})}{dt}\right)\right)$$

where $I_{ESD}$ is the ESD current pulse.

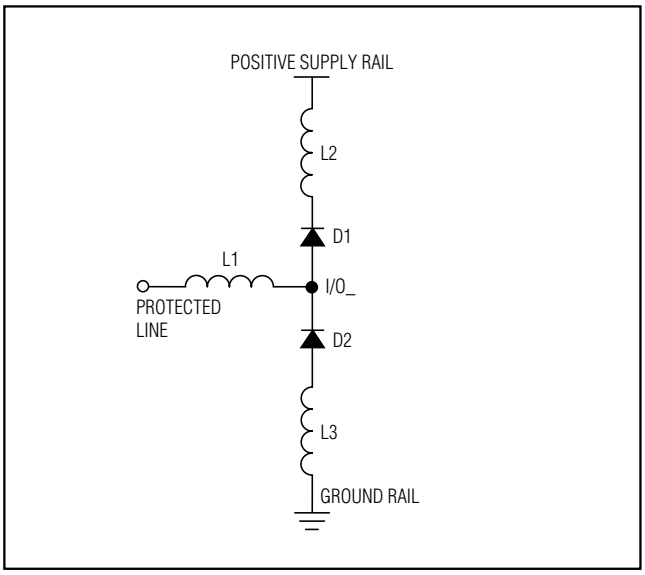



*Figure 1. Parasitic Series Inductance*

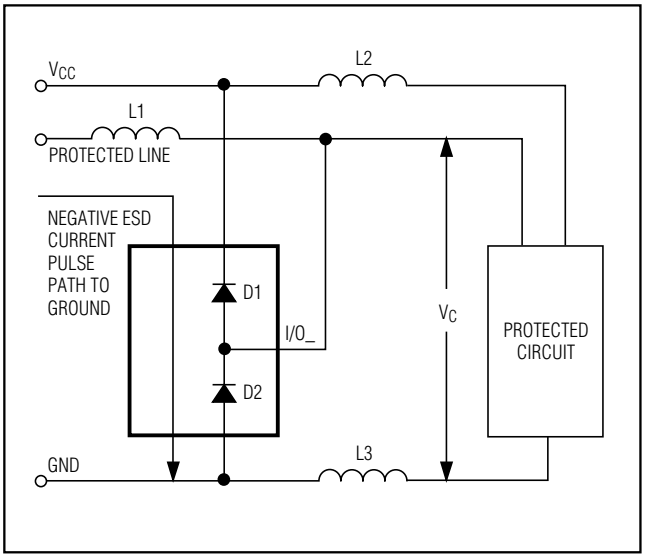



*Figure 2. Layout Considerations*

During an ESD event, the current pulse rises from zero to peak value in nanoseconds (Figure 3). For example, in a ±15kV IEC-61000-4-2 Air-Gap Discharge ESD event, the pulse current rises to approximately 45A in 1ns (di/dt = 45 x 10⁹). An inductance of only 10nH adds an additional 450V to the clamp voltage. An inductance of 10nH represents approximately 0.5in of board trace. Regardless of the device's specified diode clamp voltage, a poor layout with parasitic inductance significantly increases the effective clamp voltage at the protected signal line.

A low-ESR 0.1µF capacitor must be used between $V_{CC}$ and GND. This bypass capacitor absorbs the charge transferred by a +14kV (MAX13204E/MAX13206E/MAX13208E) and ±12kV (MAX13202E) IEC61000-4-2 Contact Discharge ESD event.

Ideally, the supply rail ($V_{CC}$) would absorb the charge caused by a positive ESD strike without changing its regulated value. In reality, all power supplies have an effective output impedance on their positive rails. If a power supply's effective output impedance is 1Ω, then by using V = I × R, the clamping voltage of $V_C$ increases by the equation $V_C = I_{ESD} \times R_{OUT}$. An ±8kV IEC 61000-4-2 ESD event generates a current spike of 24A, so the clamping voltage increases by $V_C$ = 24A × 1Ω, or $V_C$ = 24V. Again, a poor layout without proper bypassing increases the clamping voltage. A ceramic chip capacitor mounted as close to the MAX13202E/MAX13204E/MAX13206E/MAX13208E $V_{CC}$ pin is the best choice for this application. A bypass capacitor should also be placed as close to the protected device as possible.

### ±30kV ESD Protection

ESD protection can be tested in various ways. The MAX13202E/MAX13204E/MAX13206E/MAX13208E are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±14kV (MAX13204E/MAX13206E/MAX13208E) and ±12kV (MAX13202E) using the Contact Discharge method specified in IEC 61000-4-2
- ±30kV using the IEC 61000-4-2 Air-Gap Discharge method

### ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

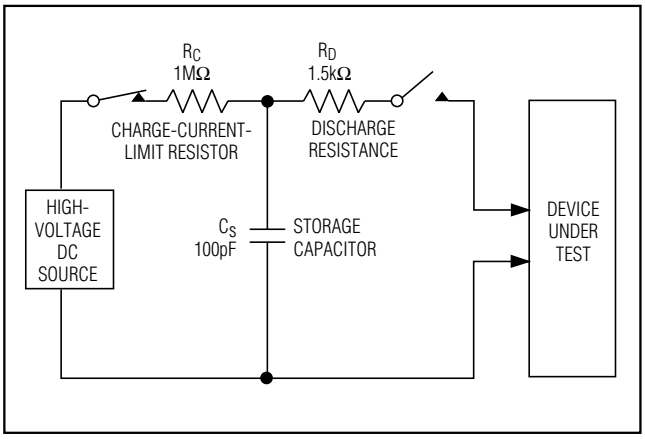



*Figure 4. Human Body ESD Test Model*

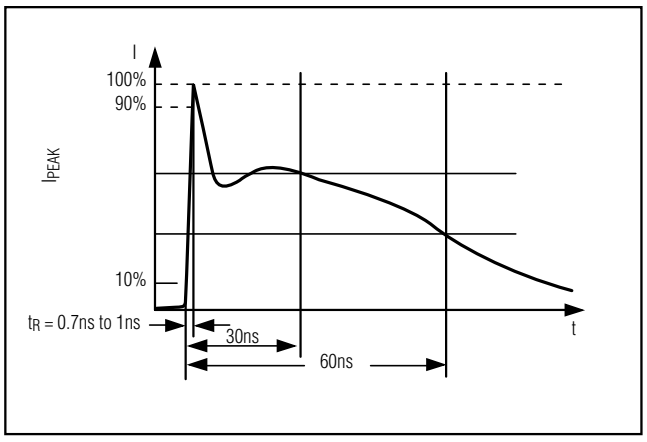



*Figure 3. IEC 61000-4-2 ESD Generator Current Waveform*

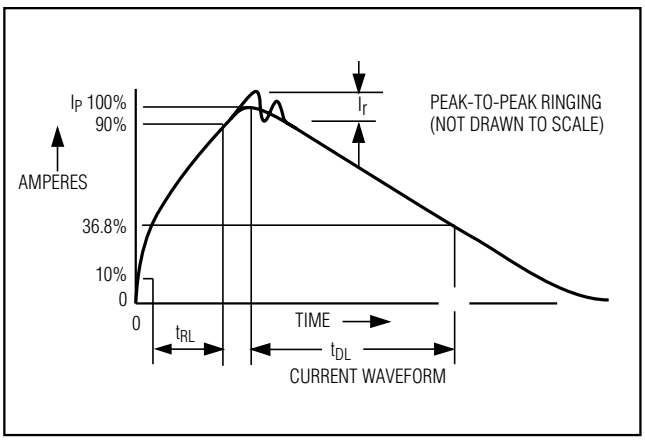



*Figure 5. Human Body Model Current Waveform*

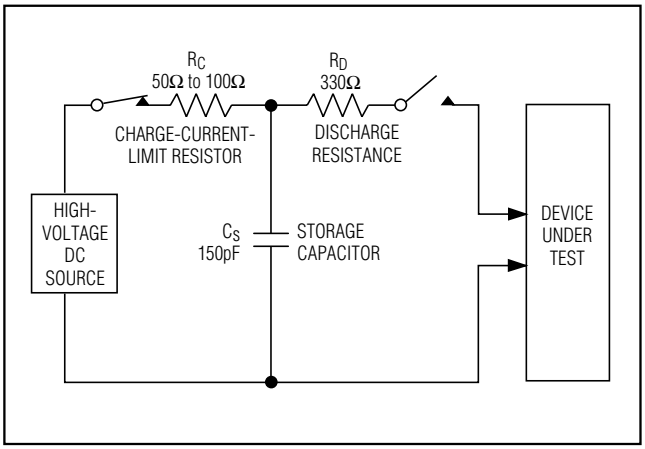



*Figure 6. IEC 61000-4-2 ESD Test Model*

### Human Body Model

Figure 4 shows the Human Body Model, and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

### IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The MAX13202E/MAX13204E/MAX13206E/MAX13208E help users design equipment that meets Level 4 of IEC 61000-4-2.

The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 6), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 3 shows the current waveform for the ±8kV IEC 61000-4-2 Level 4 ESD Contact Discharge test.

The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

### Layout Recommendations

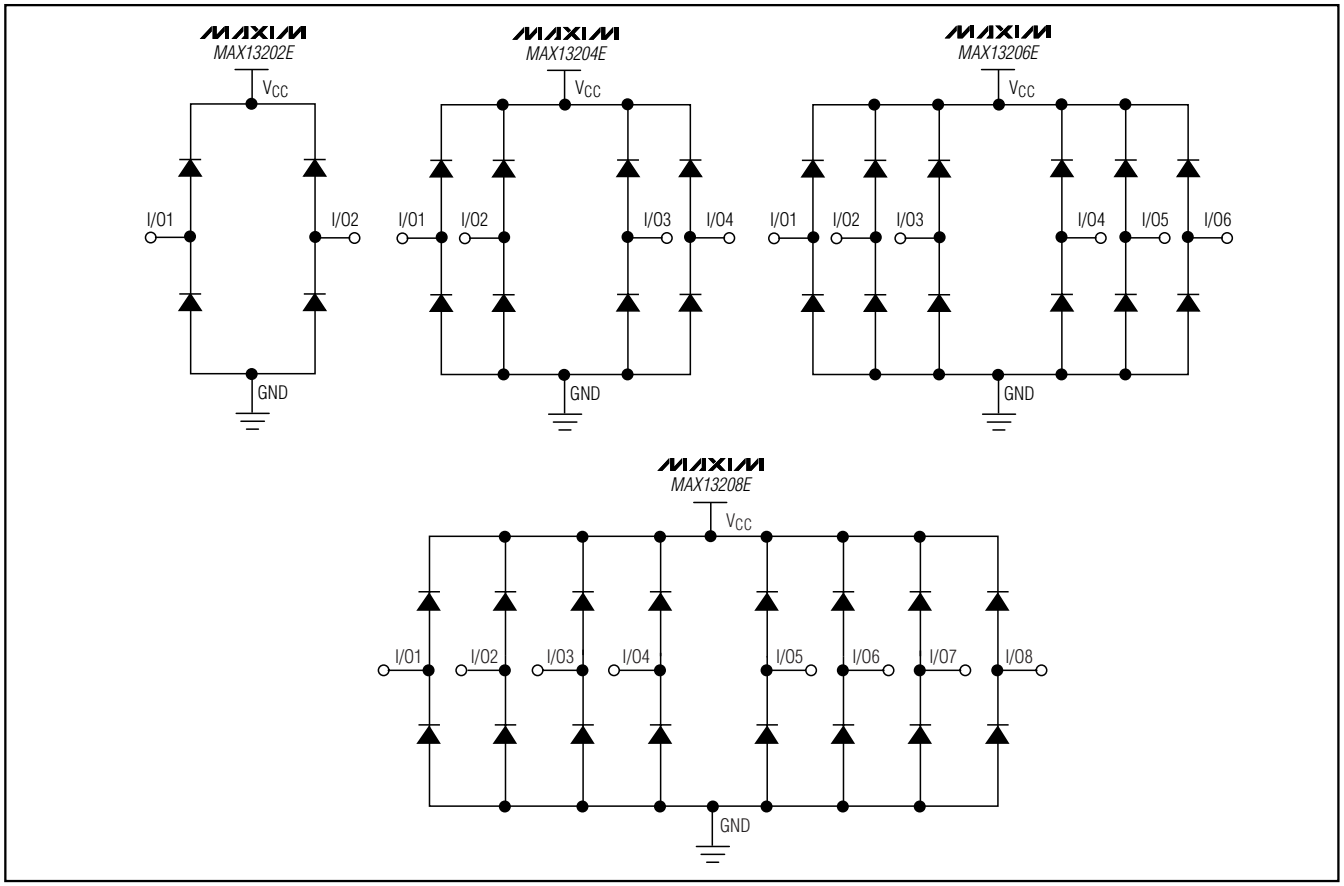
Proper circuit-board layout is critical to suppress ESD-induced line transients. The MAX13202E/MAX13204E/MAX13206E/MAX13208E clamp to ±120V; however, with improper layout, the voltage spike at the device is much higher. A lead inductance of 10nH with a 45A current spike at a dv/dt of 1ns results in an **ADDITIONAL** 450V spike on the protected line. It is **essential** that the layout of the PC board follows these guidelines:

1) Minimize trace length between the connector or input terminal, I/O_, and the protected signal line.
2) Use separate planes for power and ground to reduce parasitic inductance and to reduce the impedance to the power rails for shunted ESD current.
3) Ensure short ESD transient return paths to GND and $V_{CC}$.
4) Minimize conductive power and ground loops.
5) Do not place critical signals near the edge of the PC board.
6) Bypass $V_{CC}$ to GND with a low-ESR ceramic capacitor as close to $V_{CC}$ and ground terminals as possible.
7) Bypass the supply of the protected device to GND with a low-ESR ceramic capacitor as close to the supply pin as possible.

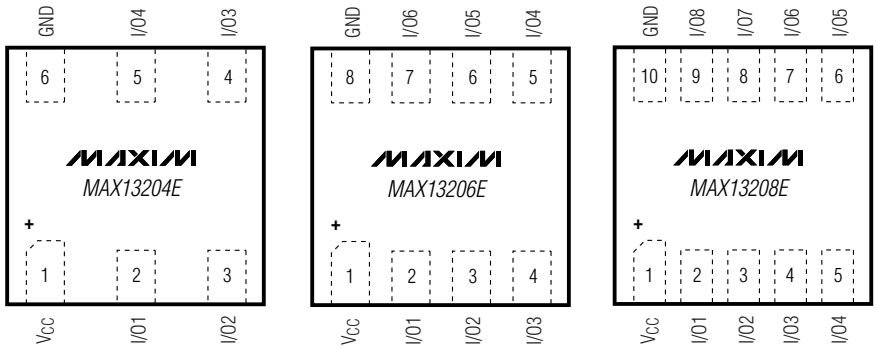
## Chip Information

PROCESS: BiCMOS

## Functional Diagrams




## Pin Configurations (continued)



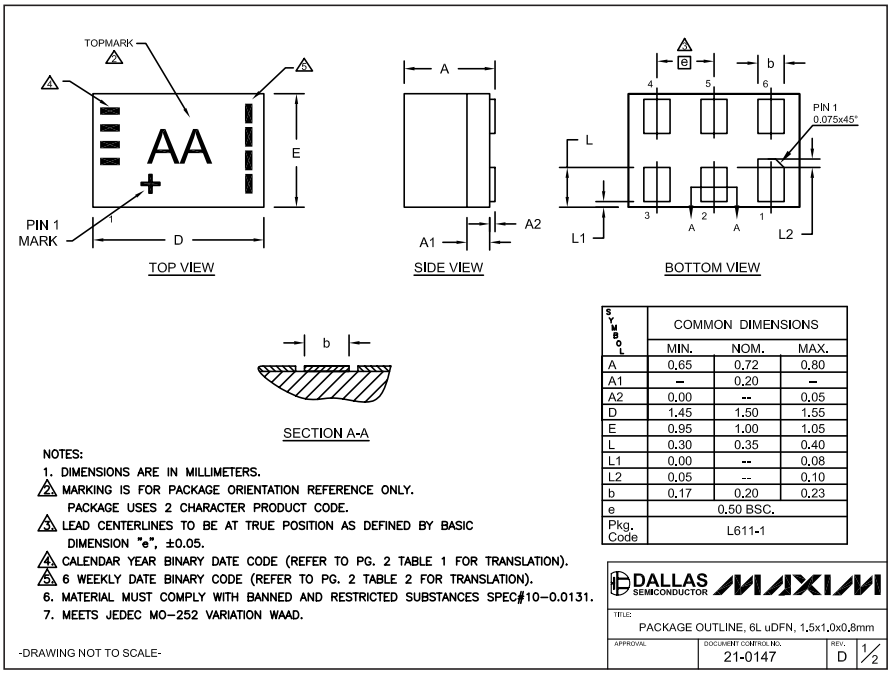

**6 µDFN (2mm x 2mm)**

**8 µDFN (2mm x 2mm)**

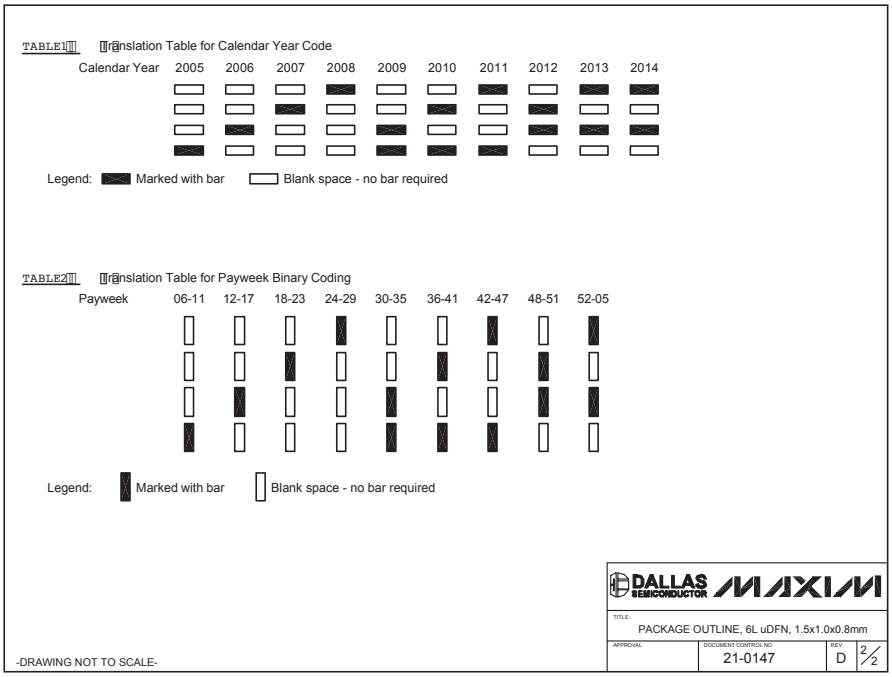
**10 µDFN (2mm x 2mm)**

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

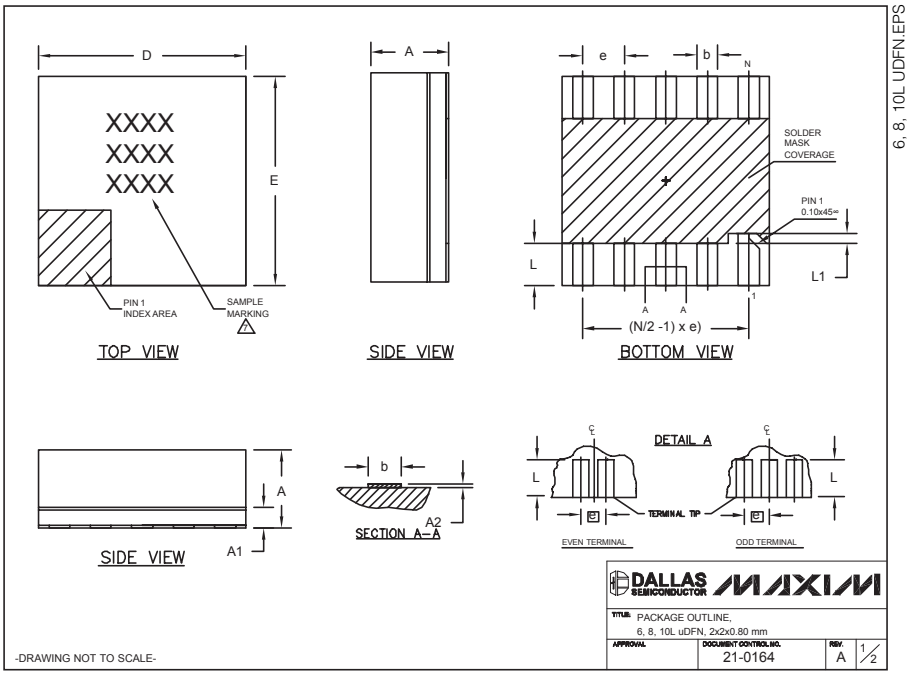



| SYMBOL | COMMON DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.65 | 0.72 | 0.80 |
| A1 | -- | 0.20 | -- |
| A2 | 0.00 | -- | 0.05 |
| D | 1.45 | 1.50 | 1.55 |
| E | 0.95 | 1.00 | 1.05 |
| L | 0.30 | 0.35 | 0.40 |
| L1 | 0.00 | -- | 0.08 |
| L2 | 0.05 | -- | 0.10 |
| b | 0.17 | 0.20 | 0.23 |
| e | 0.50 BSC. | | |
| Pkg. Code | L611-1 | | |



## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)




| COMMON DIMENSIONS | | | |
|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.15 | 0.20 | 0.25 |
| A2 | 0.020 | 0.025 | 0.035 |
| D | 1.95 | 2.00 | 2.05 |
| E | 1.95 | 2.00 | 2.05 |
| L | 0.30 | 0.40 | 0.50 |
| L1 | 0.10 REF. | | |

| PACKAGE VARIATIONS | | | | |
|---|---|---|---|---|
| PKG. CODE | N | e | b | (N/2 -1) x e |
| L622-1 | 6 | 0.65 BSC | 0.30±0.05 | 1.30 REF. |
| L822-1 | 8 | 0.50 BSC | 0.25±0.05 | 1.50 REF. |
| L1022-1 | 10 | 0.40 BSC | 0.20±0.03 | 1.60 REF. |

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. "N" IS THE TOTAL NUMBER OF LEADS.
6. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
7. ⚠ MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 6, 8, 10L uDFN, 2x2x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0164
REV. A
2/2

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