

# ESDALC6V1-1M2

## Single line low capacitance Transil<sup>™</sup> for ESD protection

### **Features**

- Single line low capacitance Transil diode
- Unidirectional ESD protection
- ESD protection > 30 kV (IEC 61000-4-2 contact discharge)
- Breakdown voltage V<sub>BR</sub> = 6.1 V min.
- Low diode capacitance (22 pF @ 0 V)
- Low leakage current (< 100 nA @ 3 V)
- Very small PCB area (0.6 mm<sup>2</sup>)
- RoHS compliant

### **Benefits**

- High ESD robustness of the equipment
- Suitable for high density boards

### Complies with the following standards:

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G Method 3015-7: class 3B
  - HBM (Human body model)

## **Applications**

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

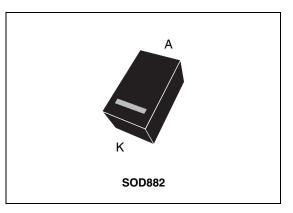
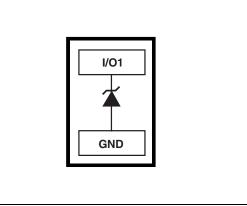


Figure 1. **Functional diagram** 



## **Description**

The ESDALC6V1-1M2 is a unidirectional single line TVS diode designed to protect the data lines or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

TM: Transil is a trademark of STMicroelectronics

## 1 Characteristics

| Symbol           | Parameter  | Value | Unit         |    |
|------------------|--|-------|--------------|----|
| V <sub>PP</sub>  | Peak pulse voltage - IEC 61000-4-2 contact discharge   | ±30   | kV           |    |
| P <sub>PP</sub>  | Peak pulse power dissipation (8/20 $\mu$ s) <sup>(1)</sup> $T_{j \text{ initial}} = T_{amb}$ | 50    | W            |    |
| I <sub>PP</sub>  | Peak pulse current (8/20 µs)   |       | 6            | А  |
| Тj               | Operating junction temperature range   |       | -40 to +125  | °C |
| T <sub>stg</sub> | Storage temperature range  |       | - 55 to +150 | °C |
| ΤL               | Maximum lead temperature for soldering during 10 s at 5 mm for                               | case  | 260          | °C |

### Table 1. Absolute maximum ratings ( $T_{amb} = 25 \text{ °C}$ )

1. For a surge greater than the maximum values, the diode will fail in short-circuit

#### Figure 2. Electrical characteristics (definitions)

| Sy              | mbol | Parameter                         | ' <b>≜</b> ,                          |
|-----------------|------|-----------------------------------|---------------------------------------|
| V <sub>B</sub>  | в =  | Breakdown voltage                 |                                       |
| I <sub>BM</sub> |      | Leakage current @ V <sub>BM</sub> | I                                     |
| V <sub>R</sub>  | м =  | Stand-off voltage                 |                                       |
| V <sub>c</sub>  |      | Clamping voltage                  |                                       |
| R <sub>d</sub>  |      | Dynamic impedance                 |                                       |
| I <sub>PP</sub> |      | Peak pulse current                |                                       |
| I <sub>B</sub>  | =    | Breakdown current                 |                                       |
| άΤ              | . =  | Voltage temperature coefficient   |                                       |
| V <sub>F</sub>  | =    | Forward voltage drop              | jSlope = 1/Rd                         |
|                 |      |                                   | ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ |

| Table 2. | Electrical | characteristics | (T <sub>amb</sub> = 25 °C) |
|----------|------------|-----------------|----------------------------|
|----------|------------|-----------------|----------------------------|

| Order code    | V <sub>BR</sub> @ I <sub>R</sub> |      | I <sub>RM</sub> @ V <sub>RM</sub> |        | V <sub>F</sub> @ 10 mA | αΤ | C @ 0 V     |        |
|---------------|----------------------------------|------|-----------------------------------|--------|------------------------|----|-------------|--------|
| Order code    | Vmin                             | Vmax | mA                                | nA max | v                      | V  | 10-4/°C max | pF typ |
| ESDALC6V1-1M2 | 6.1                              | 7.2  | 1                                 | 100    | 3                      | 1  | 4.5         | 22     |

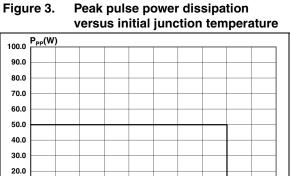


10.0

0.0

25

50

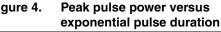


#### Peak pulse power dissipation Figure 4.

T<sub>j</sub>(°C)

150

125



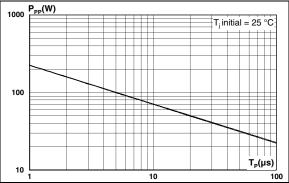


Figure 5. Clamping voltage versus peak pulse current (typical values)

75

100

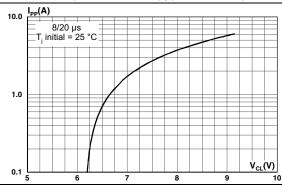
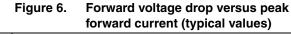
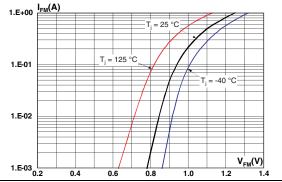
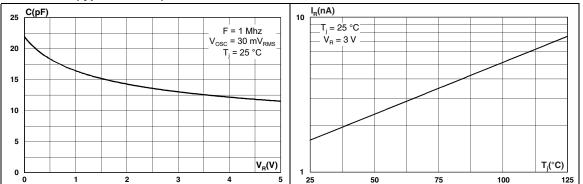


Figure 7. Junction capacitance versus reverse voltage applied (typical values)



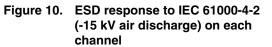


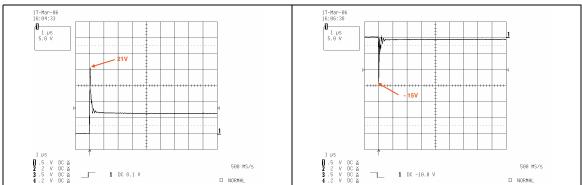
Leakage current versus junction Figure 8. temperature (typical values)



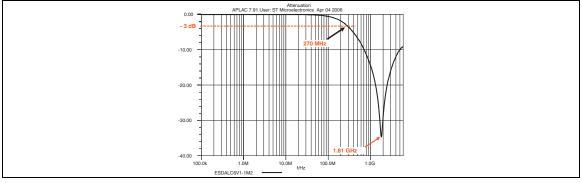
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#### Figure 9. ESD response to IEC 61000-4-2 (+15 kV air discharge) on each channel



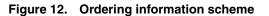


#### Figure 11. S21 attenuation





# 2 Ordering information scheme



|                     | ESDA LC 6V1 - 1 M2 |
|---------------------|--------------------|
|                     |                    |
| ESD Array           |                    |
| Low Capacitance     |                    |
| Breakdown Voltage   |                    |
| 6V1 = 6.1 Volts min |                    |
| Number of line      |                    |
| Package             |                    |
| M2 = SOD882         |                    |

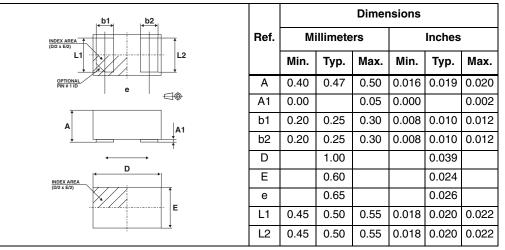


## 3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: <u>www.st.com</u>. ECOPACK<sup>®</sup> is an ST trademark.

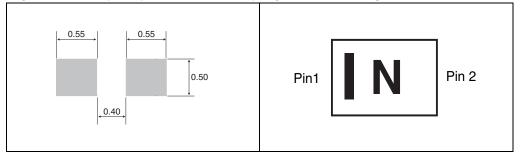
Table 3. SOD882 dimensions



Note:

Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 13. Footprint (dimensions in mm) Figure 14. Marking





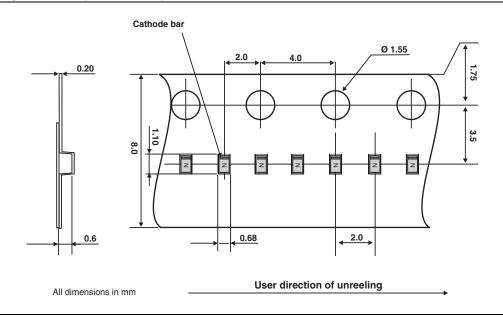


Figure 15. Tape and reel specifications

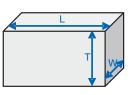


### 4 Recommendation on PCB assembly

### 4.1 Stencil opening design

- 1. General recommendation on stencil opening design
  - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

#### Figure 16. Stencil opening dimensions



b) General design rule

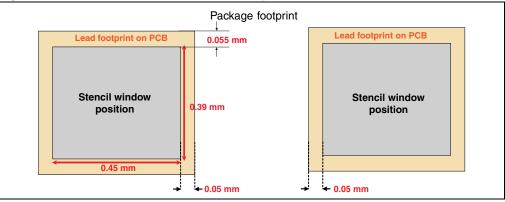
Stencil thickness (T) = 75 ~ 125  $\mu$ m

Aspect Ratio = 
$$\frac{W}{T} \ge 1.5$$

Aspect Area = 
$$\frac{L \times W}{2T(L + W)} \ge 0.66$$

- 2. Reference design
  - a) Stencil opening thickness: 100 µm
  - b) Stencil opening for leads: Opening to footprint ratio between 60% and 65%.

#### Figure 17. Recommended stencil windows position



### 4.2 Solder paste

- 1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
- 2. "No clean" solder paste is recommended.
- 3. Offers a high tack force to resist component movement during high speed.
- 4. Solder paste with fine particles: powder particle size is 20-45 μm.



### 4.3 Placement

- 1. Manual positioning is not recommended.
- 2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
- 3. Standard tolerance of ± 0.05 mm is recommended.
- 4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
- 5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
- 6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

### 4.4 PCB design preference

- 1. To control the solder paste amount, the closed via is recommended instead of open vias.
- 2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

### 4.5 **Reflow profile**

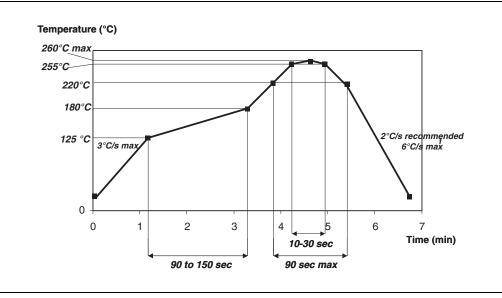


Figure 18. ST ECOPACK® recommended soldering reflow profile for PCB mounting

Note:

Minimize air convection currents in the reflow oven to avoid component movement.



# 5 Ordering information

#### Table 4. Ordering information

| Order code    | Marking          | Package | Weight  | Base qty | Delivery mode |
|---------------|------------------|---------|---------|----------|---------------|
| ESDALC6V1-1M2 | N <sup>(1)</sup> | SOD882  | 0.92 mg | 12000    | Tape and reel |

1. The marking can be rotated by multiples of  $90^\circ$  to differentiate assembly location

# 6 Revision history

#### Table 5.Document revision history

| Date        | Revision | Changes   |  |  |
|-------------|----------|---|--|--|
| 23-May-2006 | 1        | Initial release   |  |  |
| 16-Jun-2006 | 2        | Updated tape and reel illustration (Figure 15).   |  |  |
| 11-Oct-2006 | 3        | Corrected formatting errors on page 1. No technical changes.  |  |  |
| 10-May-2007 | 4        | Updated <i>Functional diagram</i> to single diode. Added <i>Section 4: Recommendation on PCB assembly</i> .   |  |  |
| 26-Nov-2007 | 5        | Corrected 2: Ordering information scheme. Updated Figure 15: Tape<br>and reel specifications. Added Figure 17: Recommended stencil<br>windows position. Reformatted to current standards. |  |  |
| 02-Nov-2010 | 6        | Updated <i>Table 1</i> , <i>Table 2</i> , base quantity change on <i>Table 4</i> and updated graphics.  |  |  |



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