NOT RECOMMENDED FOR NEW DESIGNS
POSSIBLE SUBSTITUTE PRODUCT
CA3127, HFA3127

April 2002 FN1345.6

## High-Frequency NPN Transistor Array For Low-Power Applications at Frequencies Up to 1.5GHz

The CA3227 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Each of the transistors exhibits a value of $f_T$ in excess of 3GHz, making them useful from DC to 1.5GHz. The monolithic construction of these devices provides close electrical and thermal matching of the five transistors.

## Ordering Information

| PART NUMBER (BRAND) | TEMP. RANGE ($^oC$) | PACKAGE | PKG. NO. |
|---|---|---|---|
| CA3227M (3227) | -55 to 125 | 16 Ld SOIC | M16.15 |
| CA3227M96 (3227) | -55 to 125 | 16 Ld SOIC Tape and Reel | M16.15 |

## Features

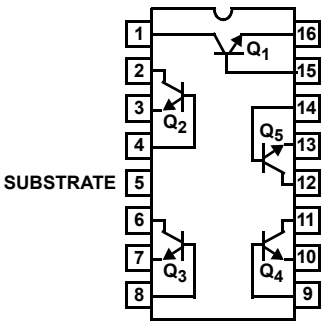
- Gain-Bandwidth Product ($f_T$) . . . . . >3GHz
- Five Transistors on a Common Substrate

## Applications

- VHF Amplifiers
- VHF Mixers
- Multifunction Combinations - RF/Mixer/Oscillator
- IF Converter
- IF Amplifiers
- Sense Amplifiers
- Synthesizers
- Synchronous Detectors
- Cascade Amplifiers

## Pinout

**CA3227 (SOIC)**
TOP VIEW



## Absolute Maximum Ratings

Collector to Emitter Voltage ($V_{CEO}$) . . . . . 8V
Collector to Base Voltage ($V_{CBO}$) . . . . . 12V
Collector to Substrate Voltage ($V_{CIO}$, Note 1) . . . . . 20V
Collector Current ($I_C$) . . . . . 20mA

## Operating Conditions

Temperature Range . . . . . -55°C to 125°C

## Thermal Information

| Thermal Resistance (Typical, Note 2) | $\theta_{JA}$ (°C/W) |
|---|---|
| 16 Ld SOIC Package | 185 |

Maximum Power Dissipation (Any One Transistor) . . . . . 85mW
Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. The collector of each transistor of these devices is isolated from the substrate by an integral diode. The substrate (Terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. $\theta_{JA}$ is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Electrical Specifications $T_A = 25°C$

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS FOR EACH TRANSISTOR** | | | | | | | |
| Collector to Base Breakdown Voltage | $V_{(BR)CBO}$ | $I_C = 10\mu A$, $I_E = 0$ | | 12 | 20 | - | V |
| Collector to Emitter Breakdown Voltage | $V_{(BR)CEO}$ | $I_C = 1mA$, $I_B = 0$ | | 8 | 10 | - | V |
| Collector to Substrate Breakdown Voltage | $V_{(BR)CIO}$ | $I_{C1} = 10\mu A$, $I_B = 0$, $I_E = 0$ | | 20 | - | - | V |
| Emitter Cutoff Current (Note 3) | $I_{EBO}$ | $V_{EB} = 4.5V$, $I_C = 0$ | | - | - | 10 | µA |
| Collector Cutoff Current | $I_{CEO}$ | $V_{CE} = 5V$, $I_B = 0$ | | - | - | 1 | µA |
| Collector Cutoff Current | $I_{CBO}$ | $V_{CB} = 8V$, $I_E = 0$ | | - | - | 100 | nA |
| DC Forward Current Transfer Ratio | $h_{FE}$ | $V_{CE} = 6V$ | $I_C = 10mA$ | - | 110 | - | |
| | | | $I_C = 1mA$ | 40 | 150 | - | |
| | | | $I_C = 0.1mA$ | - | 150 | - | |
| Base to Emitter Voltage | $V_{BE}$ | $V_{CE} = 6V$ | $I_C = 1mA$ | 0.62 | 0.71 | 0.82 | V |
| Collector to Emitter Saturation Voltage | $V_{CE\ SAT}$ | $I_C = 10mA$, $I_B = 1mA$ | | - | 0.13 | 0.50 | V |
| Base to Emitter Saturation Voltage | $V_{BE\ SAT}$ | $I_C = 10mA$, $I_B = 1mA$ | | 0.74 | - | 0.94 | V |

NOTE:

3. On small-geometry, high-frequency transistors, it is very good practice never to take the Emitter Base Junction into reverse breakdown. To do so may permanently degrade the $h_{FE}$. Hence, the use of $I_{EBO}$ rather than $V_{(BR)EBO}$. These devices are also susceptible to damage by electrostatic discharge and transients in the circuits in which they are used. Moreover, CMOS handling procedures should be employed.

## Electrical Specifications $T_A = 25^oC$, 200MHz, Common Emitter, Typical Values Intended Only for Design Guidance

| PARAMETER | SYMBOL | | TEST CONDITIONS | TYPICAL VALUES | UNITS |
|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR** | | | | | |
| Input Admittance | $Y_{11}$ | $b_{11}$ | $I_C$ = 1mA, $V_{CE}$ = 5V | 4 | mS |
| | | $g_{11}$ | | 0.75 | mS |
| Output Admittance | $Y_{22}$ | $b_{22}$ | $I_C$ = 1mA, $V_{CE}$ = 5V | 2.7 | mS |
| | | $g_{22}$ | | 0.13 | mS |
| Forward Transfer Admittance | $Y_{21}$ | $Y_{21}$ | $I_C$ = 1mA, $V_{CE}$ = 5V | 29.3 | mS |
| | | $\theta_{21}$ | | -33 | Degrees |
| Reverse Transfer Admittance | $Y_{12}$ | $Y_{12}$ | $I_C$ = 1mA, $V_{CE}$ = 5V | 0.38 | mS |
| | | $\theta_{12}$ | | -97 | Degrees |
| Input Admittance | $Y_{11}$ | $b_{11}$ | $I_C$ = 10mA, $V_{CE}$ = 5V | 4.8 | mS |
| | | $g_{11}$ | | 2.85 | mS |
| Output Admittance | $Y_{22}$ | $b_{22}$ | $I_C$ = 10mA, $V_{CE}$ = 5V | 2.75 | mS |
| | | $g_{22}$ | | 0.9 | mS |
| Forward Transfer Admittance | $Y_{21}$ | $Y_{21}$ | $I_C$ = 10mA, $V_{CE}$ = 5V | 95 | mS |
| | | $\theta_{21}$ | | -62 | Degrees |
| Reverse Transfer Admittance | $Y_{12}$ | $Y_{12}$ | $I_C$ = 10mA, $V_{CE}$ = 5V | 0.39 | mS |
| | | $\theta_{12}$ | | -97 | Degrees |
| Small Signal Forward Current Transfer Ratio | $h_{21}$ | | $I_C$ = 1mA, $V_{CE}$ = 5V | 7.1 | |
| | | | $I_C$ = 10mA, $V_{CE}$ = 5V | 17 | |
| **TYPICAL CAPACITANCE AT 1MHz, THREE-TERMINAL MEASUREMENT** | | | | | |
| Collector to Base Capacitance | $C_{CB}$ | | $V_{CB}$ = 6V | 0.3 | pF |
| Collector to Substrate Capacitance | $C_{CI}$ | | $V_{CI}$ = 6V | 1.6 | pF |
| Collector to Emitter Capacitance | $C_{CE}$ | | $V_{CE}$ = 6V | 0.4 | pF |
| Emitter to Base Capacitance | $C_{EB}$ | | $V_{EB}$ = 3V | 0.75 | pF |

## Spice Model (Spice 2G.6)

.model NPN

| | | | | |
|---|---|---|---|---|
| + | BF = 2.610E + 02 | BR = 4.401E + 00 | IS = 6.930E - 16 | RB = 130.0E + 00 |
| + | RC = 1.000E + 01 | RE = 7.396E - 01 | VA = 6.300E + 01 | VB = 2.208E + 00 |
| + | IK = 1.000E - 01 | ISE = 1.87E - 14 | NE = 1.653E + 00 | IKR = 1.000E - 02 |
| + | ISC = 9.25E - 14 | NC = 1.333E + 00 | TF = 1.775E - 11 | TR = 1.000E - 09 |
| + | CJS = 1.800E - 12 | CJE = 1.010E - 12 | PE = 8.350E - 01 | ME = 4.460E - 01 |
| + | CJC = 9.100E - 13 | PC = 3.850E - 01 | MC = 2.740E - 01 | KF = 0.000E + 00 |
| + | AF = 1.000E + 00 | EF = 1.000E + 00 | FC = 5.000E - 01 | PJS = 5.410E - 01 |
| + | MJS = 3.530E - 01 | RBM = 30.00 | RBV = 100 | IRB = 0.00 |

Please Note: No measurements have been made to model the reverse AC operation (tr is an estimation).

## Typical Performance Curves

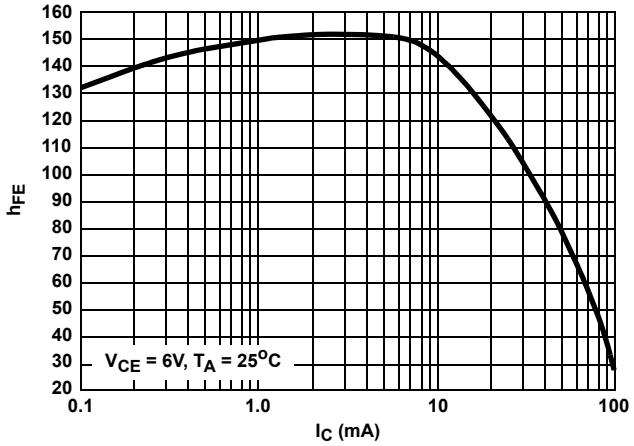



FIGURE 1. $h_{FE}$ vs COLLECTOR CURRENT

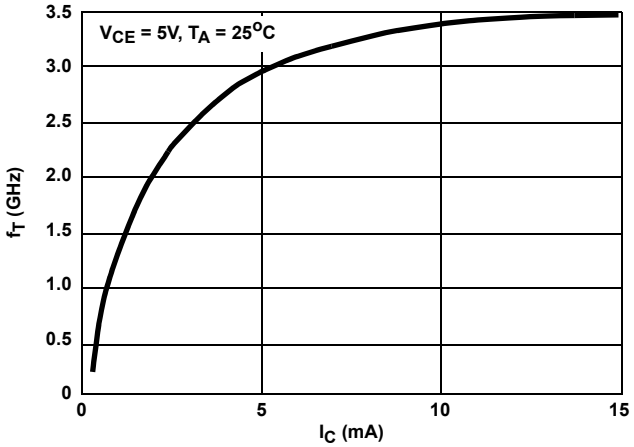



FIGURE 2. $f_T$ vs COLLECTOR CURRENT

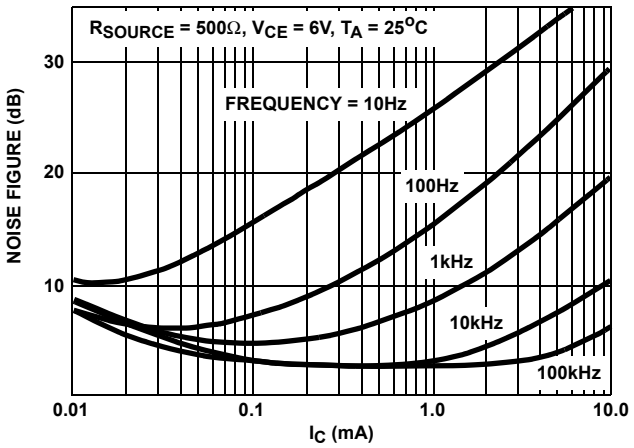



FIGURE 3. NOISE FIGURE vs COLLECTOR CURRENT

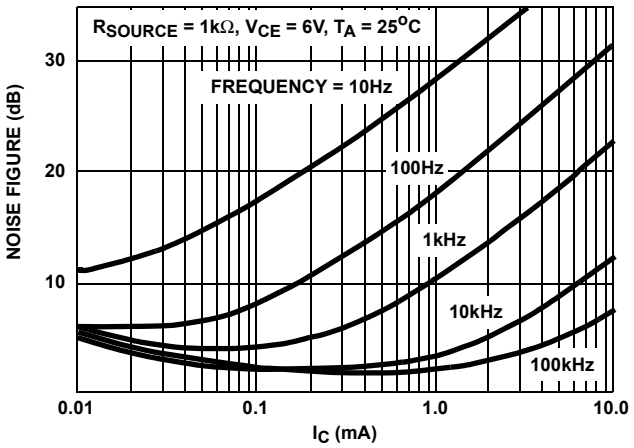



FIGURE 4. NOISE FIGURE vs COLLECTOR CURRENT

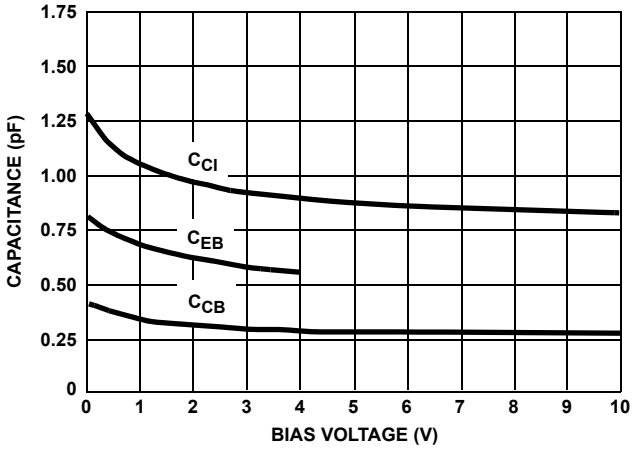



FIGURE 5. CAPACITANCE vs BIAS VOLTAGE

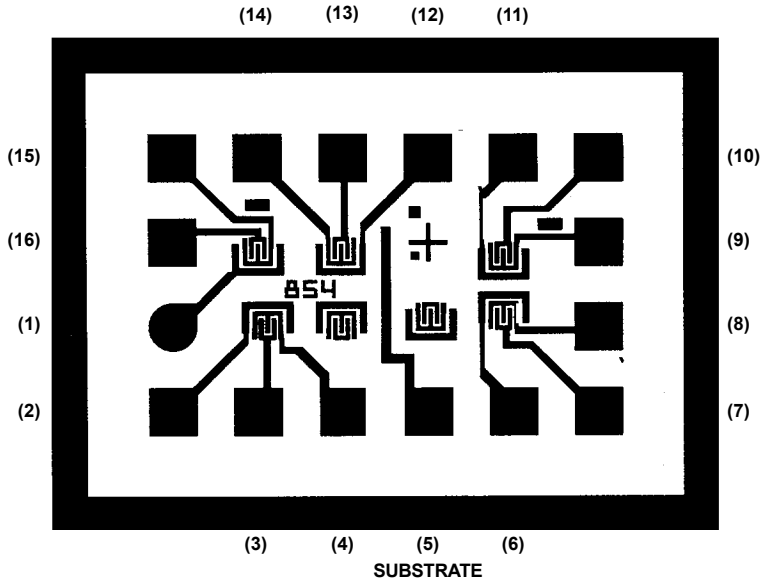
## Die Characteristics

**DIE DIMENSIONS:**

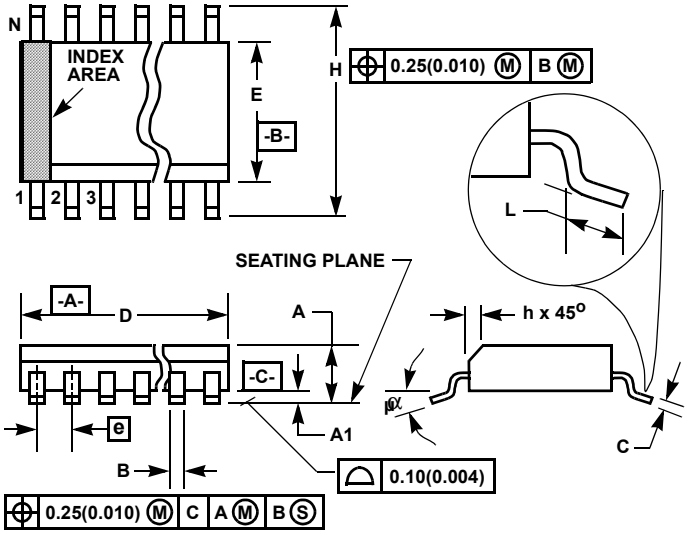
46 mils x 32 mils

## Metallization Mask Layout

**CA3227**



## Small Outline Plastic Packages (SOIC)




NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**M16.15 (JEDEC MS-012-AC ISSUE C)**
**16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.3859 | 0.3937 | 9.80 | 10.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 16 | | 16 | | 7 |
| α | $0^o$ | $8^o$ | $0^o$ | $8^o$ | - |

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