15MHz, BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output

CA5130A and CA5130 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. They are designed and guaranteed to operate in microprocessors or logic systems that use +5V supplies.

Gate protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

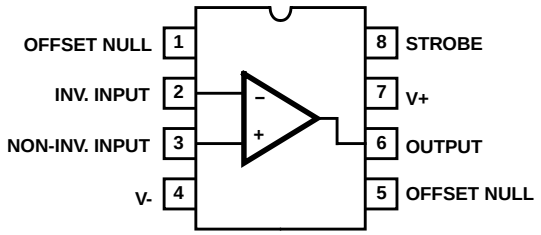
A complementary symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5130 Series circuits operate at supply voltages ranging from 4V to 16V, or ±2V to ±8V when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA5130A, CA5130 have guaranteed specifications for 5V operation over the full military temperature range of -55^{o}C to 125^{o}C.

Pinout

CA5130 (PDIP)
TOP VIEW



Features

- MOSFET Input Stage
  - Very High Z_I . . . . . 1.5TΩ (1.5 x 10^{12}Ω) (Typ)
  - Very Low I_I . . . . . 5pA (Typ) at 15V Operation
    2pA (Typ) at 5V Operation
- Ideal for Single Supply Applications
- Common Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can Be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5130A, CA5130 Have Full Military Temperature Range Guaranteed Specifications for V+ = 5V
- CA5130A, CA5130 Are Guaranteed to Operate Down to V+ = 4.5V for A_{OL}
- CA5130A, CA5130 Are Guaranteed to Operate at ±7.5V CA3130A, CA3130 Specifications

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- High Input Impedance Comparators (Ideal Interface with Digital CMOS)
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g., Follower for Single-Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to 0V)
- Peak Detectors
- Single Supply Full Wave Precision Rectifiers
- Photo Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

Part Number Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA5130AE	-55 to 125	8 Ld PDIP	E8.3
CA5130E	-55 to 125	8 Ld PDIP	E8.3

Absolute Maximum Ratings

Supply Voltage (V+ to V-) 16V
DC Input Voltage . . . . . (V+ +8V) to (V- -0.5V)
Differential Input Voltage 8V
Input Terminal Current 1mA
Output Short-Circuit Duration (Note 1) . . . . . Indefinite

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (^{O}C/W)	θ_{JC} (^{O}C/W)
PDIP Package	120	N/A

Maximum Junction Temperature (Plastic Package) . . . . . 150^{O}C
Maximum Storage Temperature Range . . . . . -65^{O}C to 150^{O}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{O}C

Operating Conditions

Temperature Range . . . . . -55^{O}C to 125^{O}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^{O}$C, V+ = 5V, V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA5130			CA5130A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	2	10	-	1.5	4	mV
Input Offset Current	I_{IO}	V_O = 2.5V	-	0.1	10	-	0.1	5	pA
Input Current	I_I	V_O = 2.5V	-	2	15	-	2	10	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0V to 1V	70	85	-	75	87	-	dB
		V_{CM} = 0V to 2.5V	60	69	-	60	69	-	dB
Input Common Mode Voltage Range	V_{ICR}+		2.5	2.8	-	2.5	2.8	-	V
	V_{ICR}-		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	Δ+ = 1V; Δ- = 1V	55	73	-	60	75	-	dB
Large Signal Voltage Gain (Note 3)	A_{OL}	V_O = 0.1V to 4.1V, R_L = ∞	95	105	-	100	105	-	dB
		V_O = 0.1V to 3.6V, R_L = 10kΩ	85	95	-	90	97	-	dB
Source Current	I_{SOURCE}	V_O = 0V	1.0	2.6	4.0	1.0	3.1	4.0	mA
Sink Current	I_{SINK}	V_O = 5V	1.0	1.7	4.0	1.0	1.4	4.0	mA
Output Voltage	V_{OUT}								
V_{OM}+		R_L = ∞	4.99	5	-	4.99	5	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
V_{OM}+		R_L = 10kΩ	4.4	4.7	-	4.4	4.7	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
V_{OM}+		R_L = 2kΩ	2.5	3.5	-	2.5	3.5	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
Supply Current	I_{SUPPLY}	V_O = 0V	-	50	100	-	50	100	μA
		V_O = 2.5V	-	260	400	-	260	400	μA

NOTE:

3. For V+ = 4.5V and V- = GND; V_{OUT} = 0.5V to 3.2V at R_L = 10kΩ.

Electrical Specifications T_A = -55°C to 125°C, V+ = 5V, V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA5130			CA5130A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	3	15	-	2	10	mV
Input Offset Current	I_{IO}	V_O = 2.5V	-	0.1	10	-	0.1	5	nA
Input Current	I_I	V_O = 2.5V	-	2	15	-	2	10	nA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0V to 1V	60	80	-	60	80	-	dB
		V_{CM} = 0V to 2.5V	50	80	-	55	80	-	dB
Input Common Mode Voltage Range	V_{ICR}+		2.5	2.8	-	2.5	2.8	-	V
	V_{ICR}-		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	Δ+ = 1V; Δ- = 1V	40	66	-	45	70	-	dB
Large Signal Voltage Gain (Note 4)	A_{OL}	V_O = 0.1V to 4.1V, R_L = ∞	90	98	-	94	98	-	dB
		V_O = 0.1V to 3.6V, R_L = 10kΩ	75	85	-	80	88	-	dB
Source Current	I_{SOURCE}	V_O = 0V	0.6	-	5.0	0.6	2.2	5.0	mA
Sink Current	I_{SINK}	V_O = 5V	0.6	-	5.0	0.6	1.15	5.0	mA
Output Voltage	V_{OUT}								
V_{OM}+		R_L = ∞	4.99	5	-	4.99	5	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
V_{OM}+		R_L = 10kΩ	4.0	4.6	-	4.0	4.6	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
V_{OM}+		R_L = 2kΩ	2.0	3.0	-	2.0	3.0	-	V
V_{OM}-			-	0	0.01	-	0	0.01	V
Supply Current	I_{SUPPLY}	V_O = 0V	-	80	220	-	80	220	µA
		V_O = 2.5V	-	300	500	-	300	500	µA

NOTE:

4. For V+ = 4.5V and V- = GND; V_{OUT} = 0.5V to 3.2V at R_L = 10kΩ.

Electrical Specifications T_A = 25°C, V+ = 15V, V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA5130			CA5130A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V± = ±7.5V	-	8	15	-	2	5	mV
Input Offset Current	I_{IO}	V± = ±7.5V	-	0.5	30	-	0.5	20	pA
Input Current	I_I	V± = ±7.5V	-	5	50	-	5	30	pA
Common Mode Rejection Ratio	CMRR		70	90	-	80	90	-	dB
Input Common Mode Voltage Range	V_{ICR}		10	-0.5 to 12	0	10	-0.5 to 12	0	V
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V\pm$, V± = ±7.5V	-	32	320	-	32	150	µV/V
Large Signal Voltage Gain	A_{OL}	V_O = 10V_{P-P}, R_L = 2kΩ	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB

Electrical Specifications $T_A = 25^oC$, V+ = 15V, V- = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	CA5130			CA5130A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Output Current									
Source	$I_{OM}+$	V_O = 0V	12	22	45	12	22	45	mA
Sink	$I_{OM}-$	V_O = 15V	12	20	45	12	20	45	mA
Supply Current	I_{SUPPLY}	V_O = 7.5V, $R_L = \infty$	-	10	15	-	10	15	mA
		V_O = 0V, $R_L = \infty$	-	2	3	-	2	3	mA
Maximum Output Voltage	V_{OUT}								
$V_{OM}+$		$R_L = \infty$	14.99	15	-	14.99	15	-	V
$V_{OM}-$			-	0	0.01	-	0	0.01	V
$V_{OM}+$		R_L = 2kΩ	12	13.3	-	12	13.3	-	V
$V_{OM}-$			-	0.002	0.01	-	0.002	0.01	V
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	10	-	-	10	-	$\mu V/^oC$

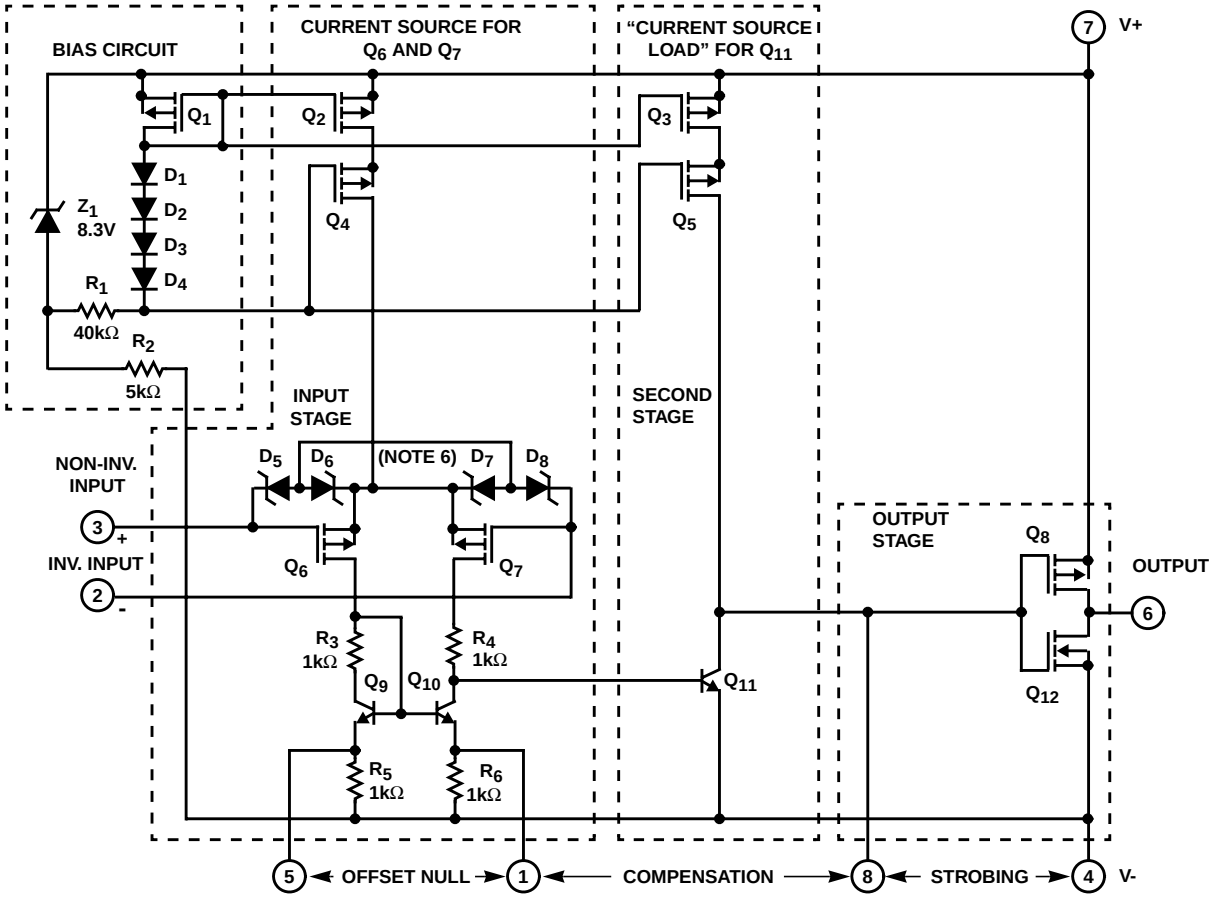
Electrical Specifications Typical Values Intended Only for Design Guidance, At $T_A = 25^oC$, $V_{SUPPLY} = \pm 7.5V$ Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA5130	CA5130A	UNITS
			TYP	TYP	
Input Offset Voltage Adjustment Range		10kΩ Across Terminals 4 and 5 or 4 and 1	±22	±22	mV
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I	f = 1MHz	4.3	4.3	pF
Equivalent Input Noise Voltage	e_N	BW = 0.2MHz, R_S = 1MΩ (Note 5)	23	23	µV
Open Loop Crossover Frequency For Unity Gain Stability ≥47pF Required	f_T	C_C = 0	15	15	MHz
		C_C = 47pF	4	4	MHz
Slew Rate	SR				
Open Loop		C_C = 0	30	30	V/µs
Closed Loop		C_C = 56pF	10	10	V/µs
Transient Response		C_C = 56pF, C_L = 25pF, R_L = 2kΩ (Voltage Follower)			
Rise Time	t_r		0.09	0.09	µs
Overshoot	OS		10	10	%
Settling Time (To <0.1%, $V_{IN} = 4V_{P-P}$)	t_S	C_C = 56pF, C_L = 25pF, R_L = 2kΩ (Voltage Follower)	1.2	1.2	µs

NOTE:

5. Although a 1MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10MΩ.

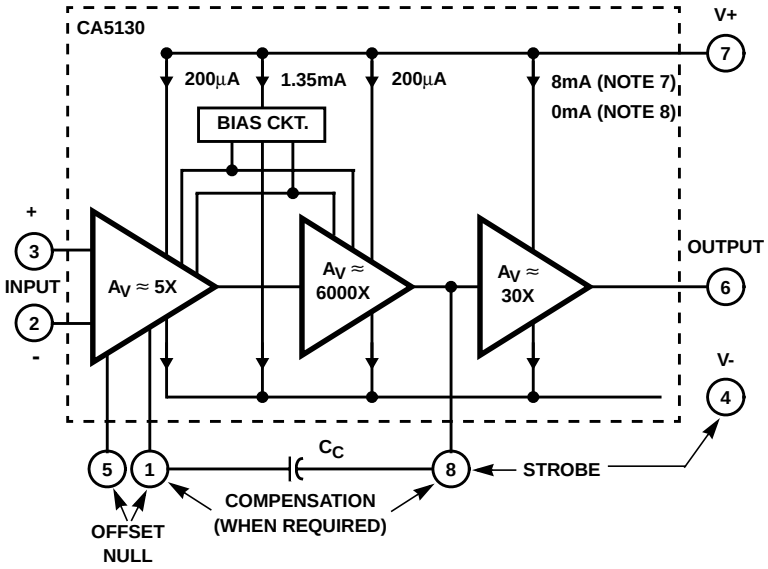
Schematic Diagram



NOTE:

6. Diodes D_5 through D_8 provide gate oxide protection for MOSFET Input Stage.

Block Diagram



NOTES:

7. Total supply voltage (for indicated voltage gains) = 15V with input terminals biased so that Terminal 6 potential is +7.5V above Terminal 4.
8. Total supply voltage (for indicated voltage gains) = 15V with output terminal driven to either supply rail.

Application Information

Circuit Description

The input terminals shown in the block diagram of the CA5130 Series CMOS Operational Amplifiers may be operated down to 0.5V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA5130 Series circuits are ideal for single supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in the Block Diagram, provide the total gain of the CA5130. A biasing circuit provides two potentials for common use in the first and second stages. Terminal 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed “OFF” condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

Input Stages

The circuit of the CA5130 is shown in the Schematic Diagram. It consists of a differential input stage using PMOS field-effect transistors (Q_6, Q_7) working into a mirror pair of bipolar transistors (Q_9, Q_{10}) functioning as load resistors together with resistors R_3 through R_6. The mirror pair transistors also function as a differential-to-single-ended converter to provide base drive to the second stage bipolar transistor (Q_{11}). Offset nulling, when desired, can be effected by connecting a 100,000Ω potentiometer across Terminals 1 and 5 and the potentiometer slider arm to Terminal 4. Cascode connected PMOS transistors Q_2, Q_4 are the constant current source for the input stage. The biasing circuit for the constant current source is subsequently described. The small diodes D_5 through D_8 provide gate oxide protection against high voltage transients, e.g., including static electricity during handling for Q_6 and Q_7.

Second Stage

Most of the voltage gain in the CA5130 is provided by the second amplifier stage, consisting of bipolar transistor Q_{11} and its cascode connected load resistance provided by PMOS transistors Q_3 and Q_5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terminals 1 and 8. A 47pF capacitor provides sufficient compensation for stable unity gain operation in most applications.

Bias Source Circuit

At total supply voltages, somewhat above 8.3V, resistor R_2 and zener diode Z_1 serve to establish a voltage of 8.3V across the series connected circuit, consisting of resistor R_1, diodes D_1 through D_4, and PMOS transistor Q_1. A tap at the junction of resistor R_1 and diode D_4 provides a gate bias potential of about 4.5V for PMOS transistors Q_4 and Q_5 with respect to Terminal 7. A potential of about 2.2V is developed across diode connected PMOS transistor Q_1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q_2 and Q_3. It should be noted that Q_1 is “mirror connected” to both Q_2 and Q_3. Since transistors Q_1, Q_2, Q_3 are designed to be identical, the approximately 200µA current in Q_1 establishes a similar current in Q_2 and Q_3 as constant current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3V, zener diode Z_1 becomes nonconductive and the potential, developed across series connected R_1, D_1-D_4, and Q_1, varies directly with variations in supply voltage. Consequently, the gate bias for Q_4, Q_5 and Q_2, Q_3 varies in accordance with supply voltage variations. This variation results in deterioration of the power supply rejection ratio (PSRR) at total supply voltages below 8.3V. Operation at total supply voltages below about 4.5V results in seriously degraded performance.

Output Stage

The output stage consists of a drain loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance load, the output can be swung within mV of either supply rail. Because the output stage is a drain loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Figure 15. Typical op amp loads are readily driven by the output stage. Because large signal excursions are nonlinear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01% accuracy levels, including the negative supply rail.

Input Current Variation with Common Mode Input Voltage

As shown in the Table of Electrical Specifications, the input current for the CA5130 Series Op Amps is typically 5pA at $T_A = 25^oC$ when Terminals 2 and 3 are at a common mode potential of +7.5V with respect to negative supply Terminal 4. Figure 24 contains data showing the variation of input current as a function of common mode input voltage at $T_A = 25^oC$. This data shows that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1pA, provided the common mode input voltage does not exceed 2V. As previously noted, the input current is essentially the result of the leakage current through the gate protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the metal can package also contributes an increment of leakage current, there are useful compensating factors. Because the gate protection network functions as if it is connected to Terminal 4 potential, and the metal can case of the CA5130 is also internally tied to Terminal 4, input Terminal 3 is essentially “guarded” from spurious leakage currents.

Offset Nulling

Offset voltage nulling is usually accomplished with a 100,000Ω potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset null adjustment usually can be effected with the slider arm positioned in the midpoint of the potentiometer's total range.

Input Current Variation with Temperature

The input current of the CA5130 Series circuits is typically 5pA at 25^{o}C. The major portion of this input current is due to leakage current through the gate protective diodes in the input circuit. As with any semiconductor junction device, including op amps with a junction FET input stage, the leakage current approximately doubles for every 10^{o}C increase in temperature. Figure 25 provides data on the typical variation of input bias current as a function of temperature in the CA5130.

In applications requiring the lowest practical input current and incremental increases in current because of “warm-up” effects, it is suggested that an appropriate heat sink be used with the CA5130. In addition, when “sinking” or “sourcing” significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input Offset Voltage (V_{IO}) Variation with DC Bias vs Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a DC gate source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA5130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential DC bias voltage applied across Terminals 2 and 3. Figure 26 shows typical data pertinent to shifts in offset voltage encountered with CA5130 devices (metal can package) during life testing. At lower temperatures (metal can and plastic packages), for example at 85^{o}C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The 2V differential voltage example represents conditions when the amplifier output stage is “toggled”, e.g., as in comparator applications.

Power-Supply Considerations

Because the CA5130 is very useful in single supply applications, it is pertinent to review some considerations relating to power supply current consumption under both single and dual supply service. Figures 1A and 1B show the CA5130 connected for both dual and single supply operation.

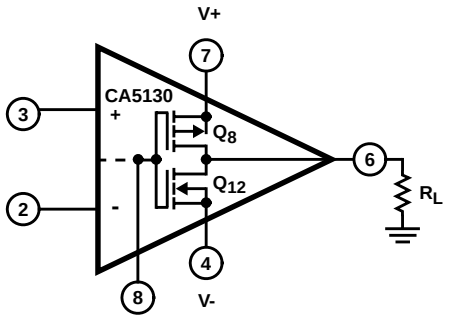


FIGURE 1A. DUAL POWER SUPPLY OPERATION

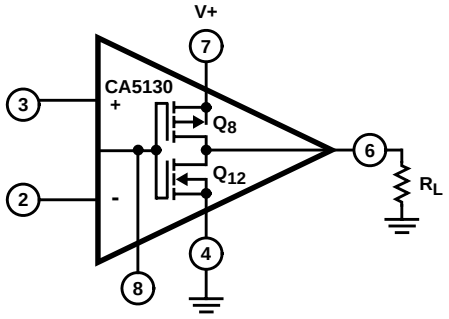


FIGURE 1B. SINGLE POWER SUPPLY OPERATION

FIGURE 1. CA5130 OUTPUT STAGE IN DUAL AND SINGLE POWER SUPPLY OPERATION

Dual supply operation: When the output voltage at Terminal 6 is 0V, the currents supplied by the two power supplies are equal. When the gate terminals of Q_8 and Q_{12} are driven increasingly positive with respect to ground, current flow through Q_{12} (from the negative supply) to the load is increased and current flow through Q_8 (from the positive supply) decreases correspondingly. When the gate terminals of Q_8 and Q_{12} are driven increasingly negative with respect to ground, current flow through Q_8 is increased and current flow through Q_{12} is decreased accordingly.

Single supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2, i.e., the voltage drops across Q_8 and Q_{12} are of equal magnitude. Figure 16 shows typical quiescent supply current vs supply voltage for the CA5130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage transfer characteristics (see Figure 15). If either Q_8 or Q_{12} are swung out of their linear regions toward cutoff (a nonlinear region), there will be a corresponding reduction in supply current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q_{12} is completely cut off and the supply current to series connected

transistors Q_8, Q_{12} goes essentially to zero. The two preceding stages in the CA5130, however, continue to draw modest supply current (see the lower curve in Figure 16) even though the output stage is strobed off. Figure 1A shows a dual supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load resistance of nominal value (e.g., 2kΩ) is connected between Terminal 6 and ground in the circuit of Figure 1B. Let it further be assumed that the input terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2. Since PMOS transistor Q_8 must now supply quiescent current to both R_L and transistor Q_{12}, it should be apparent that under these conditions the supply current must increase as an inverse function of the R_L magnitude. Figure 22 shows the voltage drop across PMOS transistor Q_8 as a function of load current at several supply voltages. Figure 15 shows the voltage transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low noise performance considerations, the use of the CA5130 is most advantageous in applications where the source resistance of the input signal is on the order of 1MΩ or more. In this case, the total input referred noise voltage is typically only 23μV when the test circuit amplifier of Figure 2 is operated at a total supply voltage of 15V. This value of total input referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1MΩ, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

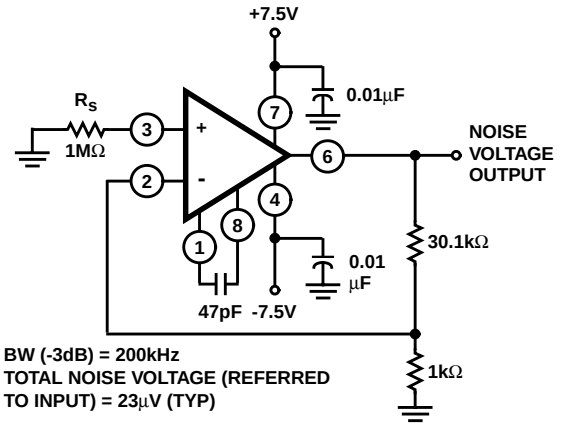


FIGURE 2. CA5130 OUTPUT STAGE IN DUAL AND SINGLE POWER SUPPLY OPERATION

Typical Applications

Voltage Followers

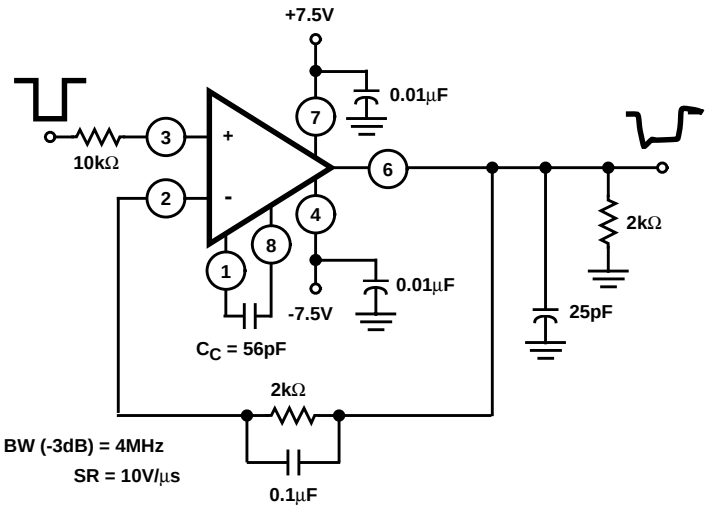
Operational amplifiers with very high input resistances, like the CA5130, are particularly suited to service as voltage followers. Figure 3 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA5130 in a split supply configuration.

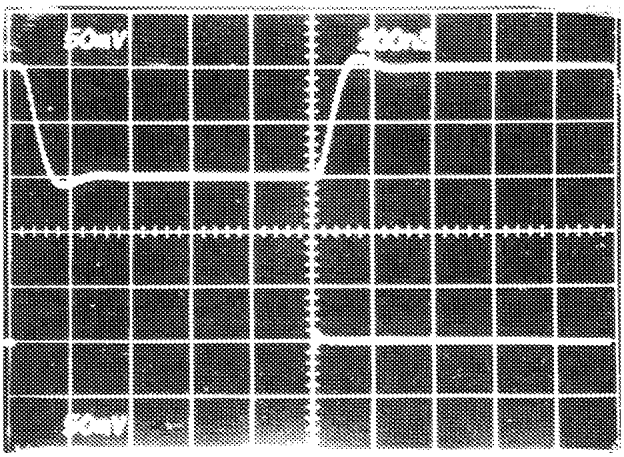
A voltage follower, operated from a single supply, is shown in Figure 4, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Figure 4A with input signal ramping. The waveforms in Figure 4B show that the follower does not lose its input-to-output phase sense, even though the input is being swung 7.5V below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Figure 4B also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA5130 in a single supply voltage follower application.

9-Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC) (see Note) is shown in Figure 5. This system combines the concepts of multiple switch CMOS ICs, a low cost ladder network of discrete metal-oxide film resistors, a CA5130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10V logic levels are used in the circuit of Figure 5.

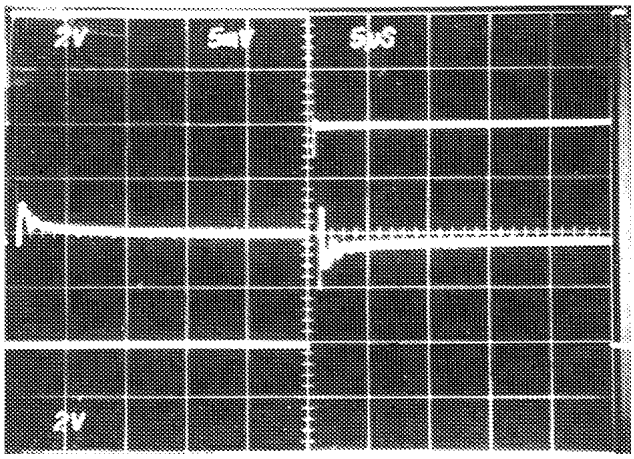
NOTE: “Digital-to-Analog Conversion Using the Intersil CD4007A CMOS IC”, Application Note AN6080.





Top Trace: Output
Bottom Trace: Input

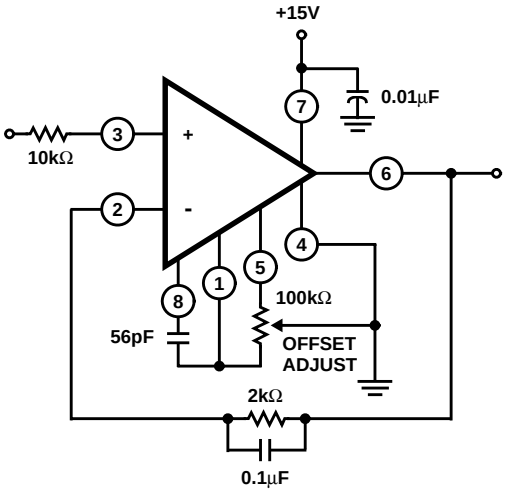
FIGURE 3A. SMALL SIGNAL RESPONSE (50mV/DIV., 200ns/DIV.)

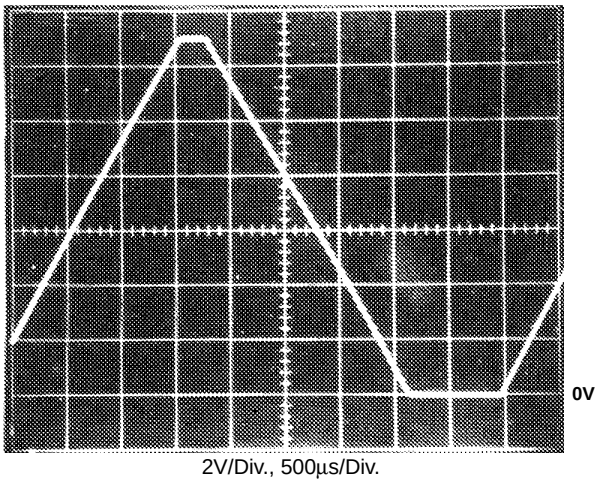


Top Trace: Output Signal = 2V/Div., 5µs/Div.
Center Trace: Difference Signal = 5mV/Div., 5µs/Div.
Bottom Trace: Input Signal = 2V/Div., 5µs/Div.

FIGURE 3B. INPUT OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME (MEASUREMENT MADE WITH TEKTRONIX 7A13 DIFFERENTIAL AMPLIFIER)

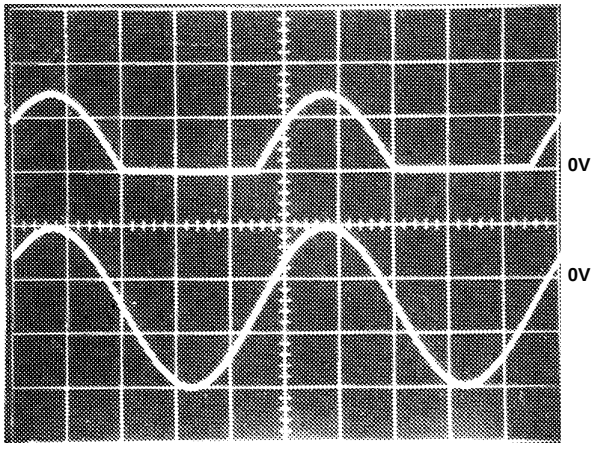
FIGURE 3. CA5130 SPLIT SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS





2V/Div., 500µs/Div.

FIGURE 4A. OUTPUT WAVEFORM WITH INPUT SIGNAL RAMPING



Top Trace: Output = 5V/Div., 200µs/Div.
Bottom Trace: Input = 5V/Div., 200µs/Div.

FIGURE 4B. OUTPUT WAVEFORM WITH GROUND REFERENCE SINE WAVE INPUT

FIGURE 4. SINGLE SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS. (e.g., FOR USE IN SINGLE SUPPLY D/A CONVERTER; SEE FIGURE 9 IN AN6080)

The circuit uses an R/2R voltage ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power supply terminal. Each CD4007A contains three “inverters”, each “inverter” functioning as a single pole double throw switch to terminate an arm of the R/2R network at either the positive or negative power supply terminal. The resistor ladder is an assembly of one percent tolerance metal oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000Ω resistors from the same manufacturing lot.

A single 15V supply provides a positive bus for the CA5130 follower amplifier and feeds the CA3085 voltage regulator. A “scale adjust” function is provided by the regulator output control, set to a nominal 10V level in this system. The line voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the CMOS building blocks simplifies the design of DAC systems tailored to particular needs.

Single Supply, Absolute Value, Ideal Full Wave Rectifier

The absolute value circuit using the CA5130 is shown in Figure 6. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative going excursion of the input signal, the CA5130 functions as a normal inverting amplifier with a gain equal to $-R_2/R_1$. When the equality of the two equations shown in Figure 6 is satisfied, the full wave output is symmetrical.

Peak Detectors

Peak detector circuits are easily implemented with the CA5130, as illustrated in Figure 7 for both the peak positive and the peak negative circuit. It should be noted that with large signal inputs, the bandwidth of the peak negative circuit is much less than that of the peak positive circuit. The second stage of the CA5130 limits the bandwidth in this case. Negative going output signal excursion requires a positive going signal excursion at the collector of transistor Q_{11}, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative going signal excursion at the collector of Q_{11}, the transistor functions in active “pull down” mode so that the intrinsic capacitance can be discharged more expeditiously.

Error Amplifier In Regulated Power Supplies

The CA5130 is an ideal choice for error amplifier service in regulated power supplies since it can function as an error amplifier when the regulated output voltage is required to approach 0V. Figure 8 shows the schematic diagram of a 40mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0V to 13V. Q_3 and Q_4 in IC_2 (a CA3066 transistor array IC) function as zeners to provide supply voltage for the CA5130 comparator (IC_1). Q_1, Q_2, and Q_5 in IC_2 are configured as a low impedance, temperature compensated source of adjustable reference voltage for the error amplifier.

Transistors Q_1, Q_2, Q_3, and Q_4 in IC_3 (another CA3086 transistor array IC) are connected in parallel as the series pass element. Transistor Q_5 in IC_3 functions as a current limiting device by diverting base drive from the series pass transistors, in accordance with the adjustment of resistor R_2.

Figure 9 contains the schematic diagram of a regulated power supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1V to 50V and currents up to 1A. The error amplifier (IC_1) and circuitry associated with IC_2 function as previously described, although the output of IC_1 is boosted by a discrete transistor (Q_4) to provide adequate base drive for the Darlington connected series pass transistors Q_1, Q_2. Transistor Q_3 functions in the previously described current limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA5130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the “on” and “off” periods, is shown in Figure 10. Resistors R_1 and R_2 are used to bias the CA5130 to the midpoint of the supply voltage and R_3 is the feedback resistor. The pulse repetition rate is selected by positioning S_1 to the desired position and the rate remains essentially constant when the resistors which determine “on period” and “off period” are adjusted.

Function Generator

Figure 11 contains a schematic diagram of a function generator using the CA5130 in the integrator and threshold detector functions. This circuit generates a triangular or square wave output that can be swept over a 1,000,000:1 range (0.1Hz to 100kHz) by means of a single control, R_1. A voltage control input is also available for remote sweep control.

The heart of the frequency determining system is an operational transconductance amplifier (OTA) (see Note 9), IC_1, operated as a voltage controlled current source. The output, I_O, is a current applied directly to the integrating capacitor, C_1, in the feedback loop of the integrator IC_2, using a CA5130, to provide the triangular wave output. Potentiometer R_2 is used to adjust the circuit for slope symmetry of positive going and negative going signal excursions.

Another CA5130, IC_3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C_2 is a “peaking adjustment” to optimize the high frequency square wave performance of the circuit.

Potentiometer R_3 is adjustable to perfect the “amplitude symmetry” of the square wave output signals. Output from the threshold detector is fed back via resistor R_4 to the input of IC_1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

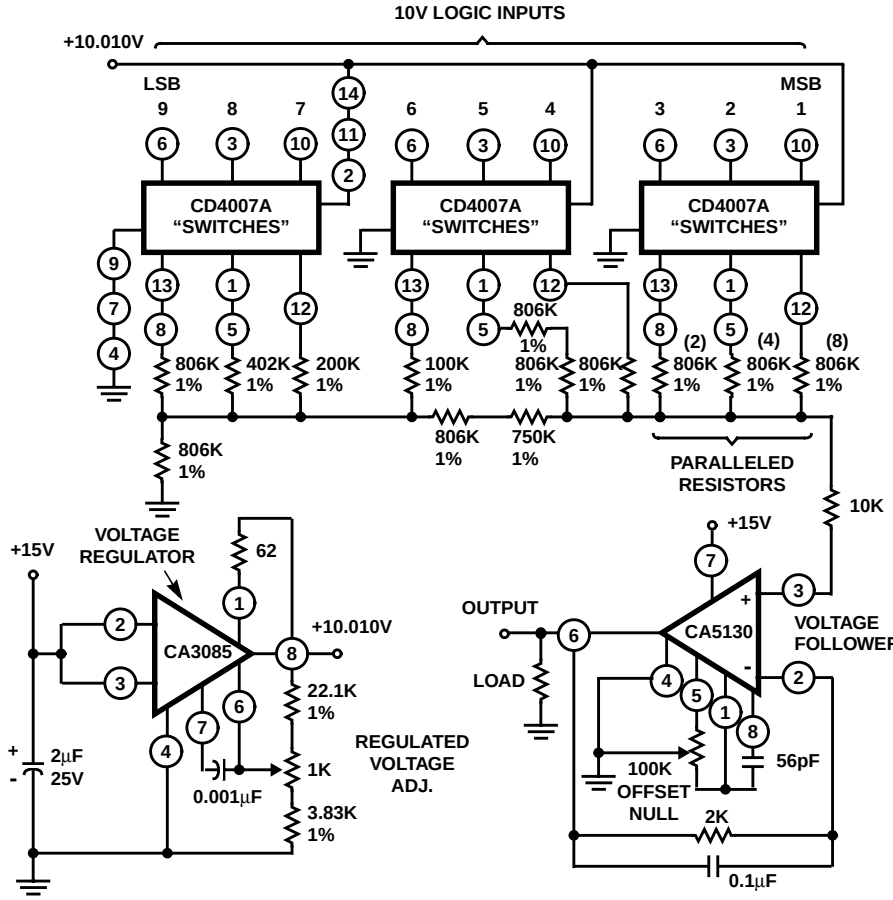
Operation with Output Stage Power-Booster

The current sourcing and sinking capability of the CA5130 output stage is easily supplemented to provide power boost capability. In the circuit of Figure 12, three CMOS transistor pairs in a single CA3600E (see Note 10) IC array are shown parallel connected with the output stage in the CA5130. In the Class A mode of CA3600E shown, a typical device consumes 20mA of supply current at 15V operation. This arrangement boosts the current handling capability of the CA5130 output stage by about 2.5X.

The amplifier circuit in Figure 12 employs feedback to establish a closed-loop gain of 48dB. The typical large signal bandwidth (-3dB) is 50kHz.

NOTES:

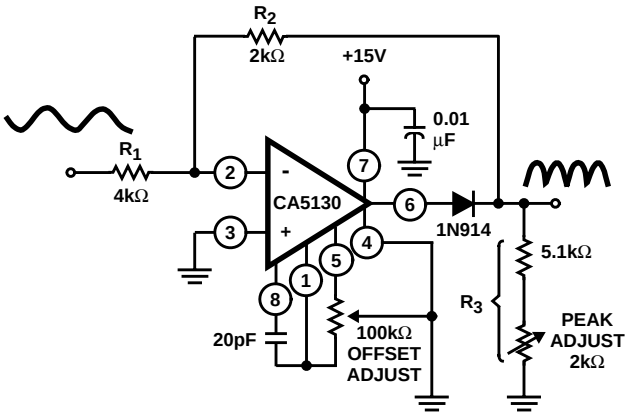
9. See File No. 475 and AN6668.
10. See File No. 619 for technical information.



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6 - 9	±1% ABS

NOTE: All Resistances are In Ohms.

FIGURE 5. 9-BIT DAC USING CMOS DIGITAL SWITCHES AND CA5130

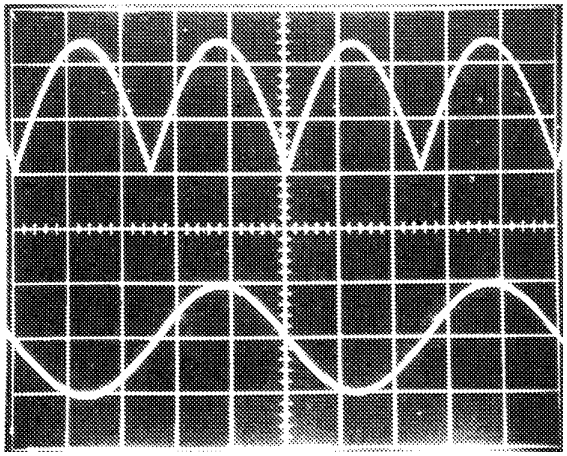


$$\text{Gain} = \frac{R_2}{R_1} = X = \frac{R_3}{R_1 + R_2 + R_3}$$

$$R_3 = R_1\left(\frac{X + X^2}{1 - X}\right)$$

$$\text{For } X = 0.5: \frac{2k\Omega}{4k\Omega} = \frac{R_2}{R_1}$$

$$R_3 = 4k\Omega\left(\frac{0.75}{0.5}\right) = 6k\Omega$$



Top Trace: Output Signal = 2V/Div.
Bottom Trace: Input Signal = 10V/Div.
Time base on both traces = 0.2ms/Div.

$20V_{P-P}$ Input: BW (-3dB) = 230kHz, DC Output (Avg) = 3.2V
$1V_{P-P}$ Input: BW (-3dB) = 130kHz, DC Output (Avg) = 160mV

FIGURE 6. SINGLE SUPPLY, ABSOLUTE VALUE, IDEAL FULL WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS

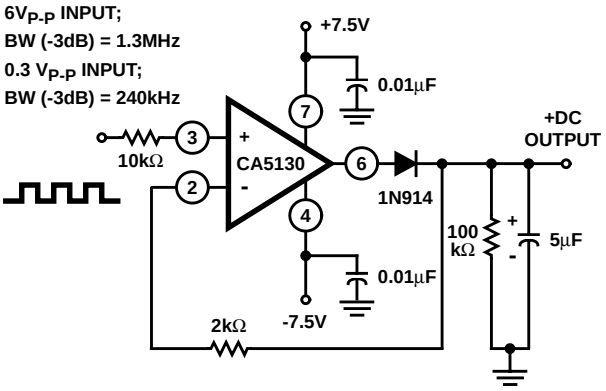


FIGURE 7A. PEAK POSITIVE DETECTOR CIRCUIT

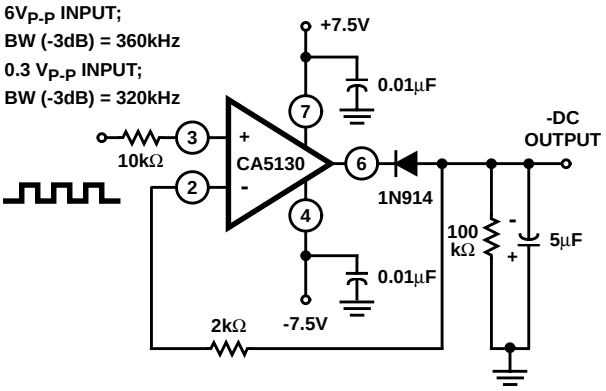
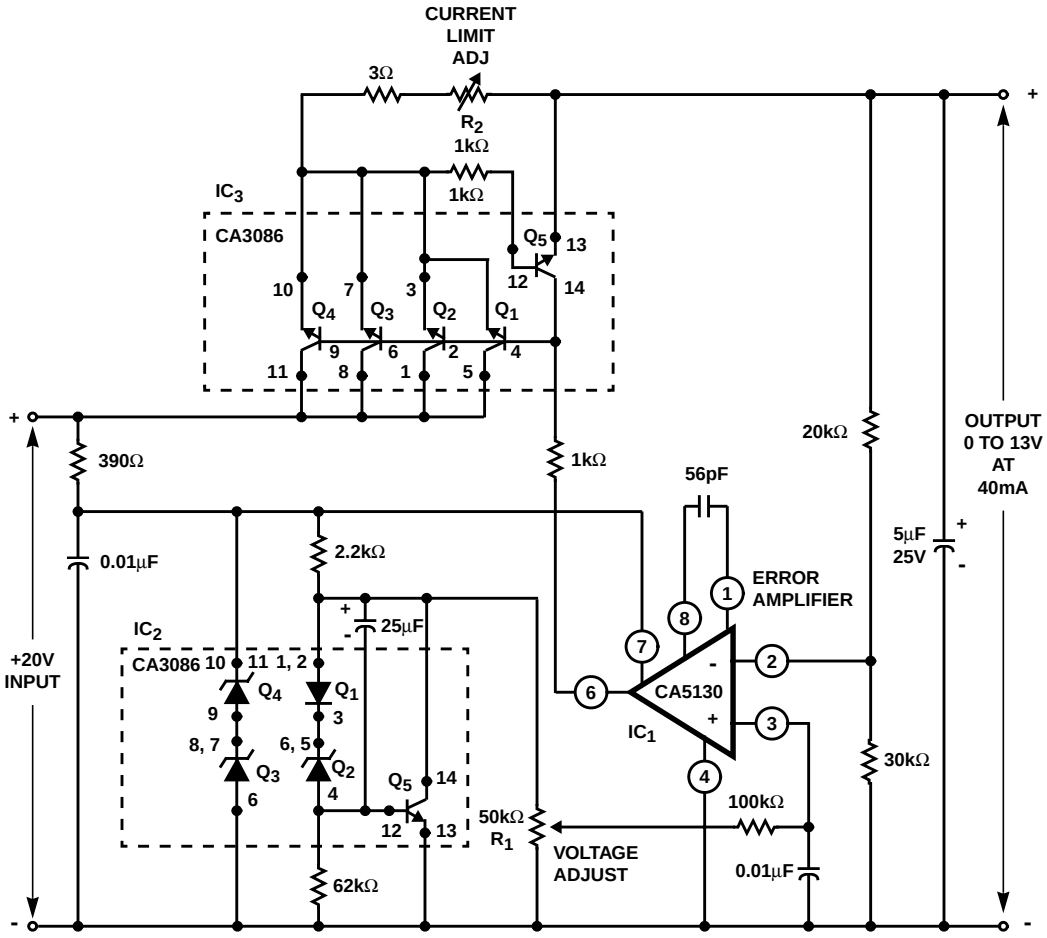


FIGURE 7B. PEAK NEGATIVE DETECTOR CIRCUIT

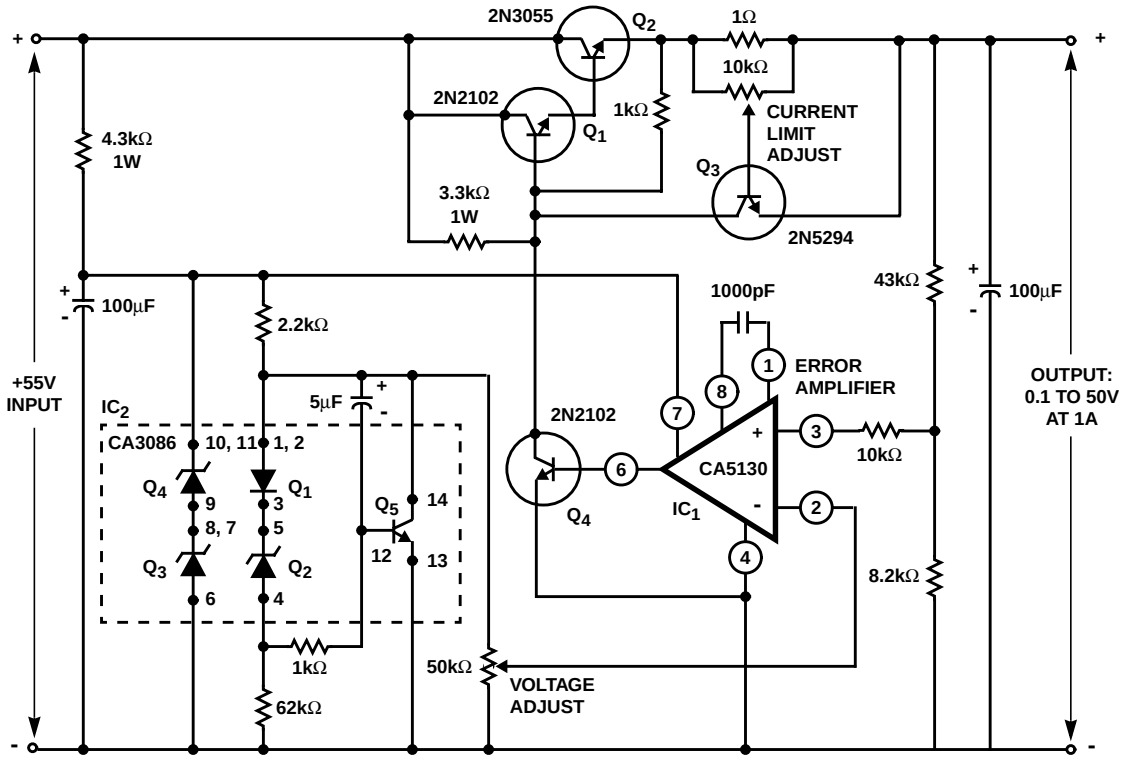
FIGURE 7. PEAK-DETECTOR CIRCUITS



NOTES:

11. Regulation (no load to full load): <0.01%.
12. Input Regulation: 0.02%/V.
13. Hum and noise output: <25µV up to 100kHz.

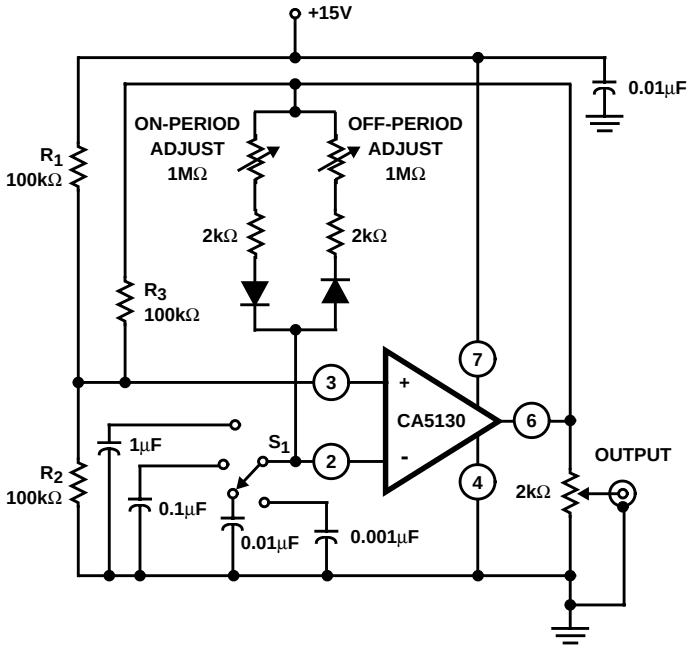
FIGURE 8. VOLTAGE REGULATOR CIRCUIT (0V TO 13V AT 40mA)



NOTES:

14. Regulation (no load to full load): <0.005%.
15. Input Regulation: 0.01%/V.
16. Hum and noise output: <250μV_{RMS} up to 100kHz.

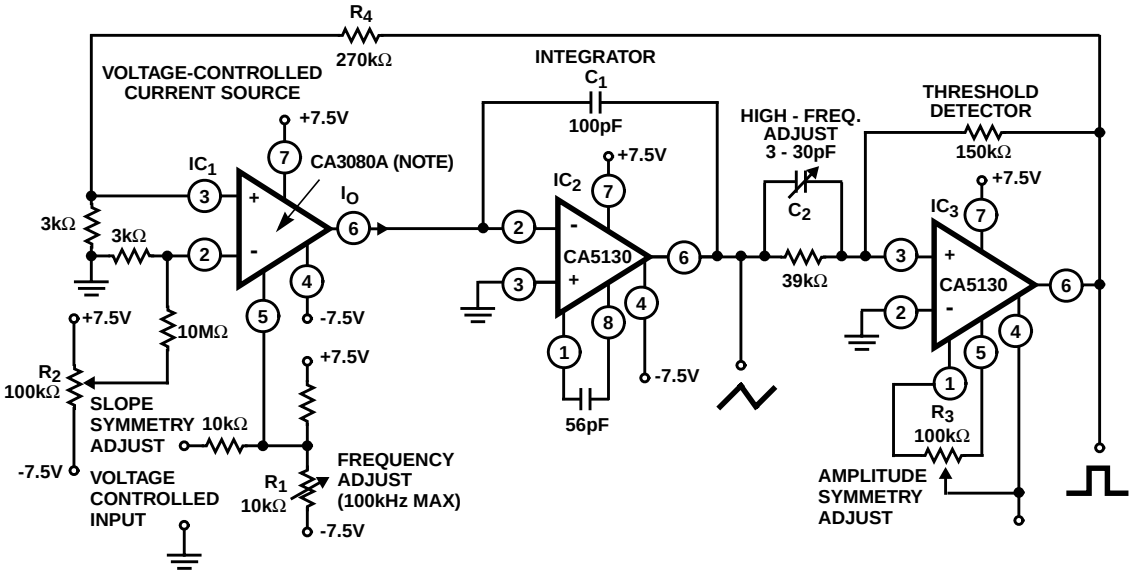
FIGURE 9. VOLTAGE REGULATOR CIRCUIT (0.1V TO 50V AT 1A)



FREQUENCY RANGE:

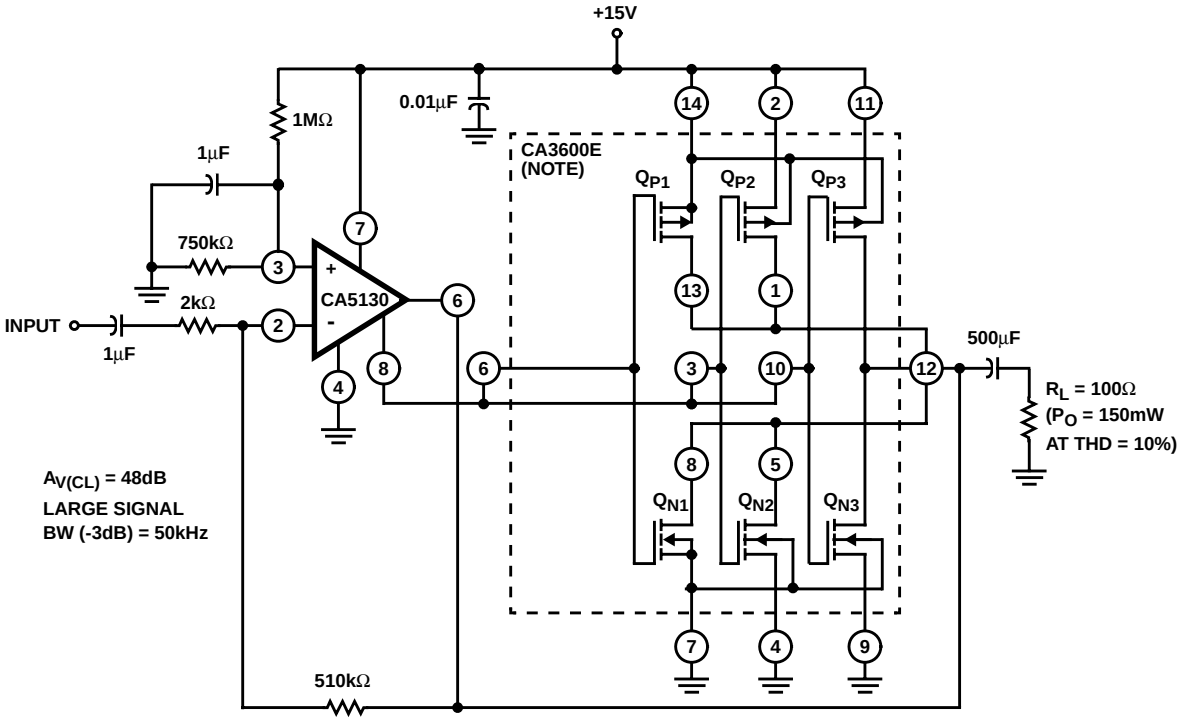
POSITION OF S_1	PULSE PERIOD
0.001μF	4μs to 1ms
0.01μF	40μs to 10ms
0.1μF	0.4ms to 100ms
1μF	4ms to 1s

FIGURE 10. PULSE GENERATOR (ASTABLE MULTIVIBRATOR) WITH PROVISIONS FOR INDEPENDENT CONTROL OF "ON" AND "OFF" PERIODS



NOTE: See File Number 475 and AN6668 for technical information.

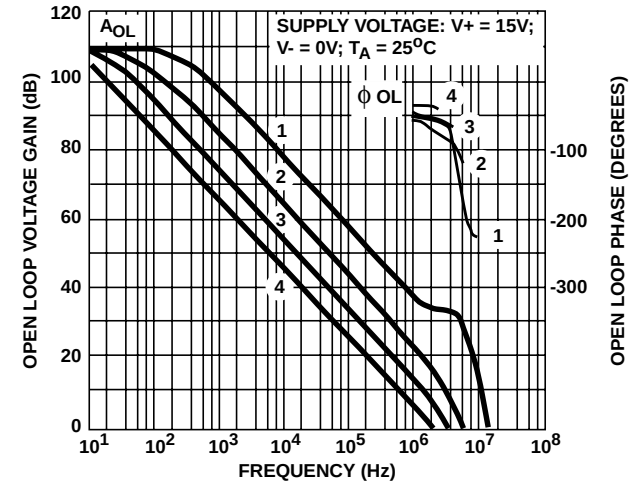
FIGURE 11. FUNCTION GENERATOR (FREQUENCY CAN BE VARIED 1,000,000/1 WITH A SINGLE CONTROL)



NOTE: Transistors Q_{P1}, Q_{P2}, Q_{P3} and Q_{N1}, Q_{N2}, Q_{N3} are parallel connected with Q_8 and Q_{12}, respectively, of the CA5130. See File Number 619.

FIGURE 12. CMOS TRANSISTOR ARRAY (CA3600E) CONNECTED AS POWER BOOSTER IN THE OUTPUT STAGE OF THE CA5130

Typical Performance Curves



1: C_L = 9pF, C_C = 0pF, R_L = ∞
2: C_L = 30pF, C_C = 15pF, R_L = 2kΩ
3: C_L = 30pF, C_C = 47pF, R_L = 2kΩ
4: C_L = 30pF, C_C = 150pF, R_L = 2kΩ

FIGURE 13. OPEN LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY

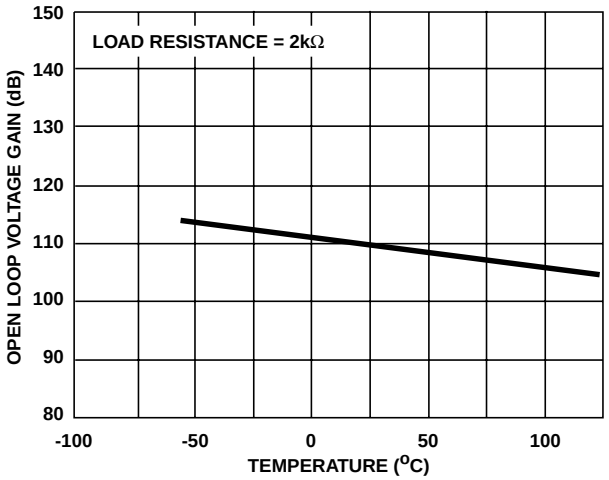


FIGURE 14. OPEN LOOP GAIN vs TEMPERATURE

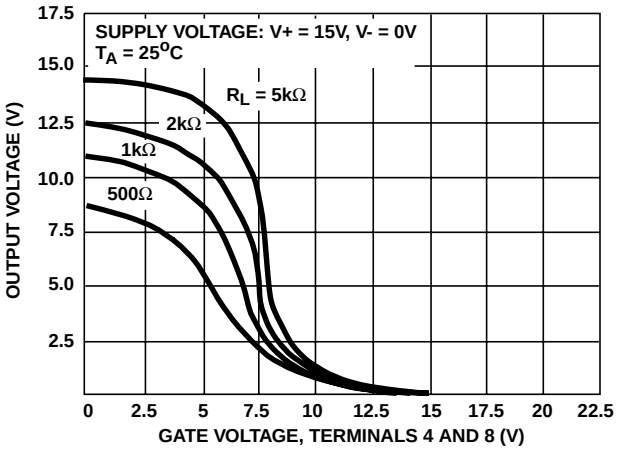


FIGURE 15. VOLTAGE TRANSFER CHARACTERISTICS OF CMOS OUTPUT STAGE

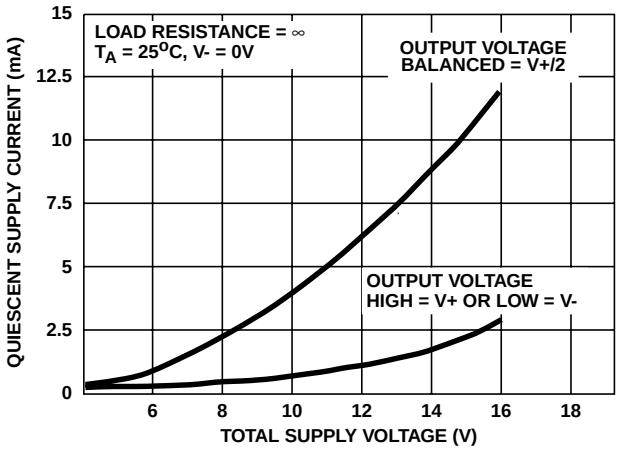


FIGURE 16. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

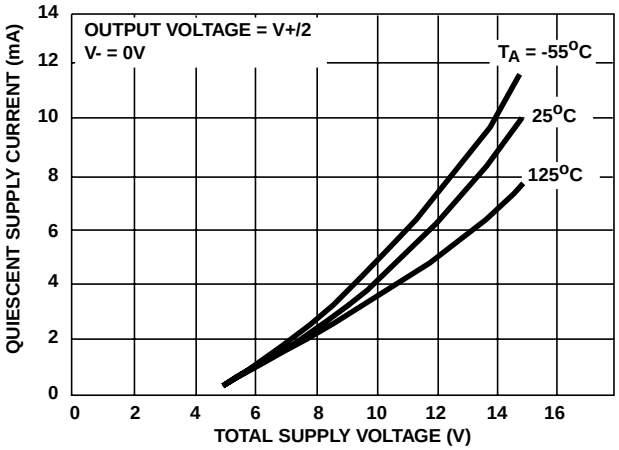


FIGURE 17. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

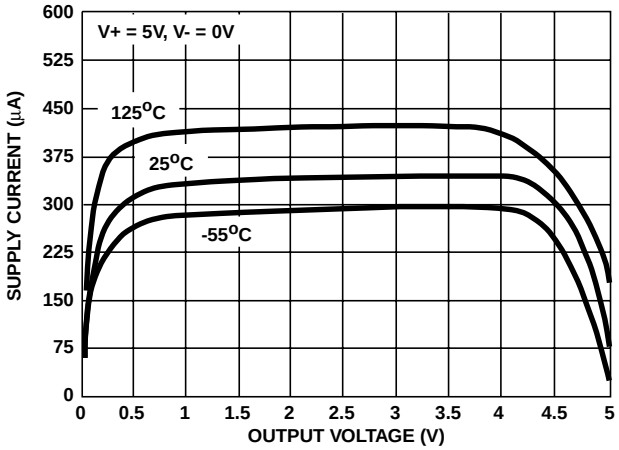


FIGURE 18. SUPPLY CURRENT vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

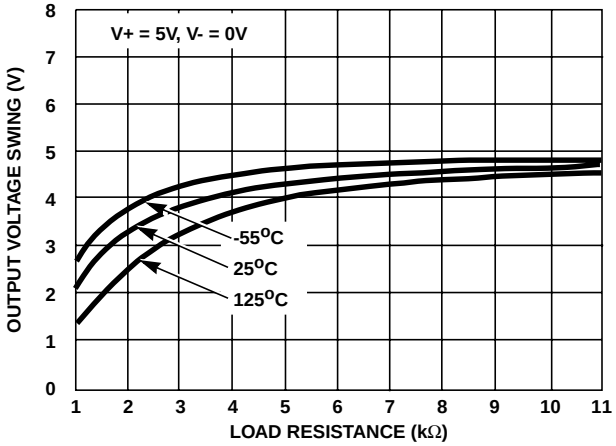


FIGURE 19. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

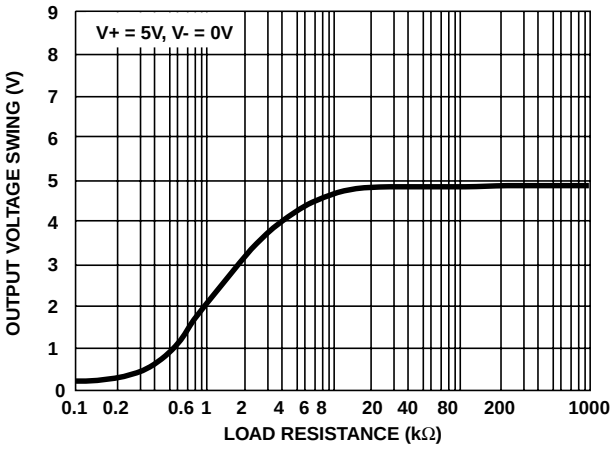


FIGURE 20. OUTPUT SWING vs LOAD RESISTANCE

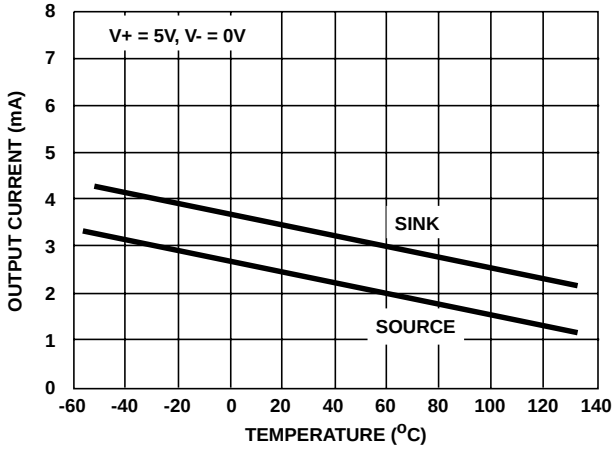


FIGURE 21. OUTPUT CURRENT vs TEMPERATURE

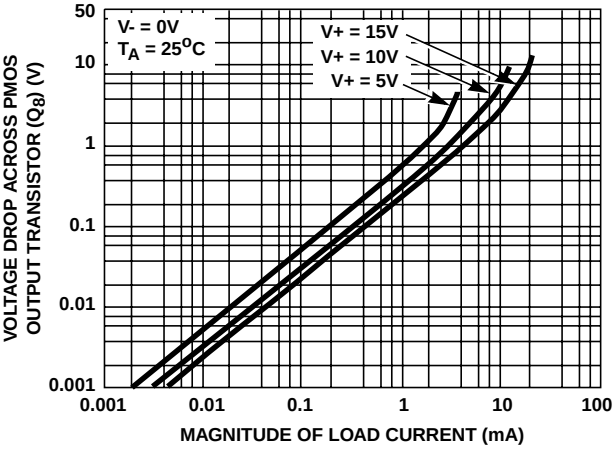


FIGURE 22. VOLTAGE ACROSS PMOS OUTPUT TRANSISTOR (Q_8) vs LOAD CURRENT

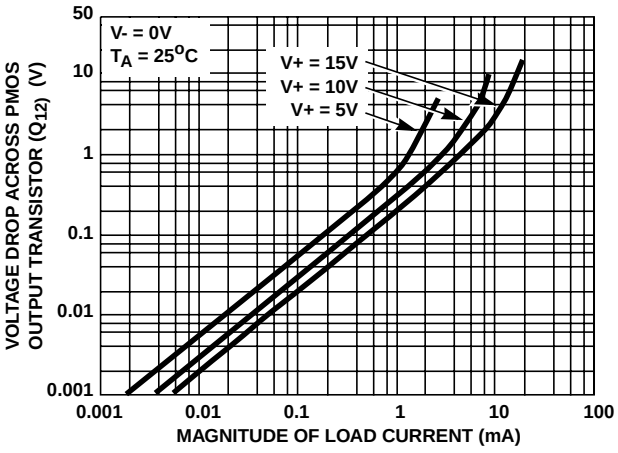


FIGURE 23. VOLTAGE ACROSS NMOS OUTPUT TRANSISTOR (Q_{12}) vs LOAD CURRENT

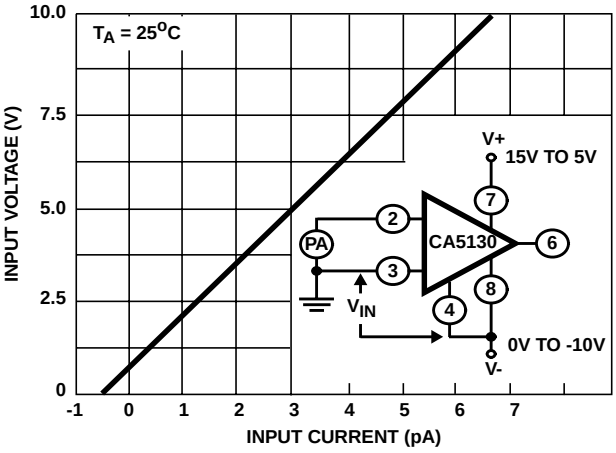


FIGURE 24. INPUT CURRENT vs COMMON MODE VOLTAGE

Typical Performance Curves (Continued)

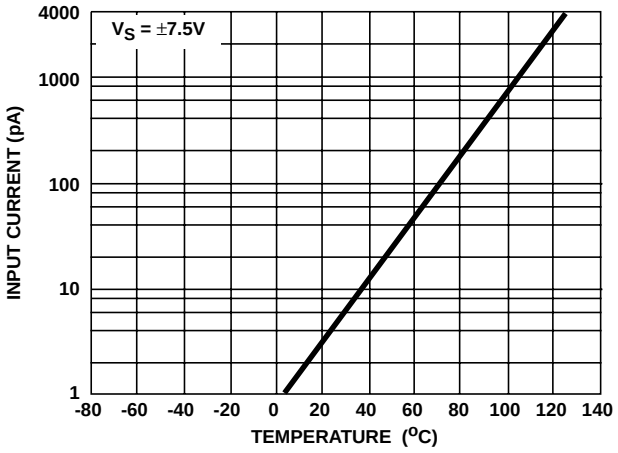


FIGURE 25. INPUT CURRENT vs TEMPERATURE

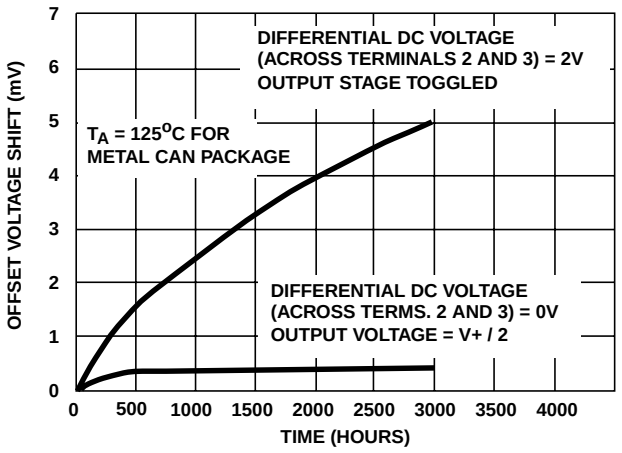
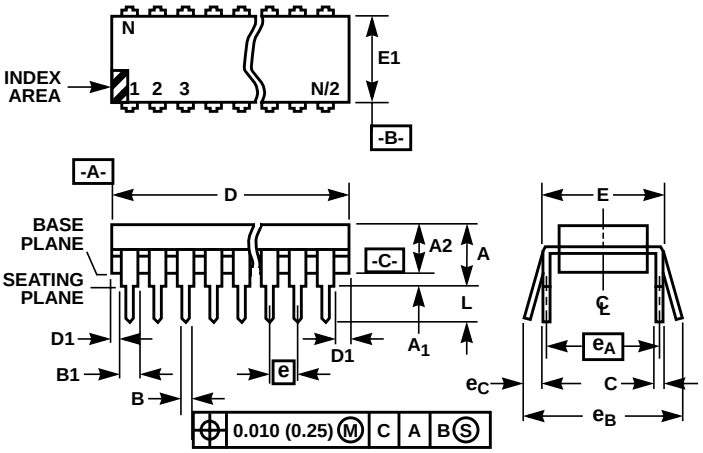


FIGURE 26. TYPICAL INCREMENTAL OFFSET VOLTAGE SHIFT vs OPERATING LIFE

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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