intersil

OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
ICM7216

ICM7226A, ICM7226B

8-Digit, Multi-Function, Frequency Counter/Timer

May 2001

Features

- **CMOS Design for Very Low Power**
- **Output Drivers Directly Drive Both Digits and Segments of Large 8-Digit LED Displays**
- **Measures Frequencies from DC to 10MHz; Periods from 0.5μs to 10s**
- **Stable High Frequency Oscillator uses either 1MHz or 10MHz Crystal**
- **Both Common Anode and Common Cathode Available**
- **Control Signals Available for External Systems Interfacing**
- **Multiplexed BCD Outputs**

Applications

- **Frequency Counter**
- **Period Counter**
- **Unit Counter**
- **Frequency Ratio Counter**
- **Time Interval Counter**

Part Number Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICM7226AIJL	-25× to 85	40 Ld CERDIP	F40.6
ICM7226BIPL	-25× to 85	40 Ld PDIP	E40.6

Description

The ICM7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexer and segment and digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

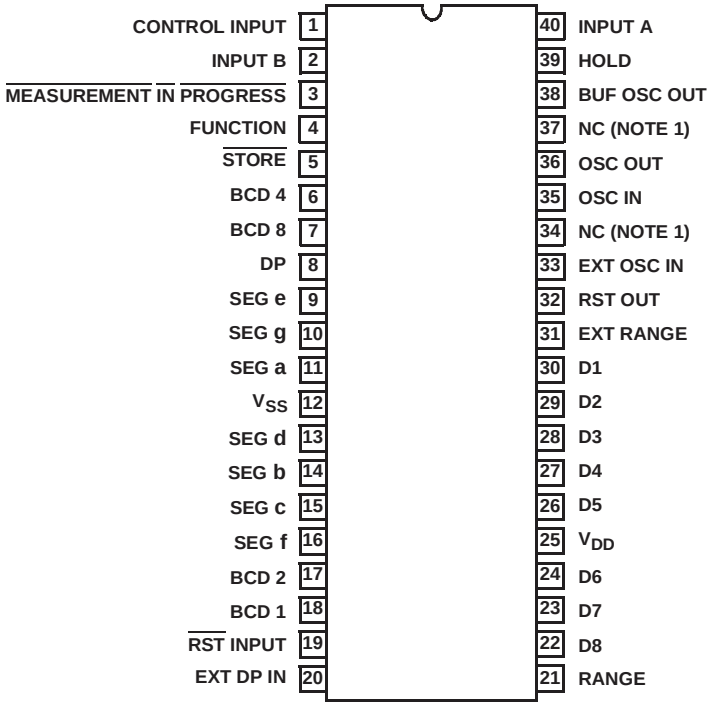
The ICM7226 can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The devices require either a 10MHz or 1MHz quartz crystal timebase, or if desired an external timebase can also be used. For period and time interval, the 10MHz timebase gives a 0.1μs resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01s, 0.1s, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1Hz. There is 0.2s between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

Leading zero blanking has been incorporated with frequency display in kHz and time in μs. The display is multiplexed at a 500Hz rate with a 12.2% duty cycle for each digit. The ICM7226A is designed for common anode displays with typical peak segment currents of 25mA, and the ICM7226B is designed for common cathode displays with typical segment currents of 12mA. In the display off mode, both digit drivers and segment drivers are turned off, allowing the display to be used for other functions.

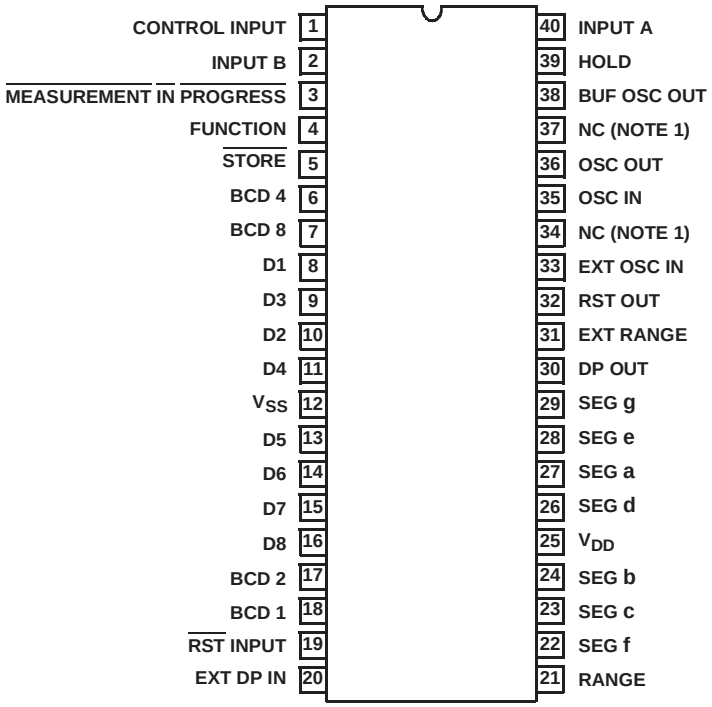
File Number **3169.2**

Pinouts

ICM7226A
COMMON ANODE (CERDIP)
TOP VIEW



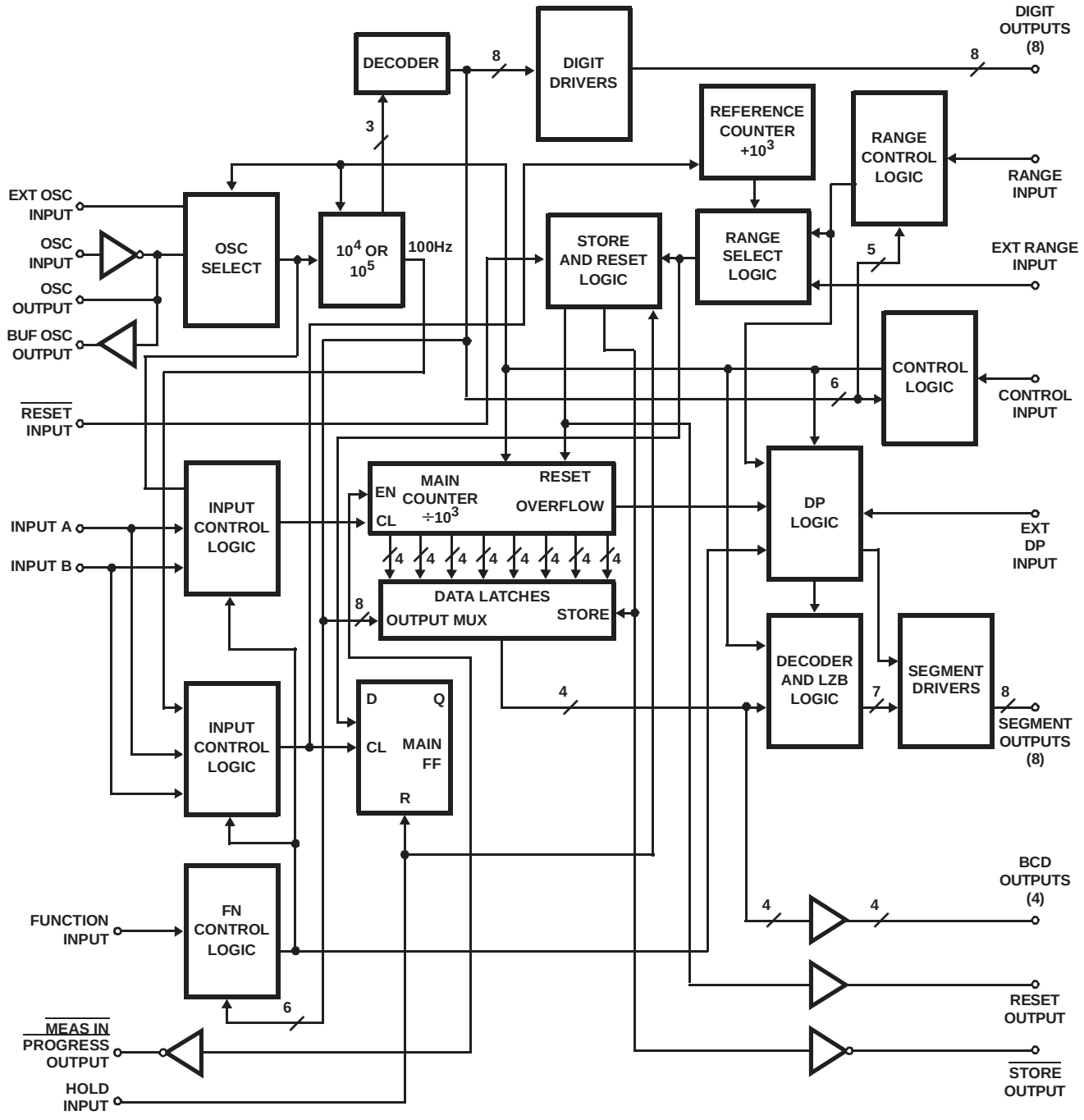
ICM7226B
COMMON CATHODE (PDIP)
TOP VIEW



NOTE:

1. For maximum frequency stability, connect to V_{DD} or V_{SS}.

Functional Block Diagram



Absolute Maximum Ratings

Maximum Supply Voltage (V_{DD} - V_{SS}) 6.5V
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
Voltage On Any Input or
Output Terminal (Note 1) . . . . . V_{DD} +0.3V to V_{SS} -0.3V

Operating Conditions

Temperature Range . . . . . -25°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	45	9
PDIP Package	50	N/A

Maximum Junction Temperature
CERDIP Package . . . . . 175°C
PDIP Package . . . . . 150°C
Maximum Storage Temperature Range . . . . . -55°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Destructive latchup may occur if input signals are applied before the power supply is established or if inputs or outputs are forced to voltages exceeding V_{DD} or V_{SS} by 0.3V.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{DD} = 5.0V, T_A = 25°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current, I_{DD}	Display Off, Unused Inputs to V_{SS}	-	2	5	mA
Supply Voltage Range (V_{DD} -V_{SS}), V_{SUPPLY}	-25°C to 85°C, INPUT A, INPUT B Frequency at f_{MAX}	4.75	-	6.0	V
Maximum Frequency INPUT A, Pin 40, $f_{A(MAX)}$	-25°C to 85°C 4.75V < V_{DD} < 6.0V, Figure 9 Function = Frequency, Ratio, Unit Counter	10	14	-	MHz
	Function = Period, Time Interval	2.5	-	-	MHz
Maximum Frequency INPUT B, Pin 2, $f_{B(MAX)}$	-25°C to 85°C 4.75V < V_{DD} < 6.0V, Figure 10	2.5	-	-	MHz
Minimum Separation INPUT A to INPUT B, Time Interval Function	-25°C to 85°C 4.75V < V_{DD} < 6.0V, Figure 1	250	-	-	ns
Oscillator Frequency and External Oscillator Frequency, f_{OSC}	-25°C to 85°C 4.75V < V_{DD} < 6.0V	0.1	-	10	MHz
Oscillator Transconductance, g_M	V_{DD} -4.75V, T_A = 85°C	2000	-	-	µS
Multiplex Frequency, f_{MUX}	f_{OSC} = 10MHz	-	500	-	Hz
Time Between Measurements	f_{OSC} = 10MHz	-	200	-	ms
Input Rate of Charge, dV_{IN}/dt	Inputs A, B	-	15	-	mV/µs
Input Voltages: Pins 2, 19, 33, 39, 40, 35					
Input Low Voltage, V_{IL}	-25°C to 85°C	-	-	1.0	V
Input High Voltage, V_{IH}		3.5	-	-	V
Pins 2, 39, 40, Input Leakage, A, B, I_{ILK}		-	-	20	µA
Input Resistance to V_{DD} Pins 19, 33, R_{IN}	V_{IN} = V_{DD} -1.0V	100	400	-	kΩ
Input Resistance to V_{SS} Pin 31, R_{IN}	V_{IN} = +1.0V	50	100	-	kΩ
Output Current					
Low Output Current, Pins 3, 5-7, 17, 18, 32, 38, I_{OL}	V_{OL} = +0.4V	400	-	-	µA
High Output Current, Pins 5-7, 17, 18, 32, H_{OL}	V_{OH} = +2.4V	100	-	-	µA
High Output Current, Pins 3, 38, H_{OL}	V_{OH} = V_{DD} -0.8V	265	-	-	µA
ICM7226A					
Segment Driver: Pins 8-11, 13-16					
Low Output Current, I_{OL}	V_O = +1.5V	25	35	-	mA
High Output Current, I_{OH}	V_O = V_{DD} -1.0V	-	100	-	µA

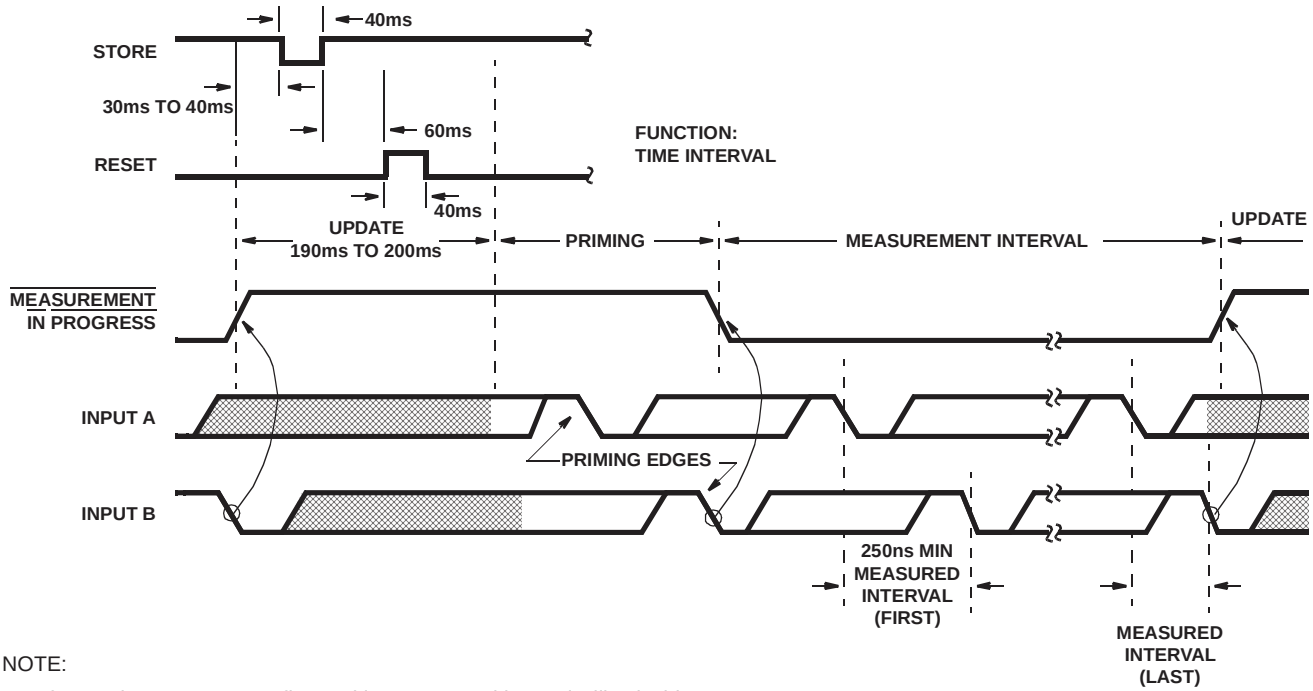
Electrical Specifications V_{DD} = 5.0V, T_A = 25°C, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Multiplex Inputs: Pins 1, 4, 20, 21					
Input Low Voltage, V_{IL}		-	-	0.8	V
Input High Voltage, V_{IH}		2.0	-	-	V
Input Resistance to V_{SS}, R_{IN}	V_{IN} = +1.0V	50	100	-	kΩ
Digit Driver: Pins 22-24, 26-30					
Low Output Current, I_{OL}	V_O = +1.0V	-	-0.3	-	mA
High Output Current, I_{OH}	$V_O = V_{DD}$ -2.0V	150	180	-	mA
ICM7226B					
Segment Driver: Pins 22-24, 26-30					
Leakage Current, I_L	$V_O = V_{SS}$	-	-	10	µA
High Output Current, I_{OH}	$V_O = V_{DD}$ -2.0V	10	15	-	mA
Multiplex Inputs: Pins 1, 4, 20, 21					
Input Low Voltage, V_{IL}		-	-	V_{DD}-2.0	V
Input High Voltage, V_{IH}		V_{DD}-0.8	-	-	V
Input Resistance to V_{SS}, R_{IN}	$V_{IN} = V_{DD}$ -1.0V	100	360	-	kΩ
Digit Driver: Pins 8-11, 13-16					
Low Output Current, I_{OL}	V_O = +1.0V	50	75	-	mA
High Output Current, I_{OH}	$V_O = V_{DD}$ -2.5V	-	100	-	µA

NOTES:

1. Assumes all leads soldered or welded to PC board and free air flow.
2. Typical values are not tested.

Timing Waveform



NOTE:

1. If range is set to 1 event, first and last measured interval will coincide.

FIGURE 1. WAVEFORMS FOR TIME INTERVAL MEASUREMENT (OTHERS ARE SIMILAR, BUT WITHOUT PRIMING PHASE)

Typical Performance Curves

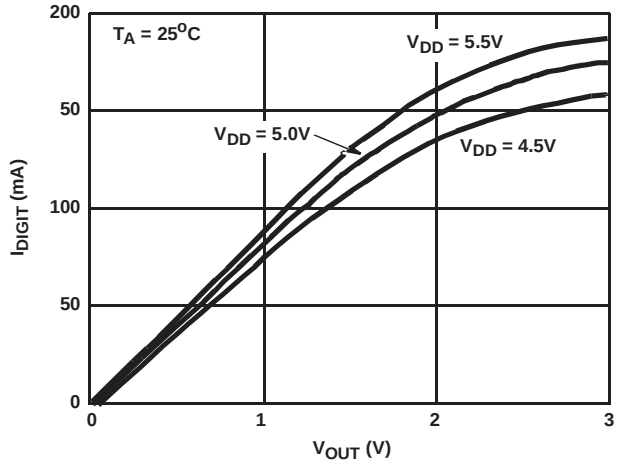


FIGURE 2. ICM7226B TYPICAL I_{DIGIT} vs V_{OUT}

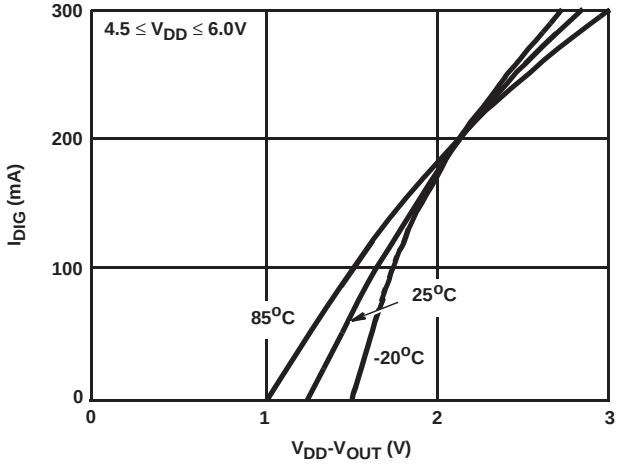


FIGURE 3. ICM7226A TYPICAL I_{DIG} vs V_{DD}-V_{OUT}

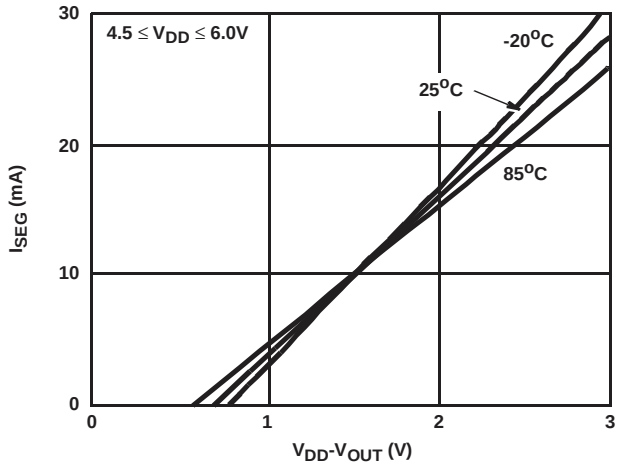


FIGURE 4. ICM7226B TYPICAL I_{SEG} vs V_{DD}-V_{OUT}

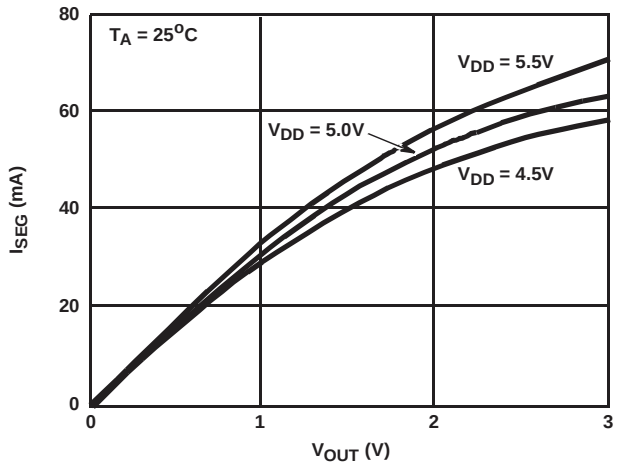


FIGURE 5. ICM7226A TYPICAL I_{SEG} vs V_{OUT}

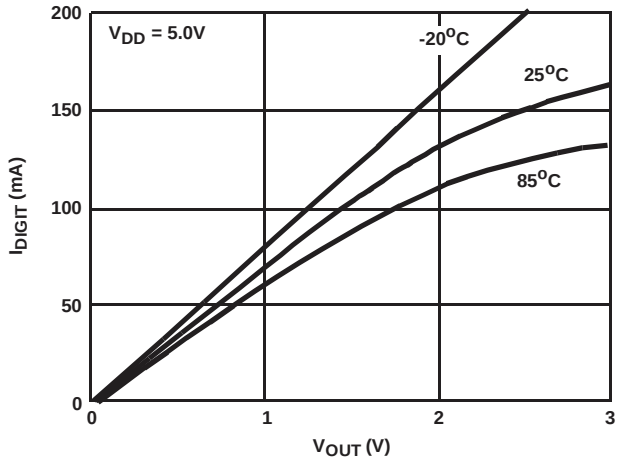


FIGURE 6. ICM7226B TYPICAL I_{DIGIT} vs V_{OUT}

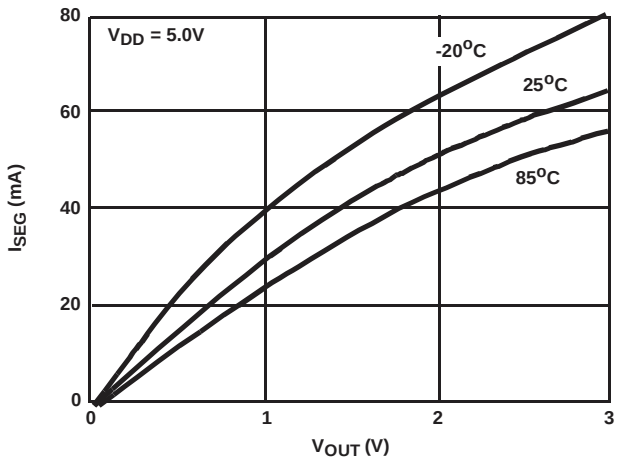


FIGURE 7. ICM7226A TYPICAL I_{SEG} vs V_{OUT}

Typical Performance Curves (Continued)

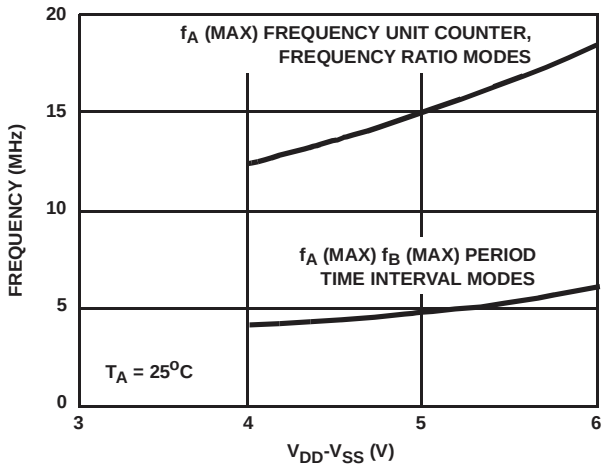


FIGURE 8. f_A(MAX), f_B(MAX) AS A FUNCTION OF SUPPLY

Description

INPUTS A and B

The signal to be measured is applied to INPUT A in frequency period, unit counter, frequency ratio and time interval modes. The other input signal to be measured is applied to INPUT B in frequency ratio and time interval. f_A should be higher than f_B during frequency ratio.

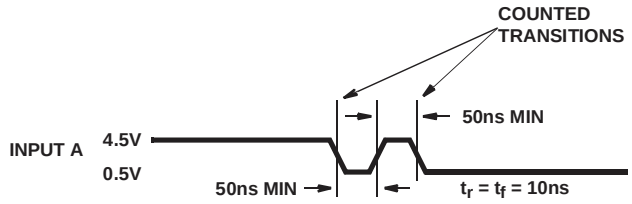


FIGURE 9. WAVEFORM FOR GUARANTEED MINIMUM f_A(MAX) FUNCTION = FREQUENCY, FREQUENCY RATIO, UNIT COUNTER

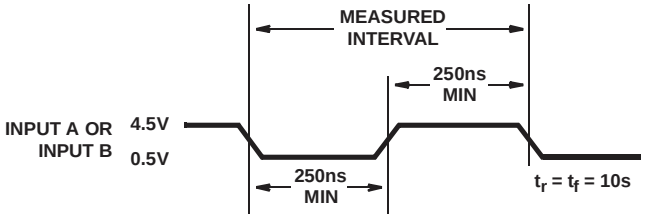


FIGURE 10. WAVEFORM FOR GUARANTEED MINIMUM f_B(MAX) AND f_A(MAX) FOR FUNCTION = PERIOD AND TIME INTERVAL

Both inputs are digital inputs with a typical switching threshold of 2.0V at V_{DD} = 5.0V and input impedance of 250kΩ. For optimum performance, the peak-to-peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs

Note that the amplitude of the input should not exceed the device supply (above the V_{DD} and below the V_{SS}) by more than 0.3V, otherwise the device may be damaged.

Multiplexed Inputs

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the function desired. This is achieved by connecting the appropriate Digit driver output to the inputs. The function, range and control inputs must be stable during the last half of each digit output, (typically 125µs). The multiplexed inputs are active high for the common anode ICM7226A and active low for the common cathode ICM7226B.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplexed inputs as shown in the application circuits.

Table 1 shows the functions selected by each digit for these inputs.

TABLE 1. MULTIPLEXED INPUT FUNCTIONS

INPUT	FUNCTION	DIGIT
FUNCTION INPUT Pin 4	Frequency	D1
	Period	D8
	Frequency Ratio	D2
	Time Interval	D5
	Unit Counter	D4
	Oscillator Frequency	D3
RANGE INPUT Pin 21	0.01s/1 Cycle	D1
	0.1s/10 Cycles	D2
	1s/100 Cycles	D3
	10s/1K Cycles	D4
	Enable External Range Input	D5
CONTROL INPUT Pin 1	Display Off	D4 and Hold
	Display Test	D8
	1MHz Select	D2
	External Oscillator Enable	D1
	External Decimal Point Enable	D3
External DP INPUT Pin 20	Decimal point is output for same digit that is connected to this input.	

Function Input

The six functions that can be selected are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio** and **Oscillator Frequency.**

The implementation of different functions is done by routing the different signals to two counters, called “Main Counter” and “Reference Counter”. A simplified block diagram of the device for functions realization is shown in Figure 11. Table 2 shows which signals will be routed to each counter in different cases. The output of the Main Counter is the information which goes to the display. The Reference Counter divides its input to 1, 10, 100 and 1000. One of these outputs will be selected through the range selector and drive the enable input of the Main Counter. This means that the Reference Counter, along with its' associated blocks, directs the Main Counter to begin counting and determines the length of the counting period. Note that Figure 11 does not show the complete functional diagram (See the Functional Block Diagram). After the end of each counting period, the output of the Main Counter will be latched and displayed, then the counter will be reset and a new measurement cycle will begin. Any change in the FUNCTION INPUT will stop the present measurement without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION INPUT is changed. In all cases, the 1-0 transitions are counted or timed.

TABLE 2. INPUT ROUTING

FUNCTION	MAIN COUNTER	COUNTER
Frequency (f_A)	Input A	100Hz (Oscillator $\div 10^5$ or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A→B)	Oscillator	Input A Input B
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{OSC})	Oscillator	100Hz (Oscillator $\div 10^5$ or 10^4)

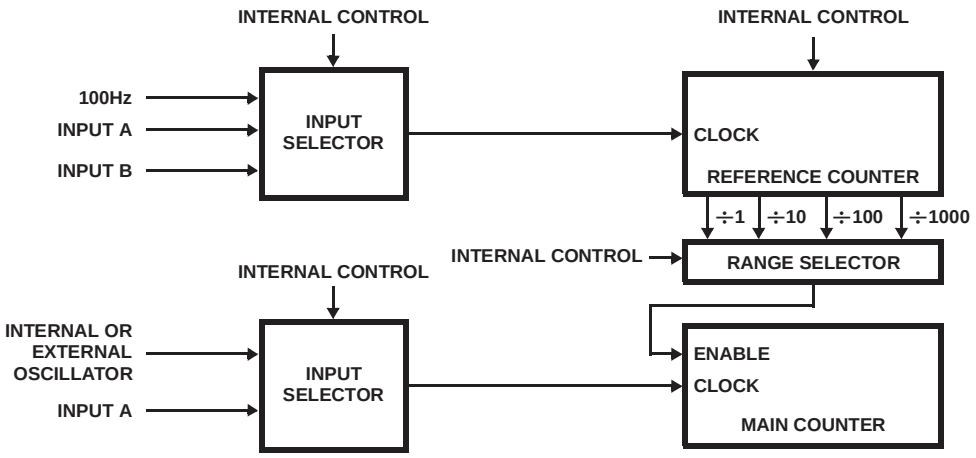


FIGURE 11. SIMPLIFIED BLOCK DIAGRAM OF FUNCTIONS IMPLEMENTATION

Frequency - In this mode input A is counted by the Main Counter for a precise period of time. This time is determined by the time base oscillator and the selected range. For the 10MHz (or 1MHz) time base, the resolutions are 100Hz, 10Hz, 1Hz and 0.1Hz. The decimal point on the display is set for kHz reading.

Period - In this mode, the timebase oscillator is counted by the Main Counter for the duration of 1, 10, 100 or 1000 (range selected) periods of the signal at input A. A 10MHz timebase gives resolutions of 0.1µs to 0.0001µs for 1000 periods averaging. Note that the maximum input frequency for period measurement is 2.5MHz.

Frequency Ratio - In this mode, the input A is counted by the Main Counter for the duration of 1, 10, 100 or 1000 (range selected) periods of the signal at input B. The frequency at input A should be higher than input B for meaningful result. The result in this case is unitless and its resolution can go up to 3 digits after decimal point.

Time Interval - In this mode, the timebase oscillator is counted by the Main Counter for the duration of a 1-0 transition of input A until a 1-0 transition of input B. This means input A starts the counting and input B stops it. If other ranges, except 0.01s/1 cycle are selected the sequence of input A and B transitions must happen 10, 100 or 1000 times until the display becomes updated; note this when measuring long time intervals to give enough time for measurement completion. The resolution in this mode is the same as for period measurement. See the Time Interval Measurement section also.

Unit Counter - In this mode, the Main Counter is always enabled. The input A is counted by the Main Counter and displayed continuously.

Oscillator Frequency - In this mode, the device makes a frequency measurement on its timebase. This is a self test mode for device functionality check. For 10MHz timebase the display will show 10000.0, 10000.00, 10000.000 and Overflow in different ranges.

Range Input

The RANGE INPUT selects whether the measurement period is made for 1,10,100 or 1000 counts of the Reference Counter or it is controlled by EXT RANGE input. As it is shown in Table 1, this gives different counting windows for frequency measurement and various cycles for other modes of measurement.

In all functional modes except Unit Counter, any change in the RANGE INPUT will stop the present measurement without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the RANGE INPUT is changed.

Control Input

Unlike the other multiplexed inputs, to which only one of the digit outputs can be connected at a time, this input can be tied to different digit lines to select combination of controls. In this case, isolation diodes must be used in digit lines to avoid crosstalk between them (see Figure 19). The direction of diodes depends on the device version, common anode or common cathode. For maximum noise immunity at this input, in addition to the 10K resistor which was mentioned before, a 39pF to 100pF capacitor should also be placed between this input and the V_{DD} or V_{SS} (See Figure 19).

Display Off - To disable the display drivers, it is necessary to tie the D4 line to the CONTROL INPUT and have the HOLD input at V_{DD}. While in Display Off mode, the segments and digit drivers are all off, leaving the display lines floating, so the display can be shared with other devices. In this mode, the oscillator continues to run with a typical supply current of 1.5mA with a 10MHz crystal, but no measurements are made and multiplexed inputs are inactive. A new measurement cycle will be initiated when the HOLD input is switched to V_{SS}.

Display Test - Display will turn on with all the digits showing 8s and all decimal points also on. The display will be blanked if Display Off is selected at the same time.

1MHz Select - The 1MHz select mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurement as with a 10MHz crystal. This is done by dividing the oscillator frequency by 10^4 rather than 10^5. The decimal point is also shifted one digit to the right in period and time interval, since the least significant digit will be in µs increment rather than 0.1µs increment.

External Oscillator Enable - In this mode, the signal at EXT OSC INPUT is used as a timebase instead of the on-board crystal oscillator (built around the OSC INPUT, OSC OUTPUT inputs). This input can be used for an external stable temperature compensated crystal oscillator or for special measurements with any external source. The on-board crystal oscillator continues to work when the external oscillator is selected. This is necessary to avoid hang-up problems, and has no effect on the chip's functional operation. If the on-board oscillator frequency is less than 1MHz or only the external oscillator is used, THE OSC INPUT MUST BE CONNECTED TO THE EXT OSC INPUT providing the timebase has enough voltage swing for OSC INPUT (See Electrical Specifications). If the external timebase is TTL level a pullup resistor must be used for OSC INPUT. The other way is to put a 22MΩ resistor between OSC INPUT and OSC OUTPUT and capacitively couple the EXT OSC INPUT to OSC INPUT. This will bias the OSC INPUT at its threshold and the drive voltage will need to be only $2V_{P-P}$. The external timebase frequency must be greater than 100kHz or the chip will reset itself to enable the on-board oscillator.

External Decimal Point Enable - In this mode, the EX DP INPUT is enabled. A decimal point will be displayed for the digit that its output line is connected to this input (EX DP INPUT). Digit 8 should not be used since it will override the overflow output. Leading zero blanking is effective for the digits to the left of selected decimal point.

Hold Input

Except in the **unit counter mode**, when the HOLD input is at V_{DD}, any measurement in progress (before $\overline{\text{STORE}}$ goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD input is at V_{DD}, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the new counter.

$\overline{\text{RST}}$ IN Input

The $\overline{\text{RST}}$ IN is provided to reset the Main Counter, stop any measurement in progress, and enable the display latches, resulting in the all zero display. It is suggested to have a capacitor at this input to V_{SS} to prevent any hangup problem on power up. See application circuits.

EXT RANGE Input

This input is provided to select ranges other than those provided in the chip. In any mode of measurement the duration of measurement is determined by the EXT RANGE if this input is enabled. This input is sampled at 10ms intervals by the 100Hz reference derived from the timebase. Figure 12 shows the relationship between this input, 100Hz reference signal and $\overline{\text{MEAS IN PROGRESS}}$. EXT RANGE can change state anywhere during the period of 100Hz reference by will be sampled at the trailing edge of the period to start or stop measurement.

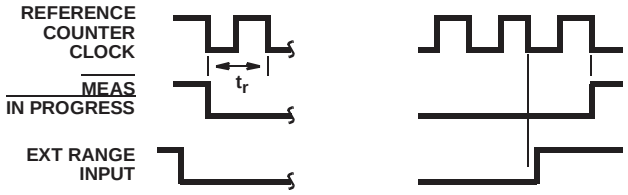


FIGURE 12. EXTERNAL RANGE INPUT TO END OF $\overline{\text{MEASUREMENT IN PROGRESS}}$

This input should not be used for short arbitrary ranges (because of its sampling period), it is provided for very long gating purposes. A way of using the ICM7226 for a short arbitrary range is to feed the gating signal into the INPUT B and run the device in the Frequency Ratio mode. Note that the gating period will be from one positive edge until the next positive edge of INPUT B (0.01s/1 cycle range).

$\overline{\text{MEAS IN PROGRESS}}$, $\overline{\text{STORE}}$, RST OUT Outputs

These outputs are provided for external system interfacing. $\overline{\text{MEAS IN PROGRESS}}$ stays low during measurements and goes high for intervals between measurements. Figure 13 shows the relationship between these outputs for intervals between measurements. All these outputs can drive a low power Schottky TTL. The $\overline{\text{MEAS IN PROGRESS}}$ can drive one ECL load if the ECL device is powered from the same power supply as the ICM7226.

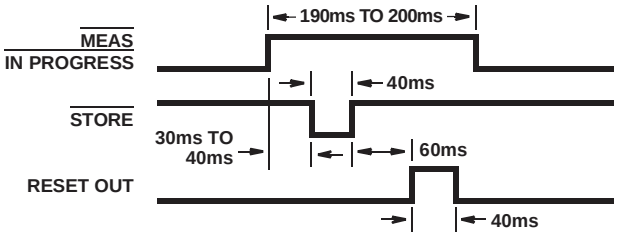


FIGURE 13. $\overline{\text{RESET OUT}}$, $\overline{\text{STORE}}$ AND $\overline{\text{MEASUREMENT IN PROGRESS}}$ OUTPUTS BETWEEN MEASUREMENTS

BCD Outputs

The BCD representation of each display digit is available at the BCD outputs in a multiplexed fashion. See Table 3 for digits truth table. The BCD output of each digit is available when its corresponding digit output is activated. Note that the digit outputs are multiplexed from D8 (MSD) to D1 (LSD). The positive going (ICM7226A, common anode) or the negative going (ICM7226B, common cathode) digit drive signals lag the BCD data by 2µs to 6µs. This starting edge of each digit drive signal should be used to externally latch the BCD data. Each BCD output drives one low power Schottky TTL load. Leading zero blanking has no effect on the BCD outputs.

TABLE 3. TRUTH TABLE BCD OUTPUTS

NUMBER	BCD 8 PIN 7	BCD 4 PIN 6	BCD 2 PIN 17	BCD 1 PIN 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

BUF OSC OUT Output

The BUFFered OSCillator OUTput is provided for use of the on-board oscillator signal, without loading the oscillator itself. This output can drive one low power Schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

Decimal Point Position

Table 4 shows the decimal point position for different modes of ICM7226 operation. Note that the digit 1 is the least significant digit. Table is given for 10MHz timebase frequency.

TABLE 4. DECIMAL POINT POSITIONS

RANGE	FREQUENCY	PERIOD	FREQUENCY RATIO	TIME INTERVAL	UNIT COUNTER	OSCILLATOR FREQUENCY
0.01s/1 Cycle	D2	D2	D1	D2	D1	D2
0.1s/10 Cycle	D3	D3	D2	D3	D1	D3
1s/100 Cycle	D4	D4	D3	D4	D1	D4
10s/1K Cycle	D5	D5	D4	D5	D1	D5
External	N/A	N/A	N/A	N/A	N/A	N/A

Overflow Indication

When overflow happens in any measurement it will be indicated on the decimal point of the digit 8. A separate LED indicator can be used. Figure 14 shows how to connect this indicator.

LED overflow indicator connections: Overflow will be indicated on the decimal point output of digit 8.

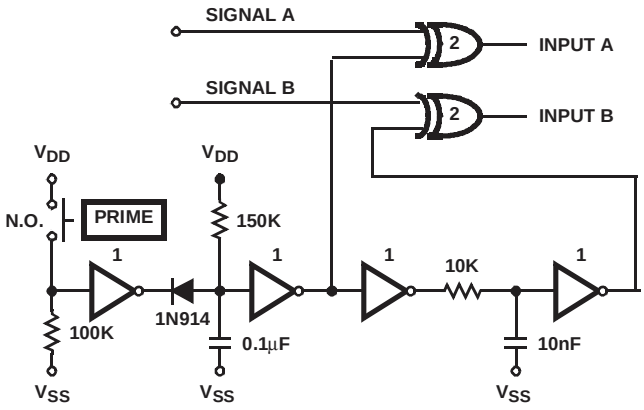
DEVICE	CATHODE	ANODE
ICM7226A	Decimal Point	D8
ICM7226B	D8	Decimal Point

FIGURE 14. SEGMENT IDENTIFICATION AND DISPLAY FONT

Time Interval Measurement

When in the **time interval** mode and measuring a single event, the ICM7226A and ICM7226B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval". The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

Priming can be easily accomplished using the circuit in Figure 15.



DEVICE	TYPE
1	CD4049B Inverting Buffer
2	CD4070B Exclusive - OR

FIGURE 15. PRIMING CIRCUIT, SIGNALS A AND B BOTH HIGH OR LOW

Following the priming procedure (when in single event or 1 cycle range) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7226A and ICM7226B as the first alternating signal states automatically prime the device. See Figure 1.

During any time interval measurement cycle, the ICM7226A and ICM7226B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.

Oscillator Considerations

The oscillator is a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35Ω. Among suitable crystals is the 10MHz CTS KNIGHTS ISI-002.

For a specific crystal and load capacitance, the required g_M can be calculated as follows:

$$g_M = \omega^2 C_{IN} C_{OUT} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where $C_L = \left(\frac{C_{IN} C_{OUT}}{C_{IN} + C_{OUT}}\right)$

C_O = Crystal Static Capacitance

R_S = Crystal Series Resistance

C_{IN} = Input Capacitance

C_{OUT} = Output Capacitance

$\omega = 2\pi f$

The required g_M should not exceed 50% of the g_M specified for the ICM7226 to insure reliable startup. The OSCillator INPUT and OUTPUT pins each contribute about 4pF to C_{IN} and C_{OUT}. For maximum stability of frequency, C_{IN} and C_{OUT} should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used, it may be desirable to use a crystal which is neither 10MHz or 1MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate is:

$f_{MUX} = \frac{f_{OSC}}{2 \times 10^4}$ for 10MHz mode and $f_{MUX} = \frac{f_{OSC}}{2 \times 10^3}$ for the 1MHz mode. The time between measurements is $\frac{2 \times 10^6}{f_{OSC}}$ in the 10MHz mode and $\frac{2 \times 10^5}{f_{OSC}}$ in the 1MHz mode.

The buffered oscillator output should be used as an oscillator test point or to drive additional logic; this output will drive one low power Schottky TTL load. When the buffered oscillator output is used to drive CMOS or the external oscillator input, a 10kΩ resistor should be added from the buffered oscillator output to V_{DD}.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the EXTERNAL OSCILLATOR INPUT to the OSCILLATOR OUTPUT or INPUT can cause undesirable shifts in oscillator frequency.

Display Considerations

The display is multiplexed at a 500Hz rate with a digit time of 244µs. An interdigit blanking time of 6µs is used to prevent display ghosting (faint display of data from previous digit superimposed on the next digit). Leading zero blanking is provided, which blanks the left hand zeroes after decimal point or any non zero digits. Digits to the right of the decimal point are always displayed. The leading zero blanking will be disabled when the Main Counter overflows.

The ICM7226A is designed to drive common anode LED displays at peak current of 25mA/segment, using displays with V_F = 1.8V at 25mA. The average DC current will be greater than 3mA under these conditions. The ICM7226B is designed to drive common cathode displays at peak current of 15mA/segment using displays with V_F = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current, if required. The Typical Performance Curves show the digit and segment currents as a function of output voltage for common anode and common cathode drivers.

To increase the light output from the displays, V_{DD} may be increased to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

The SEGment and Digit outputs in both the ICM7226A and ICM7226B are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals. External latching should be down on the leading edge of the digit signal.

Accuracy

In a Universal Counter, crystal drift and quantization errors cause errors. In **frequency, period** and **time interval** modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter, and in these modes, an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/^{O}C will cause a measurement error of 20ppm/^{O}C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode maximum accuracy is obtained with high frequency inputs and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 16. In **time interval** measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 17. In **frequency ratio** measurement can be more accurately obtained by averaging over more cycles of INPUT B as shown in Figure 18.

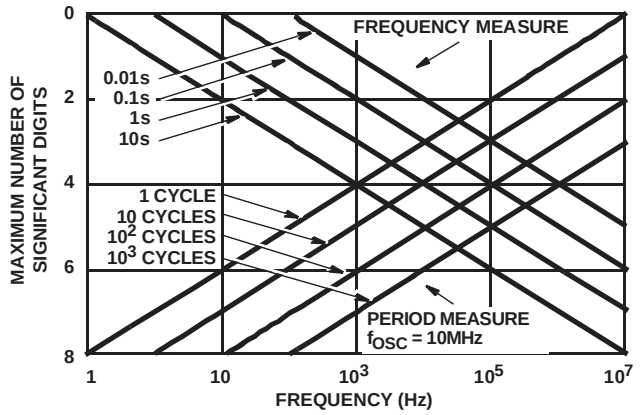


FIGURE 16. MAXIMUM ACCURACY OF FREQUENCY AND PERIOD MEASUREMENTS DUE TO LIMITATIONS OF QUANTIZATION ERRORS

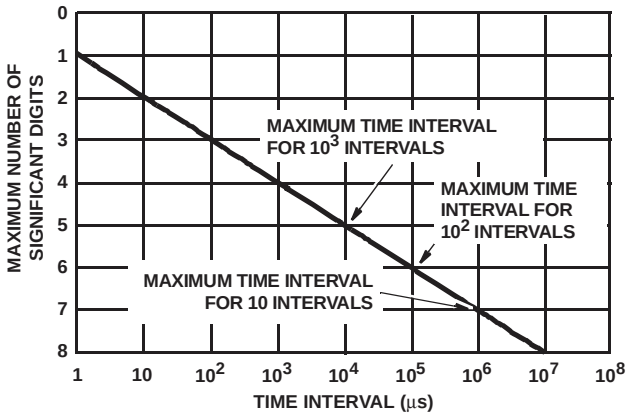


FIGURE 17. MAXIMUM ACCURACY OF TIME INTERVAL MEASUREMENT DUE TO LIMITATIONS OF QUANTIZATION ERRORS

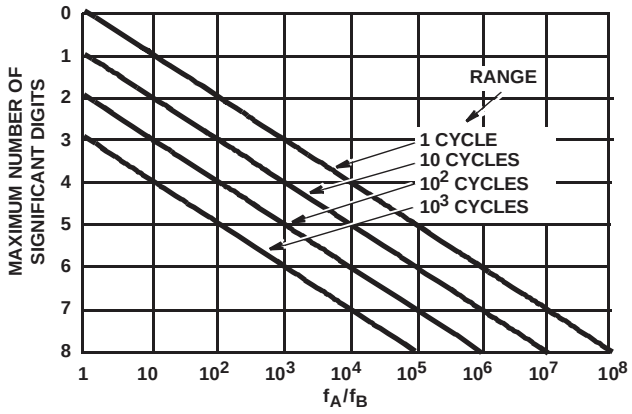
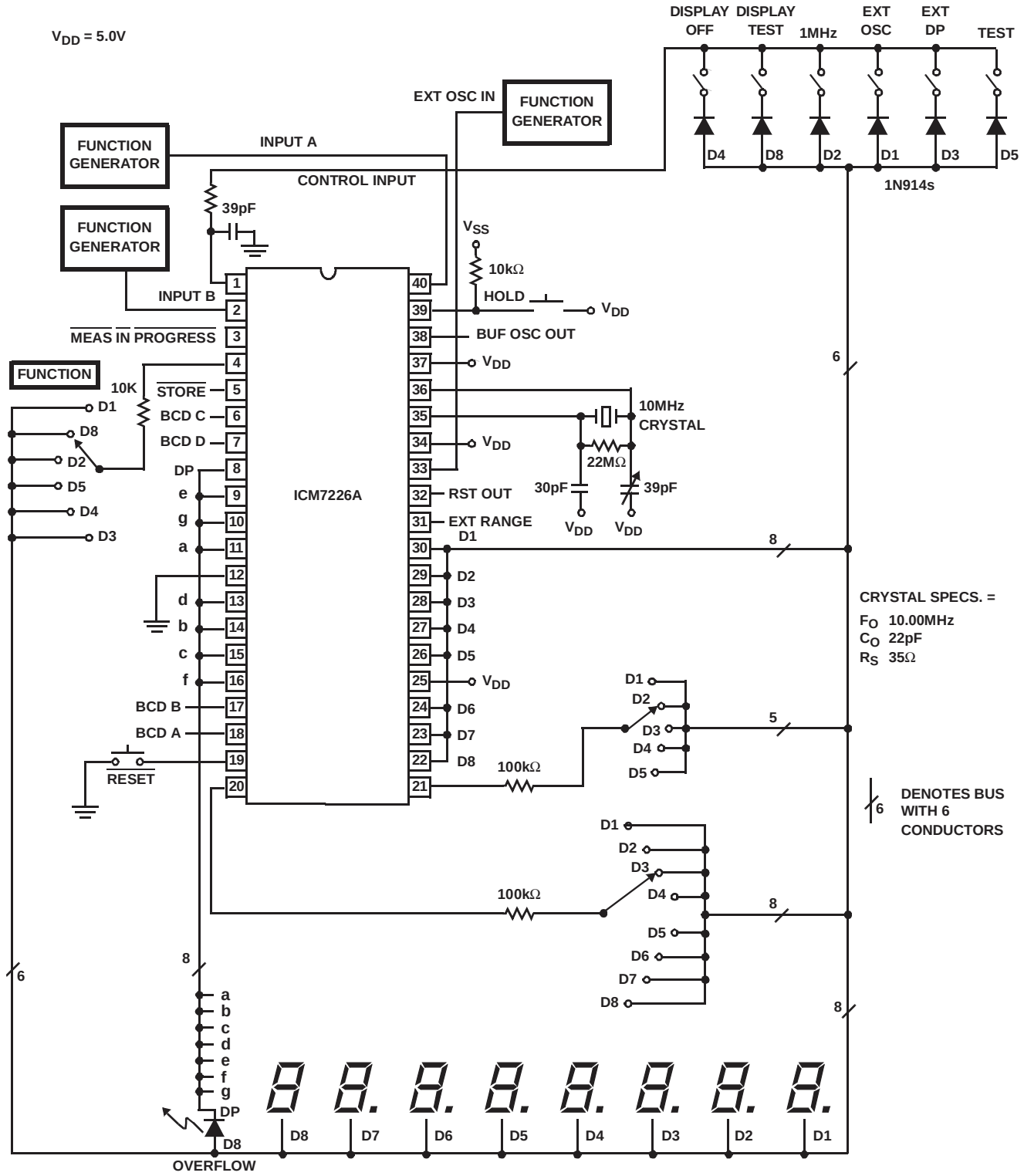


FIGURE 18. MAXIMUM ACCURACY FOR FREQUENCY RATIO MEASUREMENT DUE TO LIMITATION OF QUANTIZATION ERRORS

Test Circuit



DEVICE	CATHODE	ANODE
ICM7226A	DP	D8
ICM7226B	D8	DP

NOTE: Overflow will be indicated on the decimal point output of digit 8.

FIGURE 19.

Typical Applications

The ICM7226 has been designed as a complete stand alone Universal Counter, or used with prescalers and other circuitry in a variety of applications. Since INPUT A and INPUT B are digital inputs, additional circuitry will be required in many applications, for input buffering, amplification, hysteresis, and level shifting to obtain the required digital voltages. For many applications a FET source follower can be used for input buffering, and an ECL 10116 line receiver can be used for amplification and hysteresis to obtain high impedance input, sensitivity and bandwidth. However, cost and complexity of this circuitry can vary widely, depending upon the sensitivity and bandwidth required. When TTL prescalers or input buffers are used, a pull up resistors to V_{DD} should be used to obtain optimal voltage swing at INPUTS A and B. If prescalers aren't required, the ICM7226 can be used to implement a minimum component Universal Counter as shown in Figure 20.

For input frequencies up to 40MHz, the circuit shown in Figure 21 can be used to implement a **frequency and period counter**. To obtain the correct value when measuring frequency and period, it is necessary to divide the 10MHz oscillator frequency down to 2.5MHz. In doing this the time between measurements is lengthened to 800ms and the display multiplex rate is decreased to 125Hz.

If the input frequency is prescaled by ten, the oscillator frequency can remain at either 10MHz or 1MHz, but the decimal point must be moved. Figure 22 shows use of a ÷10 prescaler in **frequency counter** mode. Additional logic has been added to enable the ICM7226 to count the input directly in **period** mode for maximum accuracy.

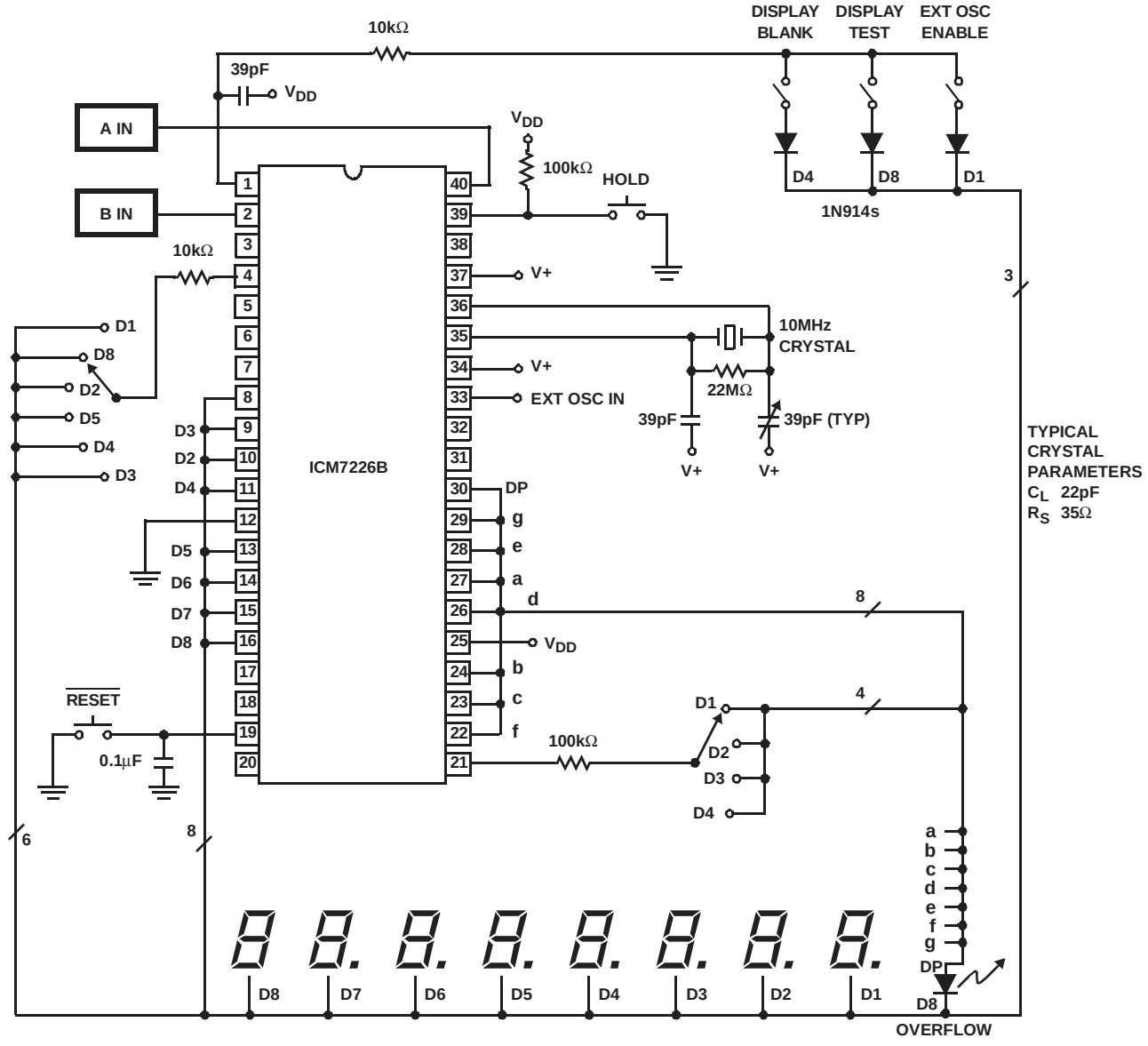


FIGURE 20. 10MHz UNIVERSAL COUNTER

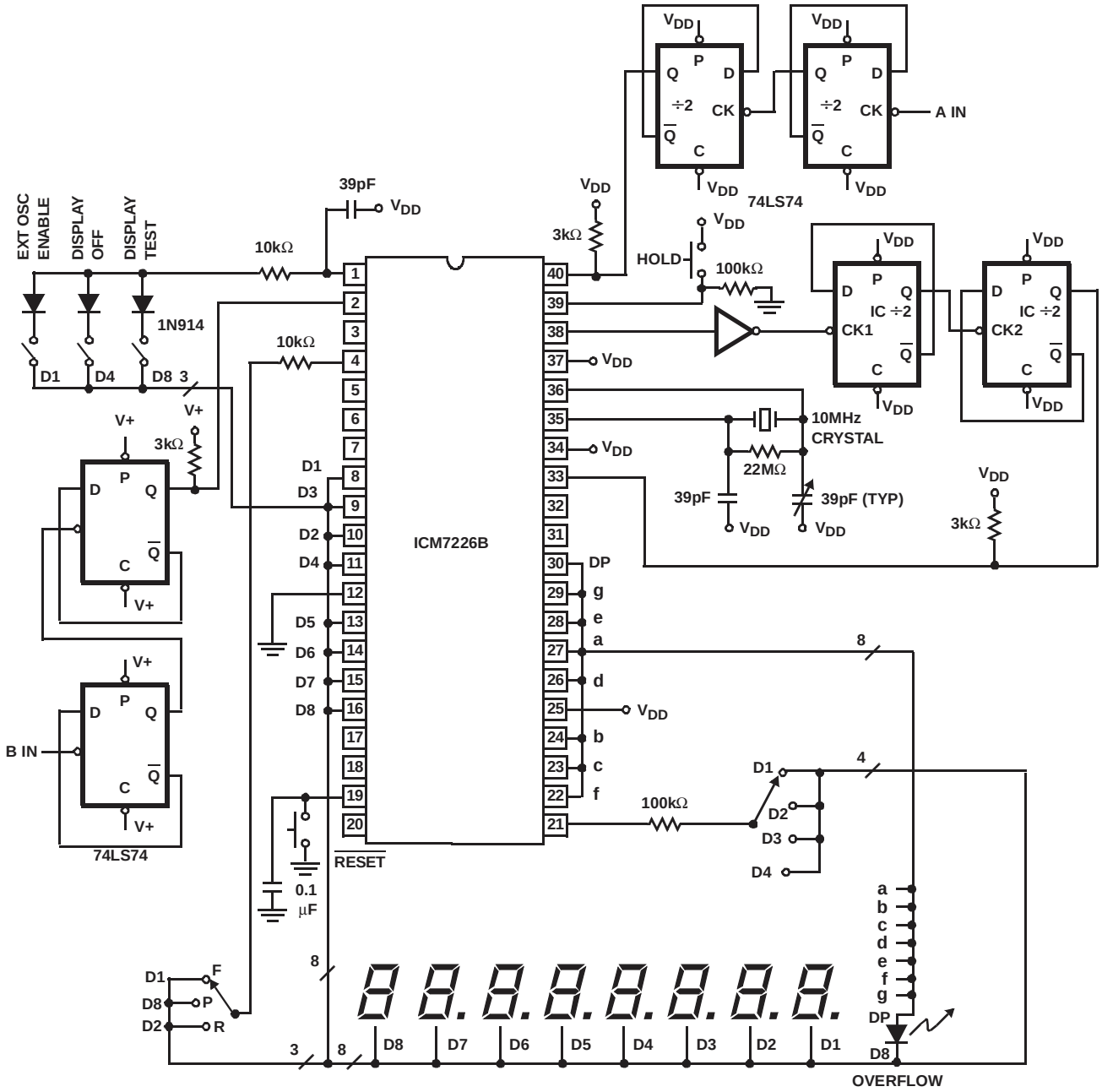


FIGURE 21. 40MHz FREQUENCY, PERIOD COUNTER

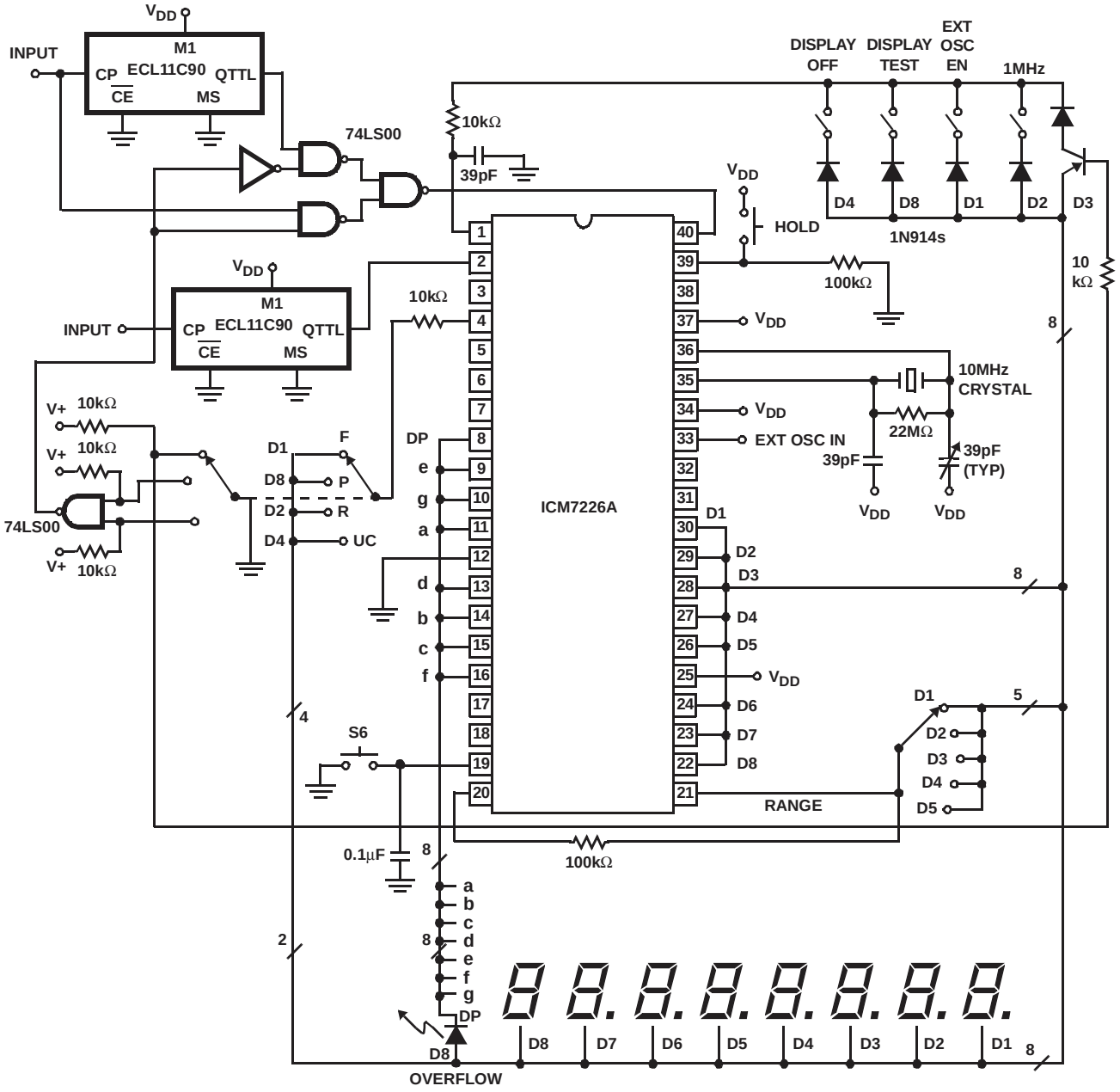


FIGURE 22. 100MHz MULTI-FUNCTION COUNTER

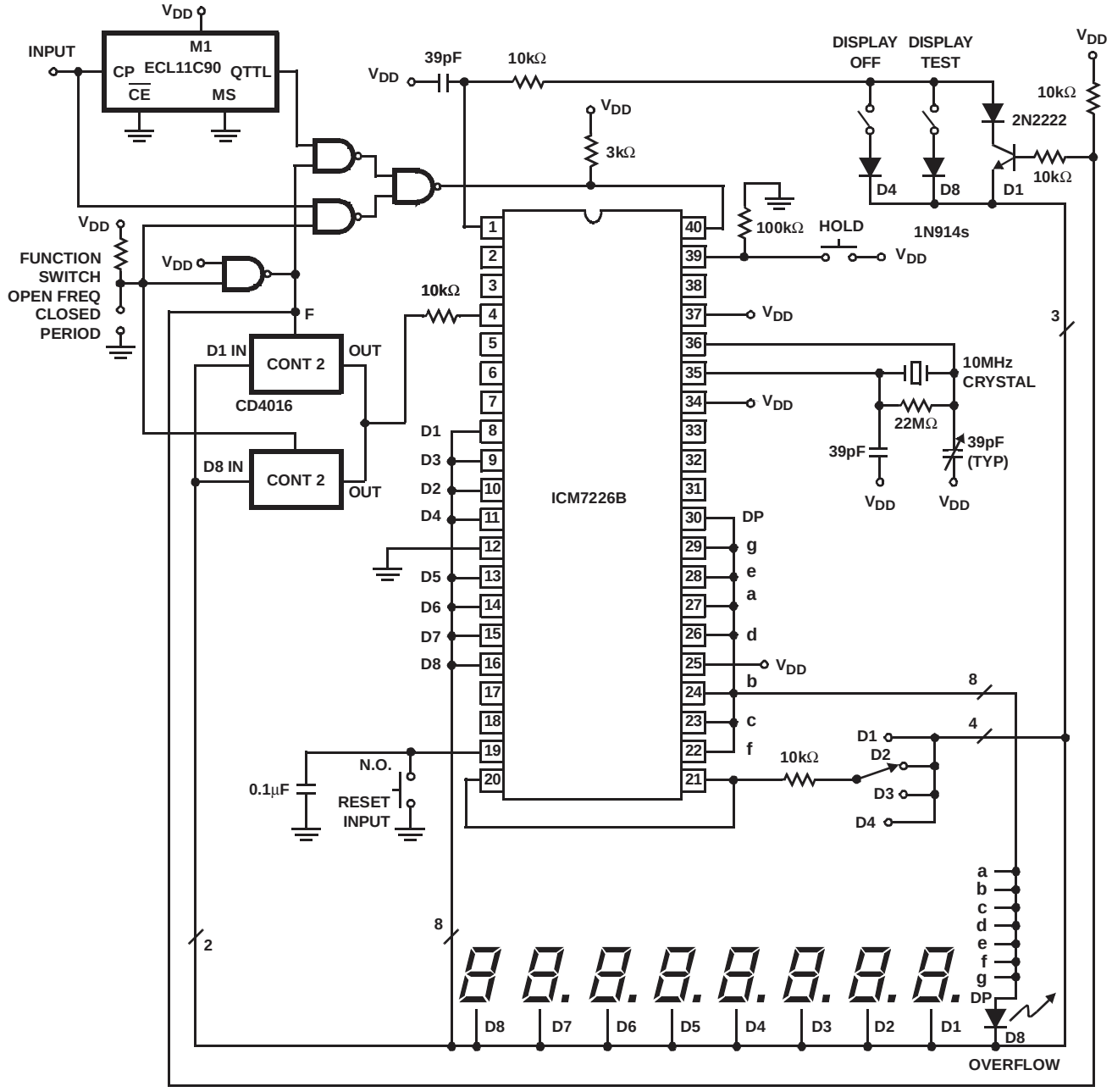


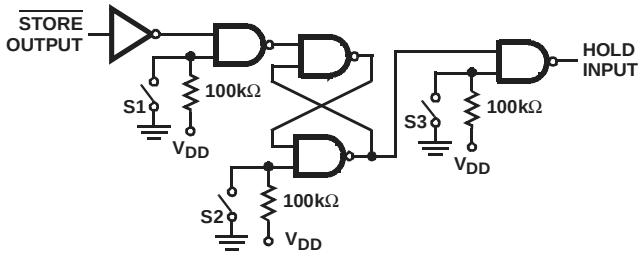
FIGURE 23. 100MHz FREQUENCY, PERIOD COUNTER

Figure 23 shows the use of a CD4016 analog multiplexer to multiplex the digital outputs back to the FUNCTION Input. Since the CD4016 is a digitally controlled analog transmission gate, no level shifting of the digit output is required. CD4051s or CD4052s could also be used to select the proper inputs for the multiplexed input on the ICM7226 from 2-bit or 3-bit digital inputs. These analog multiplexers may also be used in systems in which the mode of operation is controlled by a microprocessor rather than directly from front panel switches. TTL multiplexers such as the 74LS153 or 74LS251 may also be used, but some additional circuitry will be required to convert the digit output to TTL compatible logic levels.

The circuit shown in Figure 24 can be used in any of the circuit applications shown to implement a single measurement mode of operation. This circuit uses the $\overline{\text{STORE}}$ output to put the ICM7226 into a hold mode. The HOLD input can also be used to reduce the time between measurements. The circuit shown in Figure 25 puts a short pulse into the HOLD input a short time after STORE goes low. A new measurement will be initiated at the end of the pulse on the HOLD input. This circuit reduces the time between measurements to about 40ms from 200ms; use of the circuit shown in Figure 25 on the circuit shown in Figure 21 will reduce the time between measurements from 800ms to about 160ms.

Using LCD Display

Figure 26 shows the ICM7226 being interfaced to LCD displays, by using its BCD outputs and 8 digit lines to drive two ICM7211 display drivers.



SWITCH	FUNCTION
S1	Open-Single Meas Mode Enabled
S2	Closed-Initiate New Measurement
S3	Closed-Hold Input

FIGURE 24. SINGLE MEASUREMENT CIRCUIT FOR USE WITH ICM7226

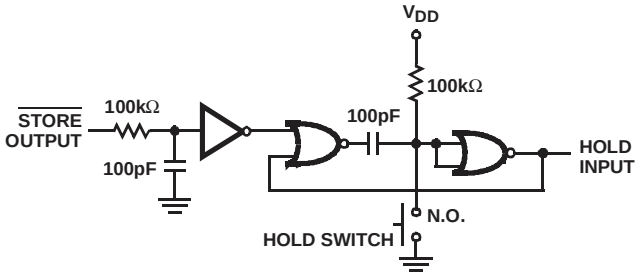


FIGURE 25. CIRCUIT FOR REDUCING TIME BETWEEN MEASUREMENTS

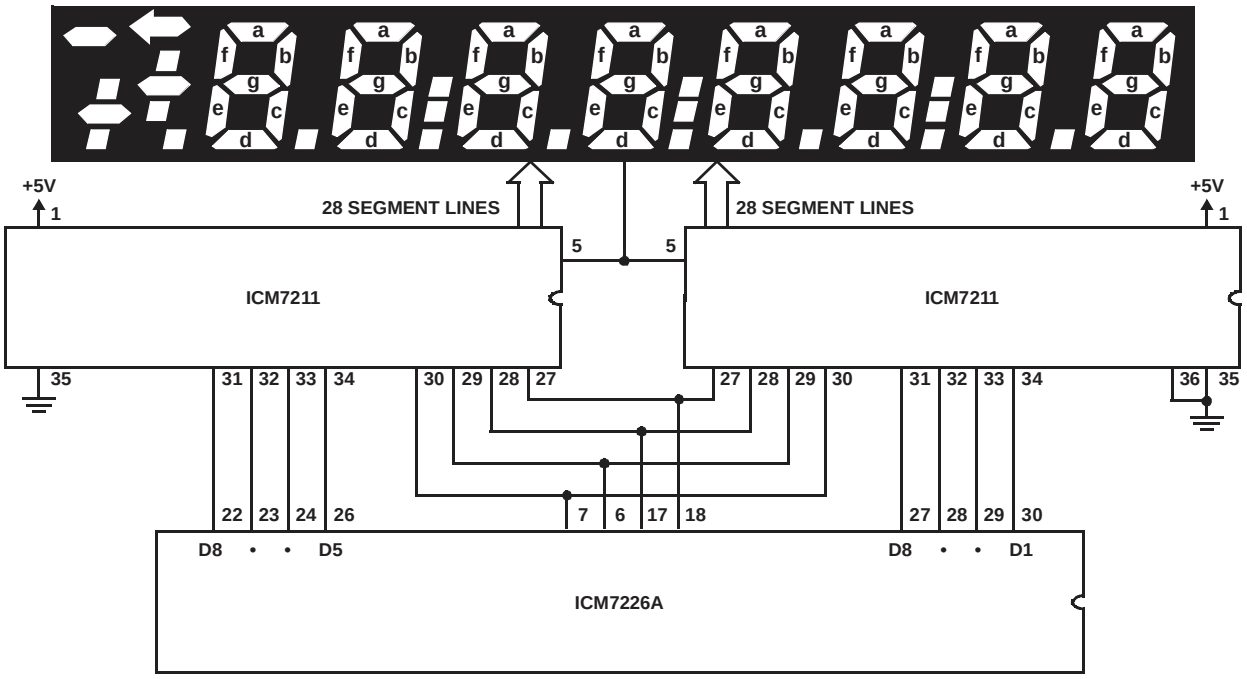


FIGURE 26. 10MHz UNIVERSAL COUNTER SYSTEM WITH LCD DISPLAY

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