

# PCI Express Development Kit Stratix<sup>®</sup> II GX Edition

## **Getting Started User Guide**



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ii Getting Started User Guide PCI Express Development Kit, Stratix II GX Edition



## Contents

### Chapter 1. About This Kit

Introduction	1–1	_
Kit Features	1–1	_
Documentation	1–3	3

#### **Chapter 2. Getting Started**

Introduction	2–1
Before You Begin	2–1
Check the Kit Contents	2–2
Inspect the Board	2–2
Hardware Requirements	2–3
Software Requirements	2–4
Software Installation	
Installing the PCI Express Development Kit, Stratix II GX Edition CD-ROM Contents	2–5
Installing the Quartus II Software and MegaCore Functions	2–6
Licensing Considerations	2–7
Using the Demo Application and Example Design	2–8
Data Flow Block Diagram	2–8
Install Drivers and PCI Express Development Board	
Finish Installing the Drivers and the Development Board, Run the Demo Application	. 2–10
Developing and Using Applications on the PCI Express Board	

#### Appendix A. Using the Parallel Flash Loader

Introduction	A–1
Hardware Setup	A–1
Parallel Flash Loader Tutorial	
Launch the Quartus II Development Tool	A–2
Prepare Application File for Downloading	
Set Up the Programming Download	
Reprogramming the PCI Express Demonstration Program	

### **Additional Information**

Revision History	Info-i
How to Contact Altera	Info-i
Typographic Conventions	Info-ii

**Altera Corporation** 



## 1. About This Kit

### Introduction

The PCI Express Development Kit, Stratix II GX Edition provides everything you need to develop and test a complete PCI Express system based on the Stratix II GX device.

The development kit includes these kit features and documentation:

- The Stratix II GX PCI Express development board
- Quartus® II Software, Development Kit Edition (DKE), and MegaCore IP Library DVD
- PCI Express Development Kit, Stratix II GX Edition CD-ROM
- Design examples
- Power supply, cables, and documentation

## **Kit Features** This section briefly describes the PCI Express Development Kit, Stratix II GX Edition features.

- *The Stratix II GX PCI Express Development Board*—a prototyping platform that allows you to develop and prototype high-speed bus interfaces as well as evaluate Stratix II GX transceiver performance.
- For specific information about board components and interfaces, refer to the *Stratix II GX EP2SGX90 PCI Express Development Board Reference Manual*.
  - Design Examples—The design examples (available on the CD-ROM) are useful for a variety of hardware applications and let you quickly begin board prototyping and device verification.
  - PCI Express Development Kit Application & Drivers—The kit's application and drivers (available on the CD-ROM) allow you to process memory read and write transactions to the board. In addition, you can initiate memory or DMA transaction pairs (read and write), as well as read the various configuration and DMA registers.

- Quartus II Software, Development Kit Edition (DKE)—The Quartus II software (available on the DVD) provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software integrates into nearly any design environment, with interfaces to industry-standard EDA tools. The kit includes:
  - The SOPC Builder system development tool
  - A one-year Quartus II software license, Windows platform only
  - The Quartus II DKE software license allows you to use the product for 12 months. After 12 months, you must purchase a renewal subscription to continue using the software. For more information, refer to the Altera website at **www.altera.com**.
- MegaCore IP Library—This library (available on the DVD) contains Altera IP MegaCore functions. You can evaluate the MegaCore functions using the OpenCore<sup>®</sup> Plus feature, which allows you to do the following:
  - Simulate the behavior of a MegaCore function within your system
  - Verify the functionality of your design, as well as quickly and easily evaluate its size and speed
  - Generate time-limited device programming files for designs that include MegaCore functions
  - Program a device and verify your design in hardware

You only need to purchase a license for a MegaCore function when you are completely satisfied with its functionality and performance, and want to take your design to production.

IP

The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use an Altera IP function in production designs.

### Documentation

The PCI Express Development Kit, Stratix II GX Edition contains the following documents:

- *Readme file*—Contains special instructions and refers to the kit's documentation.
- PCI Express Development Kit, Stratix II GX Edition Getting Started User Guide— (this document) Describes how to start using the kit.
- Stratix II GX EP2SGX90 PCI Express Development Board Reference Manual—Provides specific information about the board's components and interfaces, steps for using the board, and pin-outs and signal specifications.



### 2. Getting Started

### Introduction

The PCI Express Development Kit, Stratix II GX Edition is a complete PCI Express prototyping and testing kit based on the Stratix II GX device. With this kit, you can perform device qualification testing, memory read and write transactions to the board, read the various configuration and direct memory access (DMA) registers, and use the DMA engine in the example design to write to system DDR2 memory.

In addition to providing a PCI Express development board, the kit also includes all of the hardware and software development tools, as well as the documentation and accessories you need to begin developing PCI Express systems using the Stratix II GX device.

This user guide will familiarize you with the contents of the kit and guide you through the PCI Express development board setup. Using this guide, you can do the following:

- Inspect the contents of the kit
- Install the development tool software
- Set up licensing
- Use the demo application and example design to:
  - Perform memory read and write transactions on the board
  - Read configuration and DMA registers
- Use the development software to:
  - Set up and prepare new application designs
  - Program new designs into the development board

### Before You Begin

Before using the kit or installing the software, be sure to check the kit's contents and inspect the board to verify that you received all of the items listed in this section. If any of the items are missing, contact Altera before you proceed.

You should also verify that your computer hardware and software meet the kit's system requirements. To develop PCI Express applications, Altera recommends using two computers:

- Computer #1, as the PCI Express host system, to communicate with the board and to support the graphical user interface (GUI) for the demonstration application.
- Computer #2, as the development host for application development and to support programming of the PCI Express development board.

#### **Check the Kit Contents**

The PCI Express Development Kit, Stratix II GX Edition (ordering code: DK-PCIE-2SGX90N) contains the following items:

- Stratix II GX PCI Express development board with an EP2SGX90FF40C3NES Stratix II GX device
- PCI Express Development Kit, Stratix II GX Edition CD-ROM, which includes:
  - PCI Express example design
  - PCI Express development kit application and device drivers
  - Design examples
  - Stratix II GX EP2SGX90 PCI Express Development Board Reference Manual
  - Schematic and board design files
- One-year license of Quartus II Software Development Kit Edition (DKE), Windows only platform
- USB-Blaster<sup>™</sup> download cable
- Power supply and adapters for North America, Europe, the United Kingdom, and Japan
- Heatsink/fan combination and board standoff hardware
- Complete documentation
  - PCI Express Development Kit, Stratix II GX Edition Getting Started User Guide (this document)
  - *Quartus II Installation & Licensing for Windows*

#### **Inspect the Board**

Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

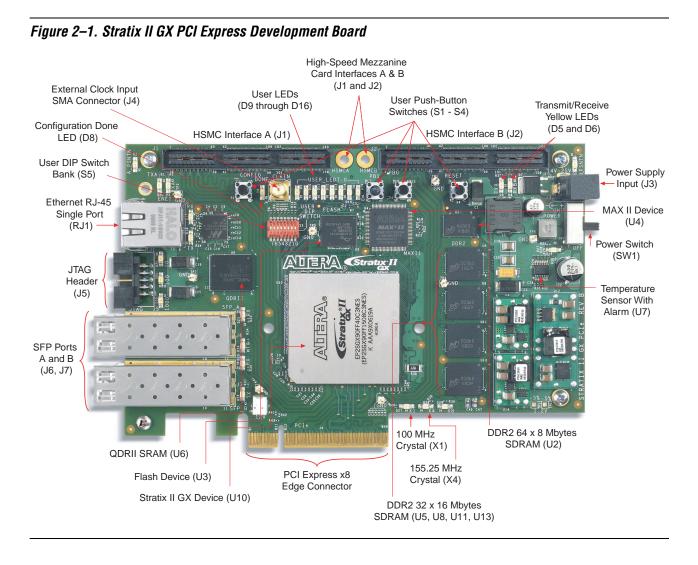


Without proper anti-static handling, the Stratix II GX PCI Express development board can be damaged.

Verify that all components are on the board and appear intact.

I

In typical applications with the PCI Express development board, a heatsink is not necessary. However under extreme conditions the board may require the use of additional cooling to stay within operating temperature guidelines. Power consumption and thermal modeling should be done to determine whether additional cooling is necessary. In the event that it is, a heatsink/fan combination has been provided for your convenience.





Refer to the *Stratix II GX EP2SGX90 PCI Express Development Board Reference Manual* (available on the PCI Express Development Kit, Stratix II GX Edition CD-ROM) for information on the board's components.

#### Hardware Requirements

To run the pre-installed demo application design requires only a single computer, Computer #1, with an x8 PCI Express slot to hold the Stratix II GX PCI Express development board.

Application development, however, also requires a second computer, Computer #2, that is loaded with the Quartus II software as a programming host. This setup provides the flexibility needed for downloading different device programming files to the development board.



The Quartus II software requires some minimum system requirements; refer to the *Quartus II Installation & Licensing for Windows* document for details.

The PCI Express Development Kit, Stratix II GX Edition provides all of the other hardware needed to use the board. This document assumes that the development board is plugged into a computer with a PCIe x8 slot. However, an external power supply and cables have been provided to run the board external to a PCIe chassis.



Do not connect the external power supply to the PCIe board if it is being powered from the backplane PCIe x8 slot.

To use this power supply when the board is NOT installed in computer #1, place the power switch (SW1) in the OFF position and connect the power cable to the board. Plug the other end into a power outlet. To power up the board, place the power switch (SW1) in the ON position. When power is supplied to the board, the LED (D19) illuminates.

If the board does not power up after the power cable is connected, ensure that the power switch (SW1) is in the ON position.

#### **Software Requirements**

Ensure that you adhere to the following software requirements:

- Windows XP operating system running on both computers
- Quartus II software version 7.2 or later.
- For the latest Quartus II software updates, please check the Altera website, **www.altera.com**.



Refer to the *Quartus II Installation & Licensing for Windows* document for further information on the Quartus II system software requirements, especially heeding the following:

• A web browser, Microsoft Internet Explorer version 5.0 or later or Firefox version 2.0 or later, to use Quartus II Help. You need

a web browser to register the Quartus II software and request license files. Refer to "Licensing Considerations" on page 2–7.

• Version 2.0 or later of the .NET framework. Refer to page 2–11 for the .NET related issue.

The instructions in this section explain how to install the following:

- PCI Express Development Kit, Stratix II GX Edition CD-ROM
- PCI Express Development Kit, Stratix II GX Edition demo application and drivers
- The Quartus II Software, Development Kit Edition DVD, including MegaCore functions from the MegaCore IP Library

#### Installing the PCI Express Development Kit, Stratix II GX Edition CD-ROM Contents

Perform this installation on Computer #1.

The PCI Express Development Kit, Stratix II GX Edition CD-ROM contains the following items:

- PCI Express Development Kit, Stratix II GX Edition GUI application and drivers
- Example design programming files
- PCI Express Development Kit, Stratix II GX Edition Getting Started User Guide (this document)
- Stratix II GX EP2SGX90 PCI Express Development Board Reference Manual

To install the PCI Express Development Kit, Stratix II GX Edition CD-ROM, perform the following steps:

- 1. Insert the PCI Express Development Kit, Stratix II GX Edition CD-ROM into your CD-ROM drive.
- 2. The CD-ROM should start an auto-install process.
- If it does not, browse to the CD-ROM drive and double click on the **setup.exe** file.
- 3. Follow the online instructions to complete the installation process.

Software

Installation

The installation program copies the PCI Express Development Kit, Stratix II GX Edition files to your hard-disk, installs the software drivers and application, and creates an icon in **Programs > Altera > Stratix II GX PCI Express Kit** *<version***#>** (Windows Start menu), which you can use to launch the development kit GUI.

When the installation is complete, the PCI Express Development Kit, Stratix II GX Edition installation program creates the directory structure shown in Figure 2–2, where *<path>* is the PCI Express Development Kit, Stratix II GX Edition installation directory for development kits associated with a specific version of the Quartus II software.

Figure 2–2. PCI Express Development Kit Installed Directory Structure

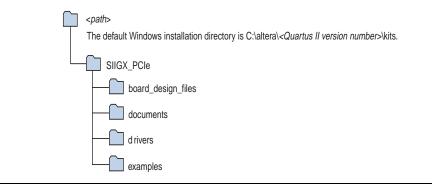


Table 2–1 lists the file directory names and a description of their contents.

Table 2–1. Installed F	ile Directory Names and Description of Contents
Directory Name	Description of Contents
board_design_files	Contains the board design and production test files. You can use the board design files as a starting point for creating your own prototype board.
documents	Contains the documentation related to the development kit.
drivers	Contains the <b>install.bat</b> file, which installs the demo application's driver files and the <b>pcie.exe</b> file.
examples	Contains the example design files for the PCI Express Development Kit, Stratix II GX Edition.

#### Installing the Quartus II Software and MegaCore Functions

Perform this installation on Computer #2.

Refer to *Installing the Quartus II Software* in the *Quartus II Installation & Licensing for Windows* for software installation instructions. After installing the software, request and install a license to enable it.

	For information on obtaining a license file, refer to "Licensing Considerations" on page 2–7.
	To use the Quartus II software included with the kit, you must first obtain a license file. A Quartus II DKE software license is included with the kit.
	During the installation of the Quartus II software, you are given the option to install the MegaCore IP Library. When prompted to do so, choose to install the MegaCore IP Library and follow the on-screen instructions.
Licensing Considerations	Before using the Quartus II software, you must request a license file from the Altera web site at <b>www.altera.com/licensing</b> and install it on your computer. When you request a license file, Altera emails you a <b>license.dat</b> file that enables the software.
	To license the Quartus II software, you need:
	<ul><li>Your network interface card (NIC) ID.</li><li>The kit serial number, which appears both on the outside of the development kit box and on the CD-ROM.</li></ul>
	Your NIC ID is a 12-digit hexadecimal number that identifies your computer. Networked (or floating-node) licensing requires a NIC ID or server host ID. When obtaining a license file for network licensing, use the NIC ID from the computer that will issue the Quartus II licenses to distributed users over a network. You can find the NIC ID for your card by typing "ipconfig /all" at a command prompt. Your NIC ID is the number on the physical address line, without the dashes.
	To obtain a license, perform the following steps.
	<ol> <li>Point your web browser to the Altera web site at www.altera.com/licensing.</li> </ol>

- 2. In the **Development Kit Licensing** list, select **Licensing for RoHS Compliant Development Kits**.
- 3. Follow the on-line instructions to request your license. A license file is emailed to you.
  - Before installing your license, close the following software if it is running on your computer:

- The Quartus II software
- The MAX+PLUS<sup>®</sup> II software
- The LeonardoSpectrum<sup>™</sup> synthesis tool
- The Synplify software
- The ModelSim<sup>®</sup> simulator
- The Precision RTL Synthesis Software
- 4. To install your license, refer to *Specifying the License File* in *Quartus II Installation & Licensing for Windows*, which is included with the kit.

### Using the Demo Application and Example Design

The kit provides an example design file and an easy-to-use demo application with a custom GUI. Using the demo application GUI you can:

- Specify endpoint (PCI Express x8 MegaCore function) DMA read, write, and loop commands
- Specify memory read/write and loop commands
- Read various configuration and DMA registers

In this section, you perform the following tasks:

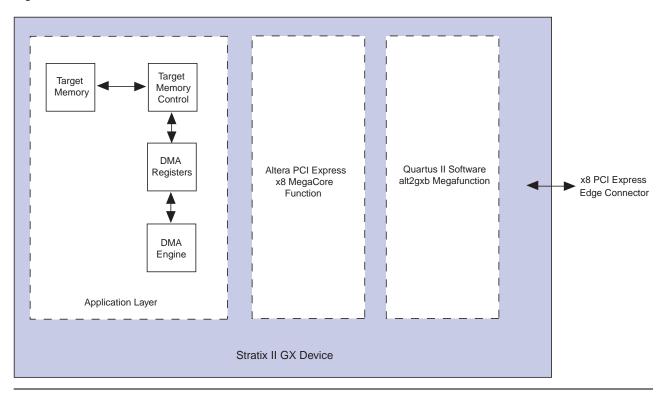
- Install the demo application drivers and PCI Express development board
- Perform memory read and write transactions on the board
- Read configuration and DMA registers
- The Stratix II GX PCI Express development board ships with a pre-installed example design. For instructions on installing the example design or any other design to the flash memory on the board, refer to Appendix A, Using the Parallel Flash Loader.

#### **Data Flow Block Diagram**

Figure 2–3 shows a block diagram of the data flow from the x8 PCI Express edge connector through the Stratix II GX device block, which includes the application layer, Altera PCI Express x8 MegaCore function, and the Quartus II software alt2gxb megafunction.

The kit's demo application allows for memory read and write transactions to the development board. In addition, the kit's example design (**SIIGX\_PCIe\_Example\_Design.sof**) has a DMA engine that allows the development board to write to system memory.

Figure 2–3. Stratix II GX Device Block



#### **Install Drivers and PCI Express Development Board**

As stated in the "Hardware Requirements" on page 2–3, for a flexible setup that allows you to download different programming files to the on-board Stratix II GX device, you need two computers. Specify computer #1 as the development board host computer, and computer #2 as the Quartus II programming host computer.



This section discusses the example design and the development board host computer (computer #1). For information on using the Quartus II programming host computer (computer #2), refer to Appendix A, Using the Parallel Flash Loader.

To install the demo application drivers and PCI Express development board, use the following steps:

To install the drivers, you need to have administrator privileges on your computer.

From computer #1:

- 1. Install the PCI Express Development Kit, Stratix II GX Edition CD-ROM.
- 2. Open the **Drivers** directory, and double-click the **install.bat** file.
- 3. After the **install.bat** file finishes copying files and installing the drivers, shut down computer #1.
- 4. Ensure that the Power slide switch is in the OFF position on the PCI Express development board and insert the board into an x8 PCI Express slot.

# Finish Installing the Drivers and the Development Board, Run the Demo Application

In this section, you finish installing the demo application drivers and the PCI Express development board, then run the demo application.

- If you want to download a programming file that is different than the kit's pre-installed example design file, refer to Appendix A, Using the Parallel Flash Loader.
- 1. Start computer #1.
- 2. When the Windows XP **Found New Hardware Wizard** appears (Figure 2–4), click **Next**.

#### Figure 2-4. Found New Hardware Wizard Window

Found New Hardware Wizard	
	Welcome to the Found New Hardware Wizard
	This wizard helps you install software for:
	Altera PCI Express Megafunction Beta
	If your hardware came with an installation CD or floppy disk, insert it now.
	What do you want the wizard to do?
	Install the software automatically (Recommended)
	Install from a list or specific location (Advanced)
	Click Next to continue.
	<back next=""> Cancel</back>

3. When the **Hardware Installation** dialog box appears (Figure 2–5), click **Continue Anyway**.

Figure 2–5. Hardware Installation Window

	The software you are installing for this hardware:
_	Altera PCI Express Megafunction Beta
	has not passed Windows Logo testing to verify its compatibility with Windows XP. ( <u>Tell me why this testing is important.</u> )
	Continuing your installation of this software may impair or destabilize the correct operation of your system either immediately or in the future. Microsoft strongly recommends that you stop this installation now and contact the hardware vendor for software that has passed Windows Logo testing.
	destabilize the correct operation of your system either immediately or in the future. Microsoft strongly recommends that you stop this installation now and contact the hardware

- 4. Click **Finish** in the **Completing the Found New Hardware Wizard** to finish installing the drivers.
- 5. To start the demo application GUI, run the kit's demo application from the shortcut, Start >Altera > PCI Express Development Kit, Stratix II GX Edition *<version*#>, or execute the pcie.exe file found in the *<path*>\stratixIIGX\_2sgx90\_pcie\drivers directory.
- If you receive an "Application Error" message when launching the demo application, please install version 2.0 or later versions of the .NET framework. Some Windows versions do not have runtime DLL for the .NET application. The .NET framework application can be downloaded from the following location: http://www.microsoft.com/downloads/details.aspx?FamilyId

=262D25E3-F589-4842-8157-034D1E7CF3A3&displaylang=en

- 6. Configure the parameters in the Altera PCI Express Demo Kit Application window (Figure 2–6) as follows:
  - Under **Commands**, turn on **EP DMA Loop**.
  - Under Address/Size:
    - Type 0x0000000 in the **Address Offset** box.
    - Type 2048 in the **Transfer Length** box.
    - Type 1000 in the **Iterations** box.
    - Select **Random Packet** in the **Data Type** list.

7. Click **Execute**. The following message appears,

```
"***SUCCESS***".
```

The demo kit application can be configured to perform other tests including memory read and write transactions on the board, loop read and write transactions; it can also read the various configuration and DMA registers. For more information about performing other tests, refer to *AN* 431: *PCI Express-to-DDR2 SDRAM Reference Design*.

Figure 2–6. Altera PCI Express Demo Kit Application Window

		<ul> <li>EP DMA Loop</li> <li>RC Mem Loop</li> </ul>	Command Information — Command — EP DMA Access Done	Data Flow 1) EP DMA READ 2) EP DMA WRITE
Transfer Leng	th Iterations	Data Type Random Packet	Configuration Registers	0x1172 0x0007 0x0107 0x010 0x010 0x01
* * * t Data	Received Data	Address Hex Code ASCII code	DMA Registers	0x00 0x00 0xff 0x302ff648
70046 Tw.F 54930 E.IO d7cab . e4410 M.D.	54770046 Tw.F 45054930 E.IO 04ad7cab . 4dfe4410 M.D.	J_ Rnd Xtr	Dma_addr64 Dma_size Dma_ctr1 Register Update	0x0000000 0x0000800 0x0000040
92439 *.\$9 c10da 2, f5346 1.SF	2aa92439 *.\$9 322c10da 2, 31ef5346 1.SF	Execute	Offset Bytes	Configuration
	Read Transfer Leng 2048 2048 * * * t Data e103c .n.< 70046 Tw.F 154930 E.I0 47cab .l. 154930 E.I0 47cab .l. 154930 E.I0 47cab .l. 154930 E.I0 152451 E.I0 152451 E.I0 15346 I.SF	Read         C         RC Mem Write           Transfer Length         Iterations           2048         1000           1000         1000             * * *           t Data         Received Data           re103c .n.<	Read       C RC Mem Write       C RC Mem Loop         Transfer Length       Iterations       Data Type         2048       1000       Random Packet           2048       1000       Random Packet           * * * <ul> <li>Address</li> <li>Hex Code</li> <li>ASCII code</li> <li>Rod Xir</li> </ul> * 103c       .n.       046e103c       .n.         70046       Tw.F       54770046       Tw.F         54930       E.IO       45054930       E.IO         04ad7cab<].	Read       EP DMA Write       EP DMA Loop         Read       RCMem Write       RCMem Loop       EP DMA Access         Transfer Length       Iterations       Data Type         2048       1000       Random Packet       Image: Configuration Registers         ****       Address       Image: Command EP DMA Access       Image: Configuration Registers         ****       Image: Command EP DMA Access       Image: Configuration Registers         ****       Image: Command EP DMA Access       Image: Command EP DMA Access         Image: Command EP DMA Access       Image: Command EP DMA Access         Image: Command EP DMA Access       Image: Command EP DMA Access         Image: Command EP DMA Access       Image: Command EP DMA Access         Image: Command EP DMA Access       Image: Command EP DMA Access         Image: Command EP DMA Access       Image: Command EP DMA Access         Image: Command EP DMA Access       Image: Command EP DMA Access         Image: Command EP DMA Access       Image: Command EP DMA Access         Image: Command EP DMA Access       Image: Command EP DMA Access         Image: Command EP DMA Access       Image: Command EP DMA Access         Image: Command EP DMA Access       Image: Command EP DMA Access         Image: Command EP DMA Access       Image: Command EP DMA Access

### Developing and Using Applications on the PCI Express Board

When developing PCI Express applications, downloading a new PCI Express SOF from Computer #2 to the development board on Computer #1 will likely produce a hardware malfunction.

The best way to configure the FPGA on the development board is to use the alternative hardware setup and POF loading method described in Appendix A. This requires creating a POF on Computer #2, removing the development board, and programming its flash memory while the board operates as a stand-alone unit.

It is possible to download an SOF with the development board installed in Computer #1, but the download has to occur while Computer #1 is booting up and before Windows configures the PCI Express bus. When successful, this method works faster than removing the board for programming, but requires the luck of good timing. This means that the download may fail and you may have to power down and try again.

When developing a non-PCI Express design, remove the board from Computer #1, install the stand-off support pegs, connect the provided separate power supply, and run any experiments in this stand-alone configuration.



### Appendix A. Using the Parallel Flash Loader

### Introduction

Chapter 2, "Getting Started," described the procedure for starting up and running a pre-installed example design using computer #1, the development board host computer. However, application development also requires a second computer to be a Quartus II programming host and a parallel flash loader (PFL).

From the Quartus II programming host computer, computer #2, you can download a programming file to the development board that is different from the kit's pre-installed example design file. The tutorial in this appendix guides you through the following tasks:

- Installing the AlteraPFL provided for flash memory programming and FPGA configuration
- Using the PFL to configure the FPGA with an application.

### **Hardware Setup**

Altera provides a USB-Blaster cable with the kit for downloading programming files from the Quartus II programming host computer to the development board installed on the other computer. Connect the USB-Blaster cable's 10-pin female plug to the Stratix II GX device's JTAG header (J5) on the development board. Align the marker line on the cable to pin 1 of the header (J5). Pin 1 of J5 is numbered on the board. Connect the other end of the USB-Blaster cable to the USB port on the computer running the Quartus II software.



- A "Hardware Malfunction" error may occur with some computers when the parallel flash loader loads the flash memory or when you load an SRAM Object File (**.sof**) file into the FPGA. In this case, use the following alternate hardware setup:
- 1. Turn off computer #1 and remove the development board from the PCI Express slot.
- 2. Connect the board to the power supply provided in the kit.
- 3. Turn the on-board power supply switch to the ON position.
- 4. Power up the board.

- 5. Connect the USB-Blaster cable between the board and the Quartus II programming host computer.
- 6. Follow the tutorial steps to program the flash memory.
- 7. Power down the board, remove the power supply, and set the power supply switch to OFF.
- 8. Reinsert the board into the PCI Express slot in computer #1 and turn the computer ON.

### Parallel Flash Loader Tutorial

This tutorial describes how to use the PFL to load an FPGA image into the Common Flash memory Interface (CFI) type flash device and configure the Stratix II GX type FPGA device on the PCI Express development board.

First, you use the Quartus II development tool to prepare and program the MAX<sup>®</sup> II device on the development board with the parallel flash loader. At the same time, you prepare and download an application to the flash device on the board. Finally, using the flash data, the PFL configures the FPGA and activates the application.

The tutorial uses two files included with the development kit:

**pfl2\_sIIgx\_pcie\_3fe.pof**, in the *<path>* **stratixIIGX\_2sgx90\_pcie examplesPFL\_2SGX\_PCIe** directory, is the MAX II Programmer Object File (.pof) that contains a parallel flash loader design.

MyFirstFPGA\_top.sof, in the <path>\Examples\stratixIIGX\_2sgx90\_pcie\examples\MyFirstFP GA directory, contains a simple test design that forces the FPGA to display counting on the development board user LEDs. The SRAM Object File, MyFirstFPGA\_top.sof, is used in the SOF-to-POF file conversion in the "Prepare Application File for Downloading" part of the tutorial.

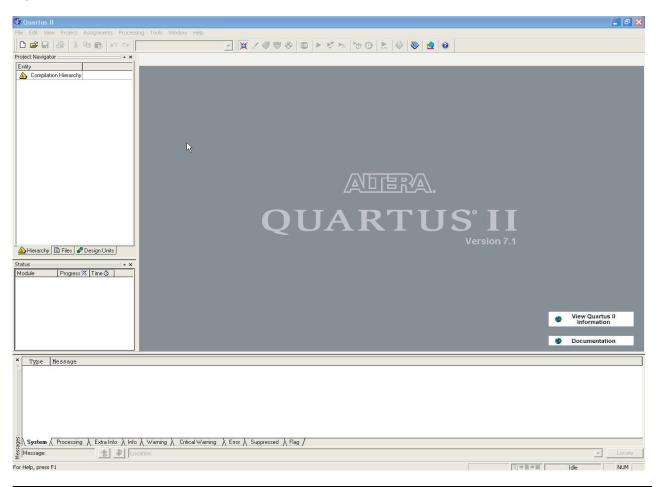
The tutorial contains three parts:

- Launch the Quartus II Development Tool
- Prepare Application File for Downloading
- Set Up the Programming Download

#### Launch the Quartus II Development Tool

Start the Quartus II software (Figure A–1).

Figure A-1. Quartus II Software Interface



#### Prepare Application File for Downloading

To prepare the blink example application for downloading to the flash device, convert **blink\_example.sof**, in the **blink\_example.qar** archive to a POF.

To convert an SOF to a POF, perform the following steps:

- 1. On the File menu, click **Convert Programming Files**.
- 2. Under Output programming file select Programmer Object File (.pof) for the Programming file type.

- 3. Click in the box next to **Configuration device** and select **CFI\_512MB** as the flash size
- 4. Click in the box next to Mode and select Fast Passive Parallel.
- 5. In the **File Name** box, specify a file name for the resulting CFI flash POF. This example uses C:/altera72/kits/SIIGX\_PCIe/Examples /MyFirstFPGA/MyFirstFPGA\_3fe.pof.
- Click Options and in the box next to Start address (Figure A-2) type 0x03FE0000 to set the option bit address. This address must match the option bit address location specified in the PFL MegaWizard<sup>®</sup> interface.
- 7. Click **OK** to close the dialog box.

Figure A–2. Options Dialog Box

<u>Start address (32-bit hexadecimal):</u>	0x0 3FE00	000
	OK	Cancel

8. Under **Input files to convert**, select the **SOF Data** cell and click **Add File**, then browse to the directory containing **MyFirstFPGA\_top.sof**, highlight the file, and click **Open**. This adds the SRAM Object File to the **Convert Programming Files** dialog box (Figure A–3).

Figure A–3. Setting Input Files to Convert

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	Specify the input files to co You can also import input f future use. Conversion setup files — Open Conv					
		cision octup Data			P	
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	Programming file type:	Programmer Object I	File (.pof)		-	
	Options	Configuration device:	CFI_512MB	Mode: Fast Passive I	Parallel 🗾	
	File <u>n</u> ame:	C:/altera/72/kits/SI	GX_PCIe/Examples/My	FirstFPGA/MyFirstFPGA_	3fe.pof	
		Remote/Local updat	e difference fi <u>l</u> e: NONE	Í.	*	
		Memory Map File				
	Input files to convert					
	File/Data area		Properties	Start Address	Add <u>H</u> ex Data	
	SOF Data		Page_0 EP2SGX90FF1508	<auto></auto>		
	Options	(0p.so)	EF230A30FF1306	0x03FE0000	Add <u>S</u> of Data	
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					Down	
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For Help, I	press F1					.// ML

9. Click **Generate** to produce the Programmer Object File that is stored in the flash device.

#### Set Up the Programming Download

- 1. To open the programmer, click on **Programmer** in the Tools menu.
- 2. Click the **Hardware Setup** button and select the download cable you are using, the **USB Blaster** in this example.
- 3. Set **Mode** to **JTAG**. Figure A–4 shows an example of the selections.

Figure A-4. Hardware Setup Selections

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	v	
Server	Port	Add Hardware
Local	LPT1	Remove Hardware
Local	038-0	
	and the second se	Local LPT1

4. Click **Auto Detect** to verify correct setup and to display the MAX II and Stratix II GX devices in the JTAG chain (Figure A–5). You may have to press the **CONFIG** switch, S1, on the board during this process before the flash chip appears in the chain.

Figure A-5. JTAG Chain

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ly	Combinational /	🔔 Hardware Se	tup USB-Blaster [USB-0]							Mode	JTAG		٣	Progress:	0%
Compilation Hierarchy		Enable real-tin	e ISP to allow background pr	ogramming (for MAX II devi	ces)										
		No Start	File	Device	Checksum	Usercode	Program/ Configure	Verily	Blank- Check	Examine	Security Bit	Erase	ISP	IPS File	
		Stop	(none)	EPM570	00000000	00000000	Configure			Constant of the second second			1		
			(none)	CFI_512MB EP25GX90	00000000	(none)									
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5. Right-click on the EPM570 MAX II device in the list, select Change File, then browse to the *<path>\Examples* \stratixIIGX\_2sgx90\_pcie\examples\PFL\_2SGX\_PCIe directory where the pfl2\_sIIgx\_pcie\_3fe.pof is located, then highlight the file and click Open (Figure A–6). The pfl2\_sIIgx\_pcie\_3fe.pof file defines the PFL design for the MAX II device.

Figure A–6. Open the PFL Design File

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		🔊 Start	File	Device	Checksum	Usercode	Program/ Configure	Verily	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP	IPS File	
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- 6. If the flash device is not listed under the EPM570GT100 device as shown in Figure A–6, highlight the EPM570GT100 device in the **Programmer utility** and right click. Select the **Attach Flash Device** option. Otherwise go to step 8 below.
- 7. Highlight and check CFI\_512MB and click OK (Figure A-7).

Figure A–7. Selecting the Flash Device Size

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8. Right-click **CFI\_512MB** and click **Change File**. Browse to the location of the Programmer Object File generated during the SOF-to-POF conversion and click **Open**. This step attaches the flash POF to the MAX II POF. The Programmer should resemble the one shown in Figure A–8.

Figure A–8. Attach Flash POF to MAX II POF

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	Mu Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP IPS	File	
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9. Turn on the check boxes for **Program/Configure** next to **pfl2\_sIIgx\_pcie\_3fe.pof**, **UFM**, **Page\_0**, and **OPTION\_BITS** (Figure A–9).

Fiaure	A-9.	Program	/Configure	Check	Boxes
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Enable real-time	ISP to allow background progr	amming (for MAX II devic	es)			
🏴 Start	File	Device	Checksum	Usercode	Program/ Configure	Verify
🛍 Stop	C:/altera/72/kits/SIIGX_P0 - CFM - UFM	Cl EPM570GT100	002E425A	FFFFFFF	2	
Auto Detect	C:/altera/72/kits/SIIGX_ Page_0 OPTION_BITS	P CFI_512MB	CBE959B1			
避 Add File	<pre>l <none></none></pre>	EP2SGX90	0000000	<none></none>	Ē	

- 10. Click **Start** to program the PFL into the MAX II device as well as program the flash device with the FPGA image. After programming is completed, the PFL configures the FPGA with the data from the flash device. When completed, the application loaded into the FPGA causes the USER\_LED[7..0] lights to display counting.
- If the FPGA is already configured prior to performing the previous steps, the following message may appear in the Message Window:

Info: Device 1 silicon ID is not ready - waiting
for pfl\_flash\_access\_granted to be asserted

In this case, press the **Config** button on the board to reset the FPGA. Operation resumes, allowing the PFL to access the flash device for programming. Figure A–10 shows the error message.



	pe	Nessage	<u>^</u>
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11. After the PFL loads the application to the FPGA, the blink application program activates and the LEDs on the board display counting. If you cycle the power switch, the program reloads from the flash device to the FPGA.

#### **Reprogramming the PCI Express Demonstration Program**

To reprogram the FPGA with the default demonstration program supplied with the kit, repeat the process in "Set Up the Programming Download" on page A–5, except in Step 8, change the file to <path>\Examples\stratixIIGX\_2sgx90\_pcie\examples \DDR2\_to\_PCIe\_ExDsgn\pcie\_ddr2\_3fe.pof.



## **Additional Information**

### **Revision History**

The table below displays the revision history for the chapters in this user guide.

Chapter	Date	Version	Changes Made
Chapter 2	March 2008	1.0.4	Changed installed directory structure.
All	October 2007	1.0.3	Replaced Appendix with Parallel Flash Loader Tutorial and made minor changes in the other chapters
All	April 2007	1.0.2	Added warning not to use external power supply when the Altera <sup>®</sup> Stratix <sup>®</sup> II GX PCI Express development board is powered from the host computer chassis
All	August 2006	1.0.1	Minor edits to flow and kit contents to reflect production version
All	July 2006	1.0.0	First publication

This user guide provides getting started information about the Altera Stratix II GX PCI Express development board.

### How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
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Product literature	Website	www.altera.com/literature
Altera literature services	Email	literature@altera.com
Non-technical support (General)	Email	nacomp@altera.com
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Note to table:

(1) You can also contact your local Altera sales office or sales representative.

**Altera Corporation** 

### Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: <b>Save As</b> dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: <b>\qdesigns</b> directory, <b>d:</b> drive, <b>chiptrip.gdf</b> file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: AN 75: High-Speed Board Design.
Italic type	Internal timing parameters and variables are shown in italic type. Examples: $t_{PIA}$ , $n + 1$ .
	Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <i><file name=""></file></i> , <i><project name="">.pof</project></i> file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
Courier type	Signal and port names are shown in lowercase Courier type. Examples: data1, tdi, input. Active-low signals are denoted by suffix n, e.g., resetn.
	Anything that must be typed exactly as it appears is shown in Courier type. For example: c:\qdesigns\tutorial\chiptrip.gdf. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword SUBDESIGN), as well as logic function names (e.g., TRI) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
••	Bullets are used in a list of items when the sequence of the items is not important.
$\checkmark$	The checkmark indicates a procedure that consists of one step only.
Ĩ	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
4	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.