Nios® II

Nios Development Board

Reference Manual, Stratix II Edition

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Contents

About this Manual

This manual provides component details about the Nios® development board, Stratix™ II Edition.

The following table shows the reference manual's revision history.

Date	Description
July 2005	Updated for the EP2S30 device.
October 2004	Updated the heat sink illustrations.
September 2004	First publication of Nios Development Board Reference Manual, Stratix II Edition

How to Find Information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Click the binoculars toolbar icon to open the Find dialog box.
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This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Introduction

Features Overview

The Nios development board, Stratix II Edition, provides a hardware platform for developing embedded systems based on Altera Stratix II devices. The Nios development board, Stratix II Edition provides the following features:

- A Stratix II FPGA with more than 13,500 adaptive logic modules (ALM) and 1.3 million bits of on-chip memory
- 16 Mbytes of flash memory
- 1 Mbyte of static RAM
- 16 Mbytes of SDRAM
- On board logic for configuring the Stratix II device from flash memory
- On-board Ethernet MAC/PHY device
- Two 5V-tolerant expansion/prototype headers each with access to 41 Stratix II user I/O pins
- CompactFlash™ connector for Type I CompactFlash cards
- Mictor connector for hardware and software debug
- Two RS-232 DB9 serial ports
- Four push-button switches connected to Stratix II user I/O pins
- Eight LEDs connected to Stratix II user I/O pins
- Dual 7-segment LED display
- JTAG connectors to Altera® devices via Altera download cables
- 50 MHz oscillator and zero-skew clock distribution circuitry
- Power-on reset circuitry

General Description

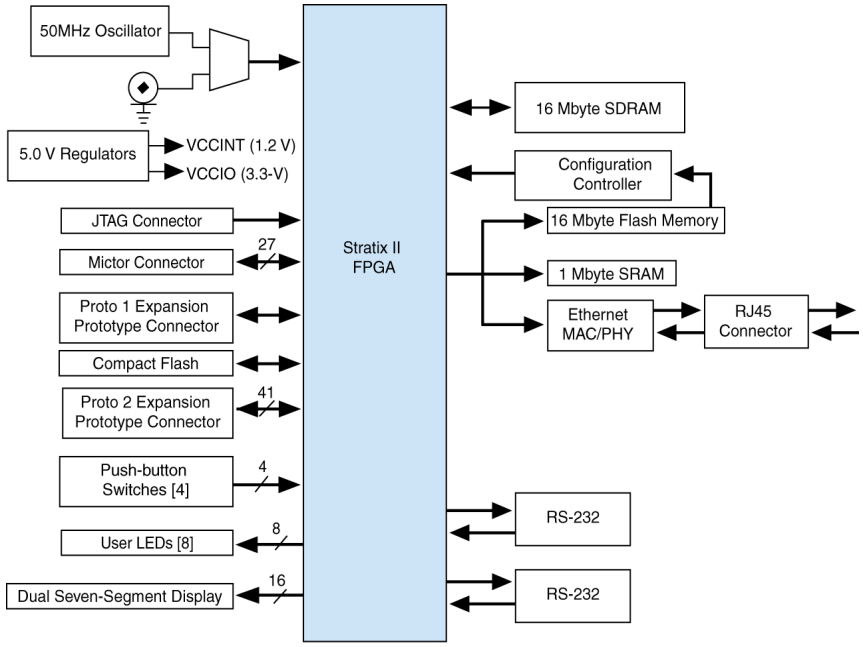
The Nios development board comes pre-programmed with a Nios II processor reference design. Hardware designers can use the reference design as an example of how to use the features of the Nios development board. Software designers can use the pre-programmed Nios II processor design on the board to begin prototyping software immediately.

This document describes the hardware features of the Nios development board, including detailed pin-out information, to enable designers to create custom FPGA designs that interface with all components on the board.

Refer to the Nios II Development Kit, Getting Started User Guide for instructions on setting up the Nios development board and installing Nios II development tools.

Figure 1–1 shows a block diagram of the Nios development board.

Figure 1–1. Nios Development Board, Stratix II Edition Block Diagram



Early shipments of the Nios development board, Stratix II edition use an EP2S60F672C5ES device. This is a fully tested engineering sample (ES) device. However, it has a known issue affecting the M-RAM blocks. The issue can be worked around easily, but some consideration is required when migrating designs based on this device to a non-ES device. There is a label near the FPGA; if the letters "ES" appear on the label, the device is an engineering sample.

For details, refer to the Stratix II FPGA Family Errata Sheet and the documented example designs included in the Nios II Development Kit.

Factory-Programmed Reference Design

When power is applied to the board, on-board logic configures the Stratix II FPGA using hardware configuration data stored in flash memory. When the device is configured, the Nios II processor design in the FPGA wakes up and begins executing boot code from flash memory.

The board is factory-programmed with a default reference design. This reference design is a web server that delivers web pages via the Ethernet port. For further information on the default reference design, see Appendix C, Connecting to the Board via Ethernet.

In the course of development, you may overwrite or erase the flash memory space containing the default reference design. Altera provides the flash image for the default reference design so you can return the board to its default state. See Appendix B, Restoring the Factory Configuration for more information.

Component List

This section introduces all the important components on the Nios development board (see Figure 2–1). A complete set of schematics, a physical layout database, and GERBER files for the development board are installed in the Nios II development kit **documents** directory.

See Figure 2–1 and Table 2–1 on page 2–6 for locations and brief descriptions of all features of the board.

Figure 2–1. Nios Development Board

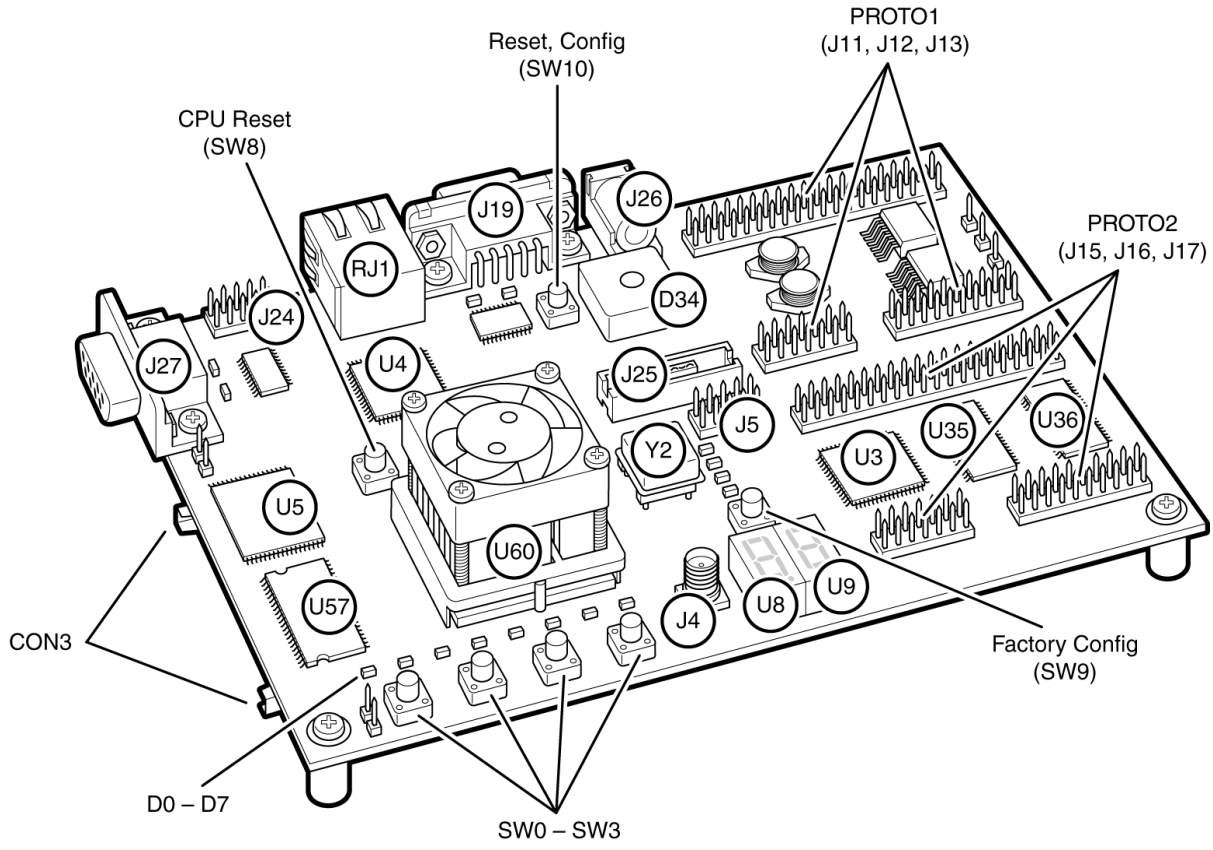


Table 2–1. Nios Development Board, Stratix Edition Components & Interfaces (Part 1 of 2)

Board Designation	Name	Description
Featured Device		
U60	Stratix II FPGA	EP2S60F672C5 or EP2S30F672C5 device with mounted heat sink
User Interface		
SW0 – SW3	Push-button switches	Four momentary contact switches for user input to the FPGA
D0 – D7	Individual LEDs	Eight individual LEDs driven by the FPGA
U8, U9	Seven-segment LEDs	Two seven-segment LEDs to display numeric output from the FPGA
Memory		
U35, U36	SRAM memory	Two SRAM chips combined to form 1 Mbyte of fast, static RAM
U5	Flash memory	16 Mbytes of nonvolatile memory for use by both the FPGA and the configuration controller
U57	SDRAM memory	16 Mbytes of SDRAM
Connectors & Interfaces		
U4, RJ1	Ethernet MAC/PHY	10/100 Ethernet MAC/PHY chip connected to an RJ-45 Ethernet connector
J19, J27	Serial connectors	Two serial connectors with 5 V-tolerant buffers. Supports all RS-232 signals.
PROTO1 (J11, J12, J13)	Expansion prototype connector	Expansion headers connecting to 41 I/O pins on the FPGA. Supplies 3.3V and 5.0V for use by a daughter card.
PROTO2 (J15, J16, J17)	Expansion prototype connector	Expansion headers connecting to 41 I/O pins on the FPGA. Supplies 3.3V and 5.0V for use by a daughter card.
CON3	CompactFlash connector	CompactFlash connector for memory expansion
J25	Mictor connector	Mictor connector for debugging Nios II systems using a First Silicon Solutions (FS2) debug probe.
J24	JTAG connector	Connects to the FPGA allowing hardware configuration from Quartus II software and software debug from the Nios II IDE.
J5	JTAG connector	Connects to the configuration controller
Configuration & Reset		
U3	Configuration controller	Altera EPM7128AE device used to configure the FPGA from flash memory

Table 2–1. Nios Development Board, Stratix Edition Components & Interfaces (Part 2 of 2)		
Board Designation	**Name**	**Description**
SW8	CPU Reset button	Push-button switch to reboot the Nios II processor configured in the FPGA
SW9	Factory Config button	Push-button switch to reconfigure the FPGA with the factory-programmed reference design
SW10	Reset, Config	Push-button switch to reset the board
LED0 – LED3	Configuration status LEDs	LEDs that display the current configuration status of the FPGA
Clock Circuitry		
Y2	Oscillator	50 MHz clock signal driven to FPGA
J4	External clock input	Connector to FPGA clock pin
Power Supply		
J26	DC power jack	17 V DC unregulated power source
D34	Bridge rectifier	Power rectifier allows for center-negative or center-positive power supplies

The sections that follow describe each component in detail.

Stratix II Device (U60)

U60 is a Stratix II FPGA in a 672-pin FineLine BGA® package. Early shipments of the Nios Development Board, Stratix II Edition included an EP2S60F672C5 device. Some early boards used engineering sample parts, indicated by "ES" after the part number. Later shipments of the board use an EP2S30F672C5 device. Table 2–2 lists the device features.

Table 2–2. Stratix II Device Features (Part 1 of 2)		
Feature	**EP2S30**	**EP2S60**
ALMs	13,552	24,176
Adaptive look-up tables (ALUTs)	27,104	48,352
Equivalent LEs	33,880	60,440
M512 RAM blocks	202	329
M4K RAM blocks	144	255
M-RAM blocks	1	2
Total RAM bits	1,369,728	2,544,192
DSP blocks	16	36

Table 2–2. Stratix II Device Features (Part 2 of 2)

Feature	EP2S30	EP2S60
18-bit x 18-bit multipliers	64	144
Enhanced PLLS	2	4
Fast PLLs	4	8
User I/O pins	500	492

The development board provides two separate methods for configuring the Stratix II device:

1. Using the Quartus II software running on a host computer, a designer configures the device directly via an Altera® download cable connected to the Stratix II JTAG header (J24).

2. When power is applied to the board, a configuration controller device (U3) attempts to configure the Stratix II device with hardware configuration data stored in flash memory. For more information on the configuration controller, see "Configuration Controller Device (U3)" on page 2–25.

For Stratix II-related documentation including Stratix II pinout data refer to the Altera Stratix II literature page at **www.altera.com/ literature/lit-stx2.html**.

Early shipments of the board had a heat sink mounted on the Stratix II FPGA. Boards shipped later than May 2005 do not include the heat sink, because thermal management is unnecessary for the majority of FPGA designs for this board. A heat sink maintains the FPGA within its specified thermal operating range, independent of the resource utilization, clock frequency, and operating conditions of the FPGA. The heat sink used on early shipments of the board is produced by Intricast Inc., part number CS1995V01. See **www.intricast.com** for details.

Refer to Altera's *AN185: Thermal Management Using Heat Sinks* for information on using heat sinks with Altera devices.

Push-Button Switches (SW0 - SW3)

SW0 – SW3 are momentary-contact push-button switches and are used to provide stimulus to designs in the Stratix II device. See Figure 2–2. Each switch is connected to a Stratix II general-purpose I/O pin with a pull-up resistor as shown in Table 2–3. Each Stratix II device pin will see a logic 0 when its corresponding switch is pressed.

Table 2–3. Push Button Switches Pin Out Table

Button	Stratix II Pin
SW0	W24
SW1	W23
SW2	Y24
SW3	Y23

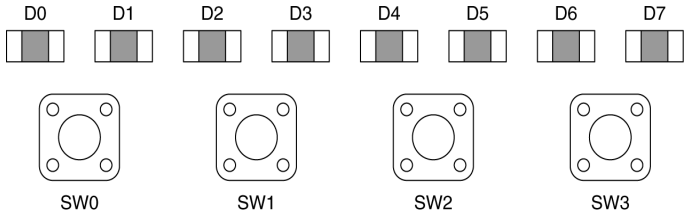
Individual LEDs (D0 - D7)

This Nios development board provides eight individual LEDs connected to the Stratix II device. See Figure 2–2. D0 – D7 are connected to general purpose I/O pins on the Stratix II device as shown in Table 2–4. When the Stratix II pin drives logic 1, the corresponding LED turns on.

Table 2–4. LED Pin Out Table

LED	Stratix II Pin
D0	AD26
D1	AD25
D2	AC25
D3	AC24
D4	AB24
D5	AB23
D6	AB26
D7	AB25

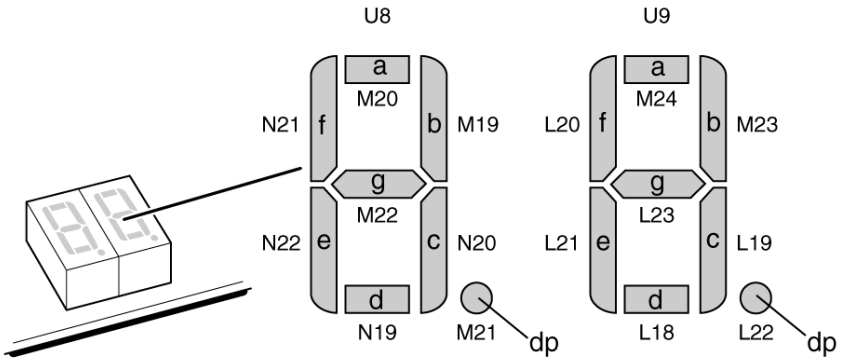
Figure 2–2. Push Button Switches & Individual LEDs



Seven-Segment LEDs (U8 & U9)

U8 and U9 are connected to the Stratix II device so that each segment is individually controlled by a general-purpose I/O pin. When the Stratix II pin drives logic 0, the corresponding LED turns on. See Figure 2–3 for Stratix II pin-out details.

Figure 2–3. Seven-Segment LEDs



SRAM Memory (U35 & U36)

U35 and U36 are IDT IDT71V416S, 512 Kbyte x 16-bit asynchronous SRAM devices. They are connected to the Stratix II device so they can be used by a Nios II embedded processor as general-purpose memory. The two 16-bit devices can be used in parallel to implement a 32-bit wide memory subsystem. The factory programmed Nios II reference design identifies these SRAM devices in its address space as a contiguous 1Mbyte, 32-bit-wide, zero-wait-state main memory.

The SRAM devices share address and data connections with the flash memory and the Ethernet MAC/PHY device. For shared bus information, see Appendix A, Shared Bus Table.

Refer to **www.idt.com** for detailed information about the SRAM devices.

Flash Memory (U5)

U5 is a 16 Mbyte AMD AM29LV128M flash memory device connected to the Stratix II device and can be used for two purposes:

1. A Nios II embedded processor implemented on the Stratix II device can use the flash as general-purpose readable memory and non-volatile storage.

2. The flash memory can hold Stratix II device configuration data that is used by the configuration controller to load the Stratix II device at power-up. See "Configuration Controller Device (U3)" on page 2–25 for related information.

A Nios II processor design in the FPGA can identify the 16 Mbyte flash memory in its address space, and can program new data (either new Stratix II configuration data, Nios II embedded processor software, or both) into flash memory. The Nios II embedded processor software includes subroutines for writing and erasing flash memory.

The flash memory device shares address and data connections with the SRAM chips and the Ethernet MAC/PHY chip. For shared bus information, see Appendix A, Shared Bus Table.

The on-board configuration controller makes assumptions about what-resides-where in flash memory. For details see section "Flash Memory Partitions" on page 2–27.

See **www.amd.com** for detailed information about the flash memory device.

SDRAM Memory (U57)

The SDRAM device (U57) is a Micron MT48LC4M32B2 with PC100 functionality and self refresh mode. The SDRAM is fully synchronous with all signals registered on the positive edge of the system clock.

The SDRAM device pins are connected to the Stratix II device (see Table 2–5). An SDRAM controller peripheral is included with the Nios II development kit, allowing a Nios II processor to view the SDRAM device as a large, linearly-addressable memory.

Table 2–5. SDRAM (U57) Pin Table (Part 1 of 2)

Pin Name	Pin Number	Connects to Stratix II Pin
A0	25	AD4
A1	26	AD3
A2	27	AD5
A3	60	W9
A4	61	W10
A5	62	AB10
A6	63	AF5
A7	64	AE5
A8	65	AC6
A9	66	AF6
A10	24	AA10
A11	21	Y9
BA0	22	AE23
BA1	23	AD23
DQ0	2	W15
DQ1	4	V14
DQ2	5	AA16
DQ3	7	AD16
DQ4	8	AF17
DQ5	10	AD17
DQ6	11	AF18
DQ7	13	AA17
DQ8	74	V16
DQ9	76	AB17
DQ10	77	AF19
DQ11	79	AD18
DQ12	80	AD19

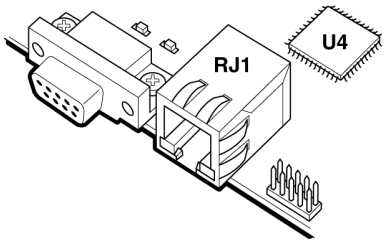
Table 2–5. SDRAM (U57) Pin Table (Part 2 of 2)		
Pin Name	**Pin Number**	**Connects to Stratix II Pin**
DQ13	82	AF20
DQ14	83	AC17
DQ15	85	V17
DQ16	31	AB18
DQ17	33	AF21
DQ18	34	AD20
DQ19	36	AD21
DQ20	37	AF22
DQ21	39	AC18
DQ22	40	W18
DQ23	42	AB19
DQ24	45	AD22
DQ25	47	AE22
DQ26	48	AF24
DQ27	50	AE24
DQ28	51	AB7
DQ29	53	V10
DQ30	54	AA8
DQ31	56	AF3
DQM0	16	AF7
DQM1	71	AD7
DQM2	28	AC7
DQM3	59	AF8
RAS_N	19	AE17
CAS_N	18	AE16
CKE	67	AE20
CS_N	20	AE19
WE_N	17	AE18
CLK	68	AF12

Refer to **www.micron.com** for detailed information.

Ethernet MAC/PHY (U4)

The LAN91C111 (U4) is a mixed signal analog/digital device that implements protocols at 10 Mbps and 100 Mbps. The control pins of U4 are connected to the Stratix II device so that Nios II systems can access Ethernet via the RJ-45 connector (RJ1).See Figure 2–4 on page 2–14. The Nios II development kit includes hardware and software components that allow Nios II processor systems to communicate with the LAN91C111 Ethernet device.

Figure 2–4. Ethernet RJ-45 Connector



The Ethernet MAC/PHY device shares address and data connections with the flash memory and the SRAM chips. For shared bus information, see Appendix A, Shared Bus Table

Refer to **www.smsc.com** for detailed information about the LAN91C111 device.

Serial Port Connectors (J19 & J27)

J19 and J27 are standard DB-9 serial connectors. These connectors are typically used for communication with a host computer using a standard, 9-pin serial cable connected to (for example) a COM port. Level-shifting buffers (U52 and U58) are used between J19 & J27 and the Stratix II device, because the Stratix II device cannot interface to RS-232 voltage levels directly.

J19 and J27 are able to transmit all RS-232 signals. Alternately, the Stratix II design may use only the signals it needs, such as J19's `RXD` and `TXD`. LEDs are connected to the `RXD` and `TXD` signals, giving a visual indication when data is being transmitted or received. Figure 2–5 and Figure 2–6 show the pin connections between the serial connectors and the Stratix II device.

Figure 2–5. Serial Connector J19

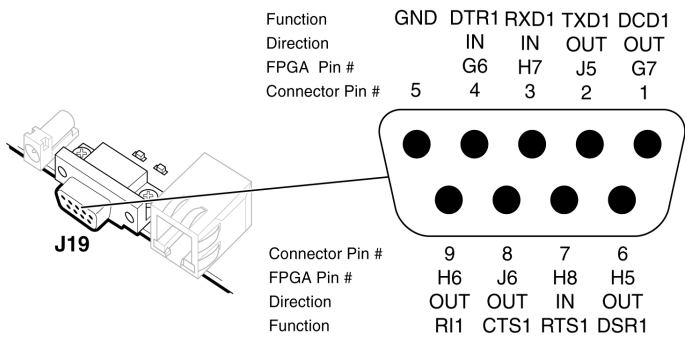
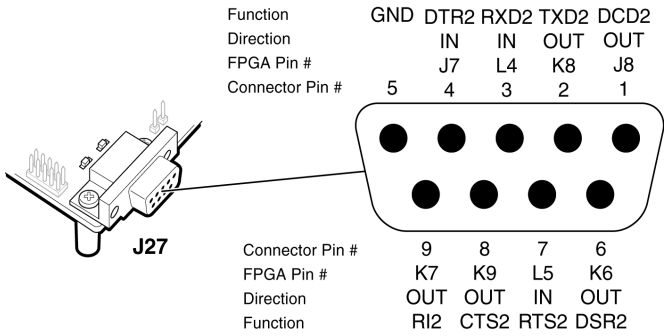


Figure 2–6. Serial Connector J27



Expansion Prototype Connectors (PROTO1 & PROTO2)

PROTO1 and PROTO2 are standard-footprint, mechanically-stable connections that can be used (for example) as an interface to a special-function daughter card. Headers J11, J12, and J13 collectively form PROTO1, and J15, J16 and J17 collectively form PROTO2.

The expansion prototype connector interface includes:

- 41 I/O pins for prototyping. All 41 I/O pins connect to user I/O pins on the Stratix II device. Each signal passes through analog switches to protect the Stratix II device from 5V logic levels. These analog switches are permanently enabled. The output logic-level on the expansion prototype connector pins is 3.3V.
  - PROTO1 switches: U19, U20, U21, U22 and U25
  - PROTO2 switches: U27, U28, U29, U30 and U31
- A buffered, zero-skew copy of the on-board oscillator output from U2.
- A buffered, zero-skew copy of the Stratix II phase-locked loop (PLL) output from U60.

- A logic-negative power-on reset signal.
- Five regulated 3.3V power-supply pins (2A total max load for both PROTO1 & PROTO2).
- One regulated 5V power-supply pin (1A total max load for both PROTO1 & PROTO2).
- Numerous ground connections.

The PROTO1 expansion prototype connector shares Stratix II I/O pins with the CompactFlash connector (CON3). Designs may use either the PROTO1 connector or the CompactFlash connector.

Refer to the Altera web site for a list of available expansion daughter cards that can be used with the Nios development board at **www.altera.com/devkits.**

Figure 2–7, and Figure 2–8 on page 2–17 show connections from the PROTO1 expansion headers to the Stratix II device. Unless otherwise noted, labels indicate Stratix II device pin numbers.

Figure 2–7. PROTO1 Expansion Prototype Connector - J11, J12 & J13

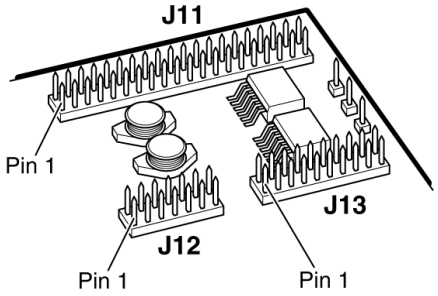
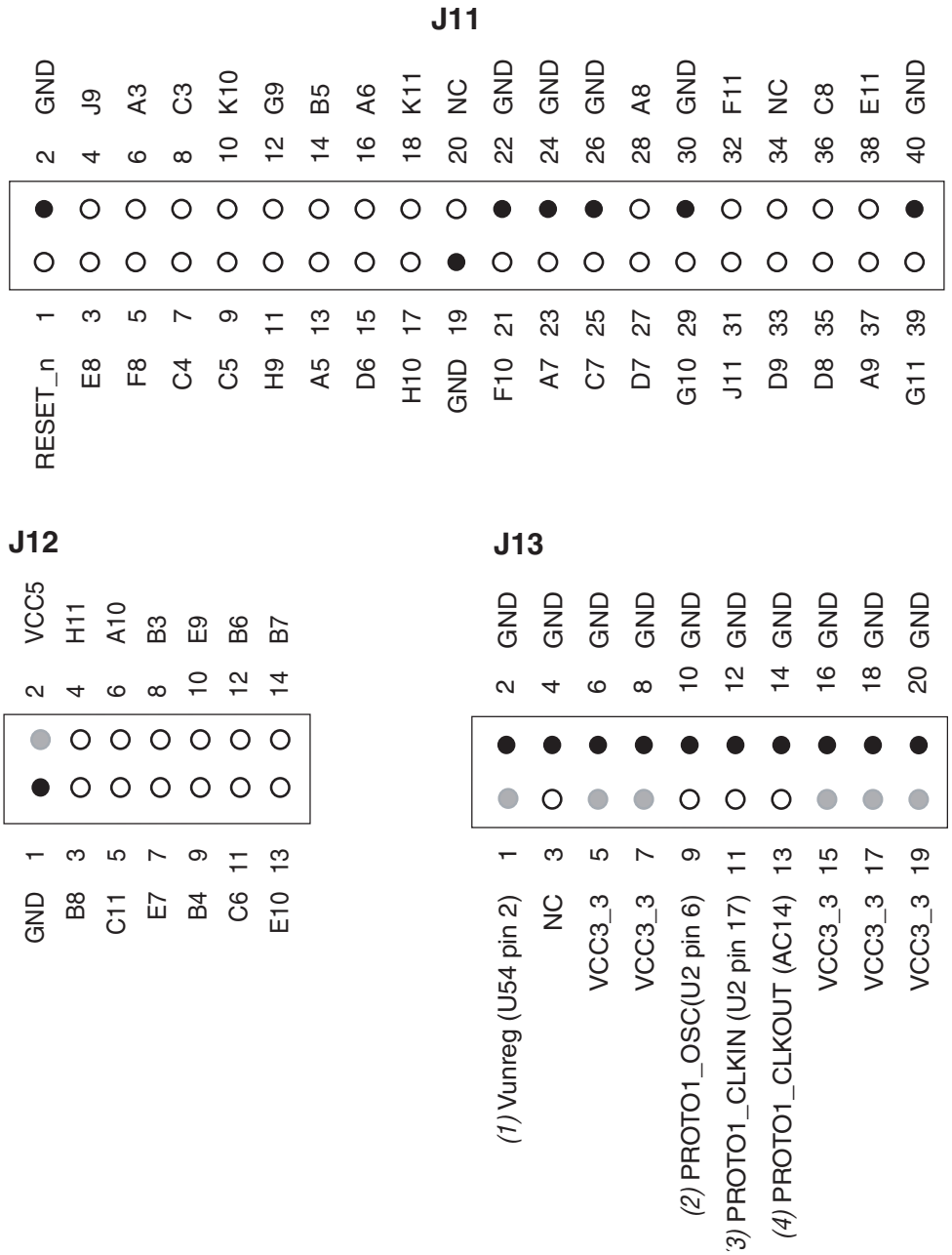


Figure 2–8. PROTO1 Pin Information - J11, J12 & J13



Note to Figure 2–8

(1) Unregulated voltage from DC power supply
(2) Clk from board oscillator
(3) Clk from FPGA via buffer
(4) Clk output from protocard to FPGA

Figure 2–9, and Figure 2–10 show connections from the PROTO2 expansion headers to the Stratix II device. Unless otherwise noted, the labels indicate Stratix II device pin numbers.

Figure 2–9. PROTO1 Expansion Prototype Connector - J15, J16 & J17

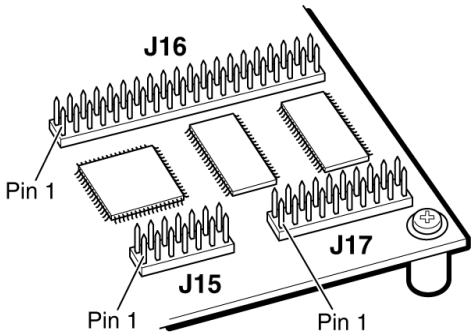
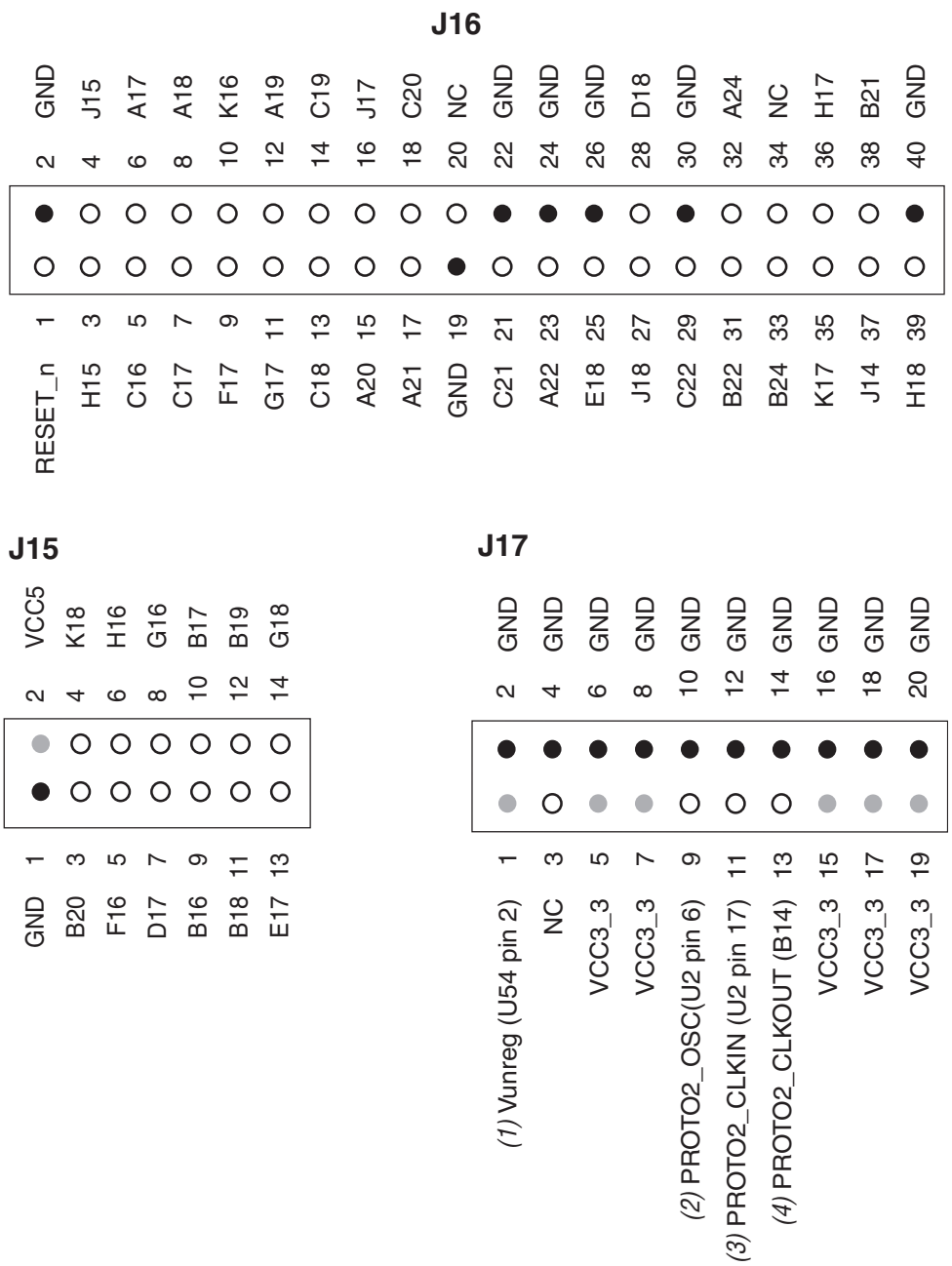


Figure 2–10. 6PROTO2 Pin Information - J15, J16 & J17



Notes to Figure 2–10

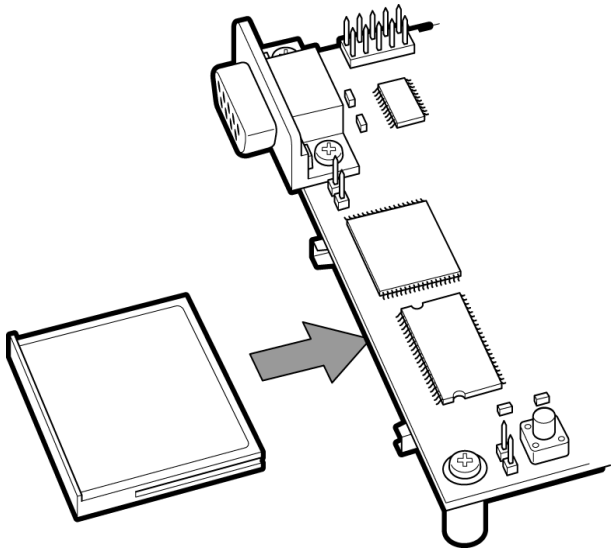
(1) Unregulated voltage from DC power supply
(2) Clk from board oscillator
(3) Clk from FPGA via buffer
(4) Clk output from protocard to FPGA

CompactFlash Connector (CON3)

The CompactFlash connector header (CON3) enables hardware designs to access a CompactFlash card. See Figure 2–11. The following two access modes are supported:

- ATA (hot swappable mode)
- IDE (IDE hard disk mode)

Figure 2–11. CompactFlash Connector



Most pins of CON3 connect to I/O pins on the FPGA. The following pins have special connections:

- Pin 13 of CON3 (VCC) is driven by a power MOSFET that is controlled by an FPGA I/O pin. This allows the FPGA to control power to the CompactFlash card for the IDE connection mode.
- Pin 26 of CON3 (-CD1) is pulled up to 5V through a 10 Kohm resistor. This signal is used to detect the presence of a CompactFlash card; when the card is not present, the signal is pulled high through the pull-up resistor.
- Pin 41 of CON3 (RESET) is pulled up to 5V through a 10 Kohm resistor, and is controlled by the EPM7128AE configuration controller. The FPGA can cause the configuration controller to assert RESET, but the FPGA does not drive this signal directly.

The CompactFlash connector shares several Stratix II I/O pins with expansion prototype connector PROTO1. See "Expansion Prototype Connectors (PROTO1 & PROTO2)" on page 2–15 for details on PROTO1.

Table 2–6 on page 2–21 provides CompactFlash pin out details.

Table 2–6. CompactFlash (CON3) Pin Table (Part 1 of 2)

Pin on CompactFlash (CON3)	CompactFlash Function (U60)	Connects to (1)
1	GND	GND
2	D03	H9
3	D04	C5
4	D05	C4
5	D06	F8
6	D07	E8
7	-CE	A9
8	A10	H11
9	-OE	W16
10	A09	A10
11	A08	E7
12	A07	B3
13	VCC	Y17(2)
14	A06	B4
15	A05	E9
16	A04	C6
17	A03	B6
18	A02	C8
19	A01	D9
20	A00	D8
21	D00	H10
22	D01	D6
23	D02	A5
24	WP	F11
25	-CD2	GND(3)
26	-CD1	AB16
27	D11	K10
28	D12	G9
29	D13	B5
30	D14	A6
31	D15	K11

Table 2–6. CompactFlash (CON3) Pin Table (Part 2 of 2)

Pin on CompactFlash (CON3)	CompactFlash Function (U60)	Connects to (1)
32	-CE2	Y16
33	-VS1	GND(3)
34	-OIORD	C7
35	-IOWR	A7
36	-WE	E10
37	RDY/BSY	J11
38	VCC	Y17(2)
39	-CSEL	GND(3)
40	-VS2	no connect(3)
41	RESET	(4)
42	-WAIT	D7
43	-INPACK	B7
44	-REG	B8
45	BVD2	G11
46	BVD1	C11
47	D081	J9
48	D091	A3
49	D101	C3
50	GND	GND(3)

Note to Table 2–6

(1) All pin numbers represent I/O pins on the FPGA, unless otherwise noted.
(2) This FPGA I/O pin controls a power MOSFET that supplies 5V VCC to CON3.
(3) This pin does not connect to the FPGA directly.
(4) RESET is driven by the EPM7128AE configuration controller device.

For more information on the CompactFlash connector (CON3), refer to **www.compactflash.org** and **www.molex.com**.

Mictor Connector (J25)

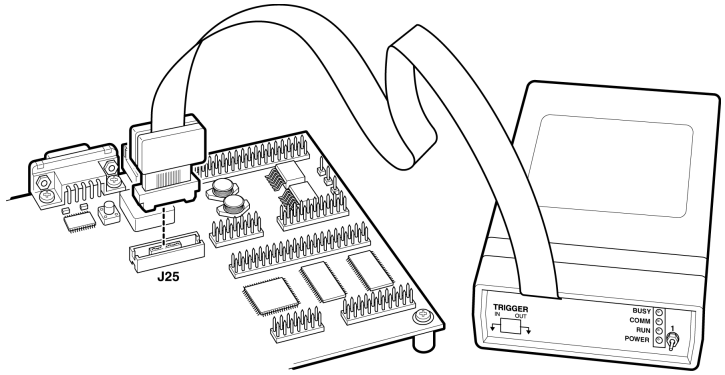
The Mictor connector (J25) can be used to transmit up to 27 high-speed I/O signals with very low noise via a shielded Mictor cable. J25 is used as a debug port. Twenty five of the Mictor connector signals are used as data, and two signals are used as clock input and clock output.

Most pins on J25 connect to I/O pins on the Stratix II device (U60). For systems that do not use the Mictor connector for debugging the Nios II processor, any on-chip signals can be routed to I/O pins and probed at J25 via a Mictor cable. External scopes and logic analyzers can connect to J25 and analyze a large number of signals simultaneously.

For details on Nios II debugging products that use the Mictor connector, refer to **www.altera.com**.

Figure 2–12 shows an example of an in-target system analyzer ISA-Nios/T (sold separately) by First Silicon Solutions (FS2) Inc. connected to the Mictor connector. For details see **www.fs2.com**.

Figure 2–12. An ISA-Nios/T Connecting to the Mictor Connector (J25)



Five of the signals connect to both the JTAG pins on the Stratix II device (U60), and the Stratix II device's JTAG connector (J24). The JTAG signals have special usage requirements. You cannot use J25 and J24 at the same time.

Figure 2–13 below shows connections from the Mictor connector to the Stratix II device. Figure 2–14 shows the pin out for J25. Unless otherwise noted, labels indicate Stratix II device pin numbers.

Figure 2–13. Mictor Connector Signaling

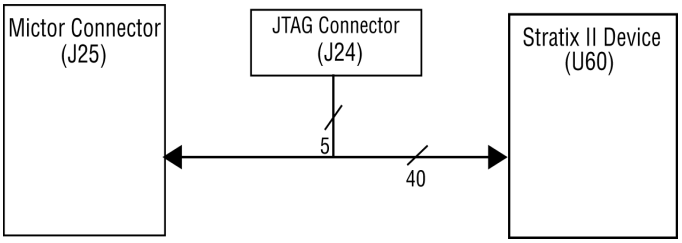
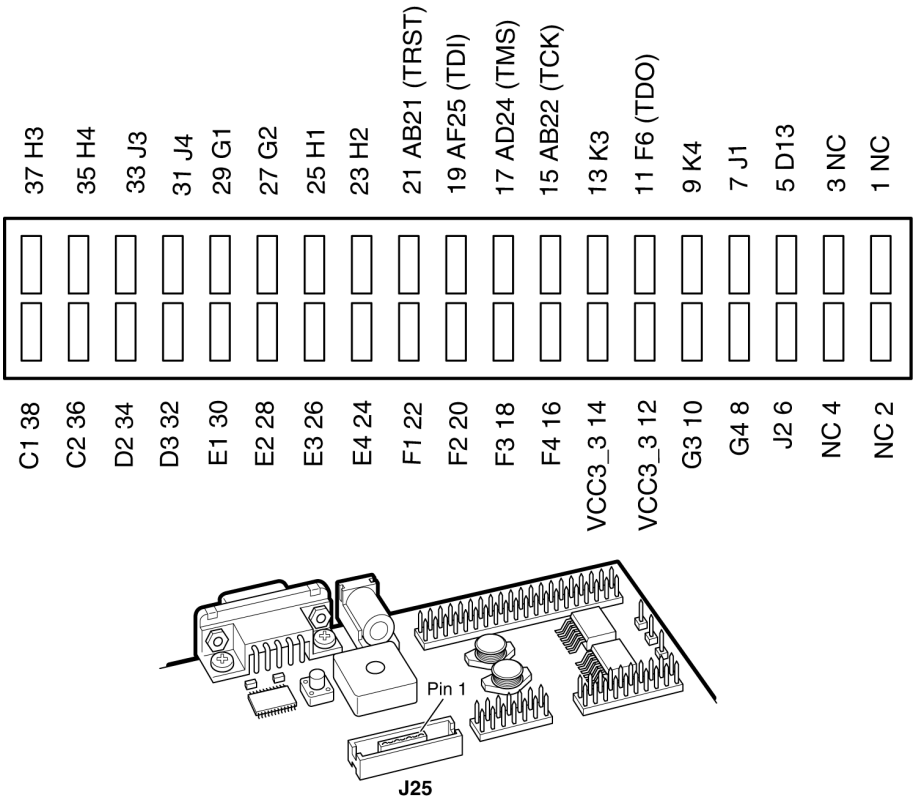


Figure 2–14. Debug Mictor Connector - J25



Configuration Controller Device (U3)

The configuration controller (U3), is an Altera MAX® 7000 EPM7128AE device. It comes preprogrammed with logic for managing board reset conditions and configuring the Stratix II device from data stored in flash memory.

Reset Distribution

The EPM7128AE device takes a power-on reset pulse from the Linear Technologies 1326 power-sense/reset-generator chip and distributes it (through internal logic) to other reset pins on the board, including the:

- LAN91C111 (Ethernet MAC/PHY) reset
- Flash memory reset
- CompactFlash reset
- Reset signals delivered to the expansion prototype connectors (PROTO1 & PROTO2)

Starting Configuration

There are four methods to start a configuration sequence. The four methods are the following:

1. Board power-on.
2. Pressing the Reset, Config button (SW10).
3. Asserting (driving 0 volts on) the EPM7128AE's `reconfigreq_n` input pin (from a Stratix II design).
4. Pressing the Factory Config button (SW9).

Stratix II Configuration

At power-up or reset, the configuration controller reads data out of the flash memory, and presents the necessary control signals to configure the Stratix II device. The Stratix II device is configured using fast passive parallel mode.

For detailed information about the Altera EPM7128AE device, refer to the MAX 7000 family literature at **www.altera.com/literature/lit-m7k.html**.

FPGA configuration data files are generated by the Quartus II software. You can write new configuration data to the board's flash memory using the Nios II integrated development environment (IDE).

For details on programming configuration data to flash memory, see the *Nios II Flash Programmer User Guide*, or refer to the Nios II IDE online help.

Factory & User Configurations

The configuration controller can manage two separate Stratix II device configurations stored in flash memory. These two configurations are referred to as the factory configuration and the user configuration. A Nios II reference design is factory-programmed into the factory configuration region of the flash memory.

The Configuration Process

Upon reset or when the Reset, Config button (SW10) is pressed, the configuration controller will attempt to download the user configuration data to the FPGA. If this process fails (because the user configuration is either invalid or not present), the configuration controller will then download the factory configuration to the FPGA.

When SW9 (Factory Config) is pressed, the configuration controller will ignore the user configuration and always configure the FPGA with the factory configuration. This switch allows you to "escape" from the situation where a valid-but-nonfunctional user configuration is present in flash memory.

The configuration controller reads data from flash memory, passes it to the FPGA, and applies appropriate control signals to configure the FPGA. When FPGA configuration completes successfully, the configuration controller electrically disconnects itself from the flash memory lines, and enters an idle state.

Flash Memory Partitions

The configuration controller expects user and factory configuration data to be stored at fixed locations (offsets) in flash memory. In addition, the factory-programmed reference design expects Nios II software and data to exist at certain locations in flash memory. Table 2–7 shows the expected flash memory partitioning.

Table 2–7. Flash Memory Partitions

Offset	Usage	Factory-Programmed Content
0x00000000 - 0x000FFFFF	User Application Space (8 MB)	Web Server Software
0x00100000 - 0x001FFFFF		Web Pages
0x00200000 - 0x007FFFFF		
0x00800000 - 0x00BFFFFF	User Configuration (4MB)	
0x00C00000 - 0x00FEFFFF	Factory Configuration (4032 KB)	Nios II Processor Reference Design
0x00FF0000 - 0x00FFFFFF	Persistent Data (64 KB)	Network Settings for Web Server

Note that this partitioning scheme is merely a convention used by the configuration controller and the factory-programmed reference design. Custom FPGA designs can use the flash memory space in any way necessary.

Altera recommends that you do not overwrite the factory-programmed flash memory contents. Without a valid factory configuration, the configuration controller may not be able to successfully configure the FPGA. If you alter the factory configuration, you can restore the board to its factory-programmed state. See Appendix B, Restoring the Factory Configuration.

User Application Space

The lower 8 MB of flash memory is the user application space. This is free space for user designs to store code and data for Nios II programs. The lower 2 MB of the user application space is factory-programmed with code and data for a web server reference design. The Nios II IDE allows you to compile Nios II programs and program them into the user application space.

User Configuration

The user configuration partition is 4 MB, starting at offset 0x00800000. This section contains the FPGA configuration data for the user configuration. Nios II development tools include documentation on how to create your own user configuration image and program it into flash memory.

Factory Configuration

The factory configuration partition is 4032 KB, starting at offset 0x00C00000. This section contains the FPGA configuration data for the factory configuration. The Nios II processor in the factory configuration is designed to start executing code from offset 0x00000000 in the flash memory. The Nios II development kit includes the source files for the factory-programmed hardware and software reference designs.

Persistent Data

The persistent data partition is 64 KB, starting at offset 0x00FF0000. This partition is for maintaining nonvolatile settings and data, such as the MAC address and IP address for the factory-programmed web server reference design. Persistent data is technically no different than other application data, but it is often convenient to think of certain data as independent from the user hardware or software.

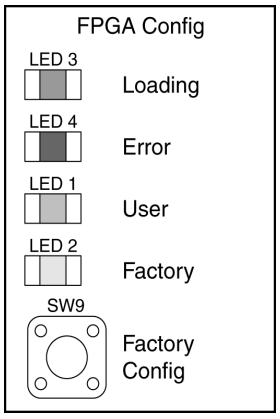
Configuration-Status LEDs

The EPM7128AE device is connected to four status LEDs that show the configuration status of the board at a glance (see Figure 2–15). You can tell which configuration, if any, was loaded into the FPGA at power-on by looking at the LEDs (see Table 2–8 on page 2–29). If a new configuration was downloaded into the Stratix II device via JTAG, then all of the LEDs will turn off.

Table 2–8. Configuration Status LED Indicators

LED	LED Name	Color	Description
LED3	Loading	Green	This LED blinks while the configuration controller is actively transferring data from flash memory into the Stratix II FPGA.
LED4	Error	Red	If the red Error LED is on, then configuration was not transferred from flash memory into the Stratix II device. This can happen if, for example, the flash memory contains neither a valid user or factory configuration.
LED1	User	Green	This LED turns on when the user configuration is being transferred from flash memory and stays illuminated when the user configuration data is successfully loaded into the Stratix II device.
LED2	Factory	Amber	This LED turns on when the factory configuration is being transferred from flash memory and stays illuminated if the factory configuration was successfully loaded into the Stratix II device.

Figure 2–15. LED1 – LED4



Configuration & Reset Buttons

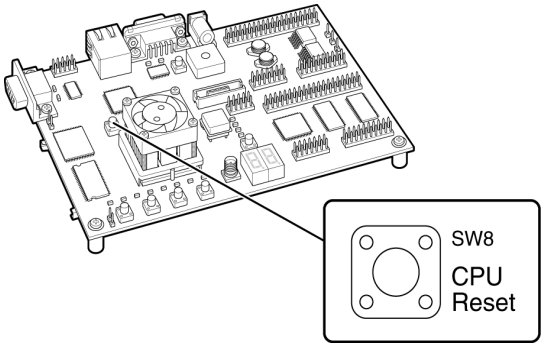
The Nios development board uses dedicated switches SW8, SW9 and SW10 for the following fixed functions:

SW8 – CPU Reset

When SW8 is pressed, a logic-0 is driven onto the Stratix II I/O pin AA15 (DEV_CLRn). The result of pressing SW8 depends on how the Stratix II device is currently configured.

The factory-programmed Nios II reference design treats SW8 as a CPU-reset pin (see Figure 2–16). The Nios II reference design will reset and start executing code from its reset address when SW8 is pressed.

Figure 2–16. CPU Reset Button



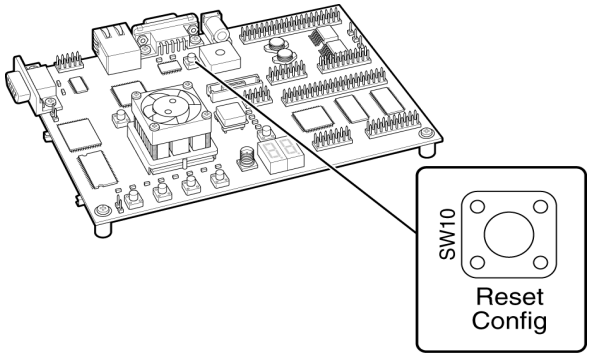
SW9 – Factory Config

Pressing Factory Config (SW9) commands the configuration controller to re-configure the Stratix II device with the factory configuration.

SW10 – Reset, Config

Reset, Config (SW10) is the power-on reset button (see Figure 2–17). When SW10 is pressed, a logic 0 is driven to the power-on reset controller (U18). See "Power-Supply Circuitry" on page 2–35 for more details. After SW10 is pressed, the configuration controller will load the Stratix II device from flash memory.

Figure 2–17. Reset, Config Button



JTAG Connectors (J24 & J5)

The Nios development board, has two 10-pin JTAG headers (J24 and J5) compatible with Altera download cables, such as the USB-Blaster™. Each JTAG header connects to one Altera device and forms a single-device JTAG chain. J24 connects to the Stratix II device (U60), and J5 connects to the EPM7128AE device (U3).

JTAG Connector to Stratix II Device (J24)

J24 connects to the JTAG pins (TCK, TDI, TDO, TMS, TRST) of the Stratix II device (U60) as shown in Figure 2–18. Altera Quartus II software can directly configure the Stratix II device with a new hardware image via an Altera download cable as shown in Figure 2–19. In addition, the Nios II IDE can access the Nios II processor JTAG debug module via a download cable connected to the J24 JTAG connector.

Figure 2–18. JTAG Connector (J24) to Stratix II Device

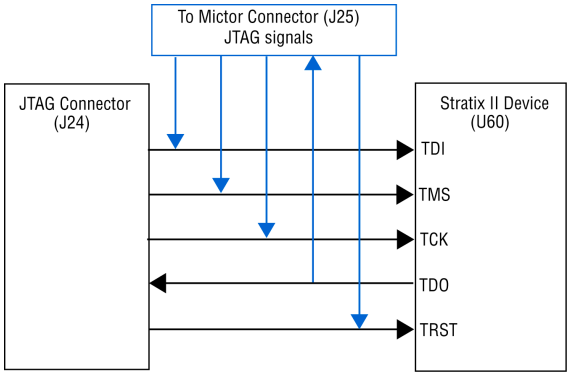
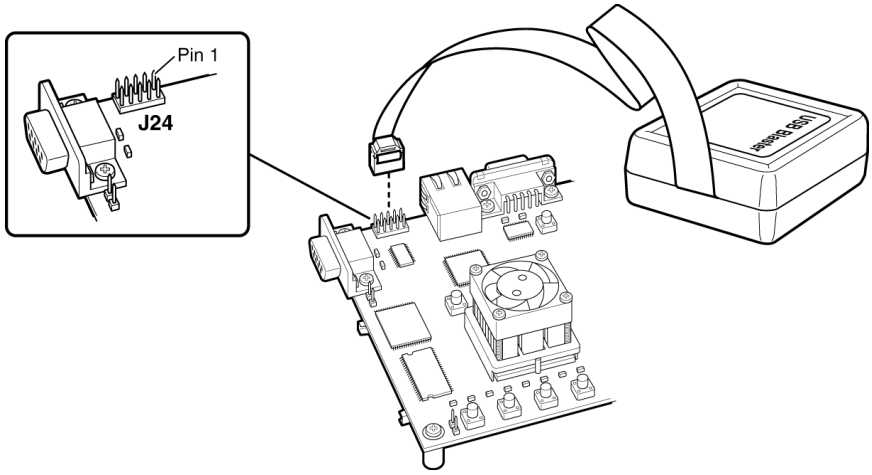


Figure 2–19. USB Blaster Connected to Stratix II JTAG Connector



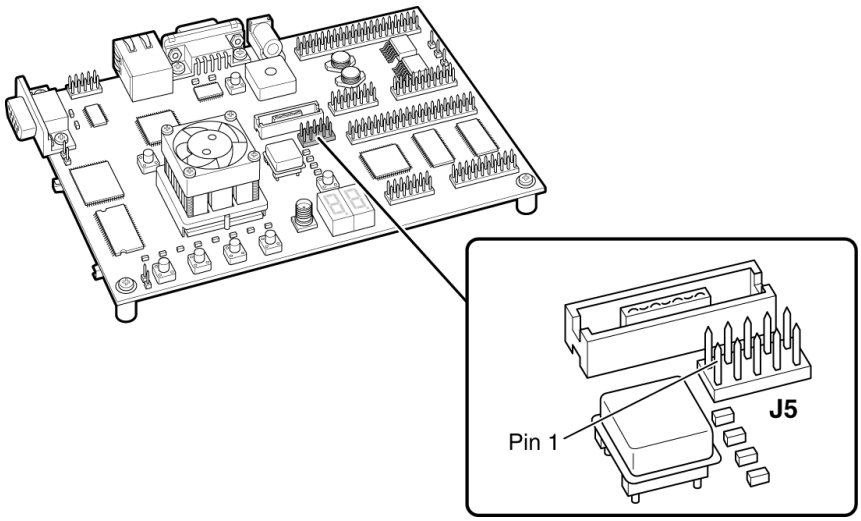
The Stratix II device's JTAG pins can also be accessed via the Mictor connector (J25). The pins of J24 are connected directly to pins on J25, and care must be taken so that signal contention does not occur between the two connectors.

JTAG Connector to EPM7128AE Device (J5)

J5 connects to the JTAG pins (TCK, TDI, TDO, TMS, TRST) of the EPM7128AE device (U3). Altera Quartus II software can perform in-system programming (ISP) to reprogram the EPM7128AE device (U3) with a new hardware image via an Altera download cable.

Note that the orientation of J5 is rotated 180° compared to J24.

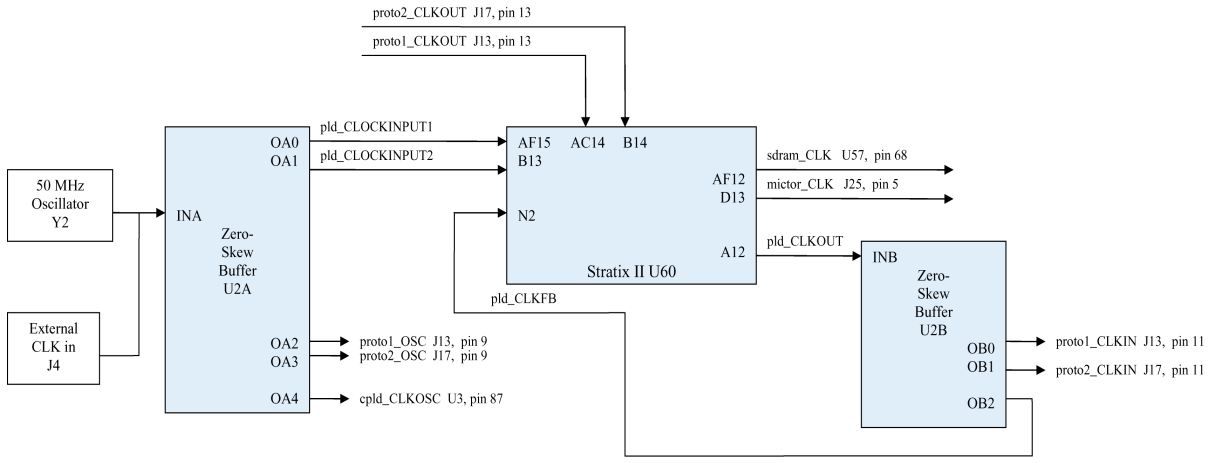
Figure 2–20. JTAG Connector (J5) to MAX Device



Clock Circuitry

The Nios development board includes a 50 MHz free-running oscillator (Y2) and a zero-skew, point-to-point clock distribution network that drives the Stratix II FPGA (U60), the EPM7128AE configuration controller device (U3), and pins on the PROTO1 & PROTO2 connectors. The zero-skew buffer (U2) distributes both the free-running 50 MHz clock and a clock output from one of the FPGA's internal PLLs. See Figure 2–21.

Figure 2–21. Clock Circuitry



Note to Figure 2–21:

(1) An external clock can be enabled by stuffing location R15 with a 49.9 ohm 0603 resistor and stuffing location R13 with a 330 ohm 0603 resistor.

The Stratix II FPGA receives clock input from buffer U2, and from the PROTO1 and PROTO2 connectors, as follows:

- The buffer U2 drives the Stratix II pins AF15 (CLK4p) and B13 (CLK12p).
- The proto1_CLKOUT net (J13, pin 13) drives the Stratix II pin AC14 (CLK5p).
- The proto2_CLKOUT net (J17, pin 13) drives the Stratix II pin B14 (CLK3p).

The FPGA can synthesize new clock signals internally using on-chip PLLs, and drive the clocks to various components on the board. As shown in Figure 2–21, the clock circuitry allows the Stratix II FPGA to:

- Drive the SDRAM chip (U57) via pin AF12, driven by on-chip PLL6.
- Drive the Mictor connector (J25) clock via pin D13, driven by on-chip PLL5.

- Drive the PROTO1 & PROTO2 connectors via pin A12, driven by on-chip PLL5.
- Feedback to FPGA pin N2 (CLK11p). This clock feedback path is not used by Altera-provided reference designs, but is available to the user if necessary.

The 50 MHz oscillator (Y2) is socketed and can be changed or removed by the user. To drive the clock circuitry using the external clock connector (J4), you must first stuff location R15 with a 49.9 ohm 0603 resistor and stuff location R13 with a 330 ohm 0603 resistor. Note that the configuration controller and other Altera-provided reference designs are designed to work only with the 50 MHz clock. If you change the clock frequency, it is your responsibility to accommodate the new clock everywhere it is used on the development board.

Power-Supply Circuitry

The Nios development board runs from a 17V, unregulated, input power supply. On-board circuitry generates 5V, 3.3V, and 1.2V regulated power levels.

- The input power-supply can be either center-negative or center-positive. A bridge rectifier (D34) presents the appropriate polarity to the voltage regulators.
- The 5V supply is presented on pin 2 of J12 and J15 for use by any device plugged into the PROTO1 & PROTO2 expansion connectors.
- The 3.3V supply is used as the power source for all Stratix II device I/O pins. The 3.3V supply is also available for PROTO1 & PROTO2 daughter cards.
- The 1.2V supply is used only as the power supply for the Stratix II device core (VCCINT) and it is not available on any connector or header.

Appendix A. Shared Bus Table

Description

On the Nios development board, Stratix II edition, the flash memory, SRAM and Ethernet MAC/PHY devices share address and control lines. These shared lines are referred to as the Shared Bus. Using SOPC Builder, designers can interface a Nios II processor system to any device connected to the off-chip Shared Bus. Table A–9 on page A–1 lists all connections between the devices connected to the Shared Bus.

Table A–9. Shared Bus Table (Part 1 of 3)

NET Name	NET Description	PLD (U60)		Flash (U5)		SRAM (U35)		SRAM (U36)		Ethernet (U4)	
		Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
FSE_A0	Shared Address	IO	T2	D15/A-1	51						
FSE_A1		IO	T3	A0	31					A1	78
FSE_A2		IO	U1	A1	26	A0	1	A0	1	A2	79
FSE_A3		IO	U2	A2	25	A1	2	A1	2	A3	80
FSE_A4		IO	V1	A3	24	A2	3	A2	3	A4	81
FSE_A5		IO	V2	A4	23	A3	4	A3	4	A5	82
FSE_A6		IO	W1	A5	22	A4	5	A4	5	A6	83
FSE_A7		IO	W2	A6	21	A5	18	A5	18	A7	84
FSE_A8		IO	Y1	A7	20	A6	19	A6	19	A8	85
FSE_A9		IO	Y2	A8	10	A7	20	A7	20	A9	86
FSE_A10		IO	AA1	A9	9	A8	21	A8	21	A10	87
FSE_A11		IO	AA2	A10	8	A9	22	A9	22	A11	88
FSE_A12		IO	AB1	A11	7	A10	23	A10	23	A12	89
FSE_A13		IO	AB2	A12	6	A11	24	A11	24	A13	90
FSE_A14		IO	W3	A13	5	A12	25	A12	25	A14	91
FSE_A15		IO	W4	A14	4	A13	26	A13	26	A15	92
FSE_A16		IO	Y3	A15	3	A14	27	A14	27		
FSE_A17		IO	Y4	A16	54	A15	42	A15	42		
FSE_A18		IO	AA3	A17	19	A16	43	A16	43		
FSE_A19		IO	AA4	A18	18	A17	44	A17	44		
FSE_A20		IO	AB3	A19	11						
FSE_A21		IO	AB4	A20	12						
FSE_A22		IO	AC2	A21	15						
FSE_A23		IO	AC3	A22	2						
FSE_A24		IO	P5	NC.A23 (1)	1						

Table A–9. Shared Bus Table (Part 2 of 3)

NET Name	NET Description	PLD (U60)		Flash (U5)		SRAM (U35)		SRAM (U36)		Ethernet (U4)	
		Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
FSE_D0	Shared Data	IO	E16	D0	35	D0	7			D0	107
FSE_D1		IO	G15	D1	37	D1	8			D1	106
FSE_D2		IO	E19	D2	39	D2	9			D2	105
FSE_D3		IO	D20	D3	41	D3	10			D3	104
FSE_D4		IO	G19	D4	44	D4	13			D4	102
FSE_D5		IO	D19	D5	46	D5	14			D5	101
FSE_D6		IO	E20	D6	48	D6	15			D6	100
FSE_D7		IO	F20	D7	50	D7	16			D7	99
FSE_D8		IO	T4			D8	29			D8	76
FSE_D9		IO	T5			D9	30			D9	75
FSE_D10		IO	U3			D10	31			D10	74
FSE_D11		IO	U4			D11	32			D11	73
FSE_D12		IO	T8			D12	35			D12	71
FSE_D13		IO	T9			D13	36			D13	70
FSE_D14		IO	V3			D14	37			D14	69
FSE_D15		IO	V4			D15	38			D15	68
FSE_D16		IO	U5					D0	7	D16	66
FSE_D17		IO	U6					D1	8	D17	65
FSE_D18		IO	T6					D2	9	D18	64
FSE_D19		IO	T7					D3	10	D19	63
FSE_D20		IO	U7					D4	13	D20	61
FSE_D21		IO	U8					D5	14	D21	60
FSE_D22		IO	V5					D6	15	D22	59
FSE_D23		IO	V6					D7	16	D23	58
FSE_D24		IO	V7					D8	29	D24	56
FSE_D25		IO	V8					D9	30	D25	55
FSE_D26		IO	W5					D10	31	D26	54
FSE_D27		IO	W6					D11	32	D27	53
FSE_D28		IO	W7					D12	35	D28	51
FSE_D29		IO	W8					D13	36	D29	50
FSE_D30		IO	AA5					D14	37	D30	49
FSE_D31		IO	AA6					D15	38	D31	48

Table A–9. Shared Bus Table (Part 3 of 3)

NET Name	NET Description	PLD (U60)		Flash (U5)		SRAM (U35)		SRAM (U36)		Ethernet (U4)	
		Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
FLASH_CS_n	Chip Select	IO	AE4	CE_n	32						
FLASH_OE-N	Read Enable	IO	AB9	OE_n	34						
FLASH_RW-N	Write Enable	IO	AD6	WE_n	13						
FLASH_WP_N	Write Protect/ACC	IO	Y6	WE_n.ACC	16						
FLASH _BYTE_N	Byte Enable	IO	AB11	BYTE_n	53						
FLASH_RESET_N	Reset			Reset_n	14						
FLASH_RY-BY_N	Ready/Busy	IO	AE6	RY/BY_n	17						
SRAM_BE_N0	Byte Enable 0	IO	K20			BE0#	39				
SRAM_BE_N1	Byte Enable 1	IO	K19			BE1#	40				
SRAM_BE_N2	Byte Enable 2	IO	K22					BE2#	39		
SRAM_BE_N3	Byte Enable 3	IO	K21					BE3#	40		
SRAM_CS_N	Chip Select	IO	J19			CS_n	6	CS_n	6		
SRAM_OE_N	Read Enable	IO	J22			OE_n	41	OE_n	41		
SRAM_WE_N	Write Enable	IO	J21			WE_n	17	WE_n	17		
ENET_ADS_N	Address Strobe	IO	AD2							ADS#	37
ENET_AEN	Address Enable	IO	AF10							AEN	41
ENET_BE_N0	Byte Enable 0	IO	AD8							BE0#	94
ENET_BE_N1	Byte Enable 1	IO	AF9							BE1#	95
ENET_BE_N2	Byte Enable 2	IO	Y11							BE2#	96
ENET_BE_N3	Byte Enable 3	IO	W12							BE3#	97
ENET_CYCLE_N	Bus Cycle	IO	AC9							CYCLE#	35
ENET_DATACS_N	Data Chip Select	IO	Y12							DATACS #	34
ENET_INTRQ0	Interrupt	IO	AD11							INTRO	29
ENET_IOCHRDY	IO Char Ready	IO	AD1							ARDY	38
ENET_IOR_N	Read	IO	AC10							RD#	31
ENET_IOW_N	Write	IO	AE11							WR#	32
ENET_LCLK	Local Bus Clock	IO	W11							LCLK	42
ENET_LDEV_N	Local Device	IO	Y7							LDEV#	45
ENET_RDYRTN_N	Ready Return	IO	V12							RDYRTN #	46
ENET_W_R_N	Write/Read	IO	AC8							W/R#	36

Note to Table A–9:

(1) This pin is NC for AM29LV128M but is provided for compatible devices that have the active pin A23.

Appendix B. Restoring the Factory Configuration

Introduction

To restore the factory configuration, you must reprogram the flash memory on the board, and you must reprogram the EPM7128AE configuration controller device.

The files required for this operation are included in the Nios II development kit's *<Nios II kit path>*/**examples/factory_recovery** directory.

Reprogramming the Flash Memory

To reprogram the flash memory on the development board, perform the following steps:

1. Open a Nios II SDK Shell by choosing **Windows Start > Programs > Altera > Nios II Development Kit** *<installed version>* **> Nios II SDK Shell**.
2. From the **examples** directory, change to the **factory_recovery** directory for your development kit.

   ```
   cd factory_recovery/niosII_stratixII_2s60_ES
   ```

3. Run the flash-restoration script:

   ```
   ./restore_my_flash
   ```

Follow the script's instructions.

Reprogramming the EPM7128AE Configuration Controller Device

If the configuration controller design was modified, you must also reprogram the EMP7128AE device (U3). The EPM7128AE configuration controller device also must be reprogrammed.

1. Move the programming cable from J24 to J5, labeled "For U3".

   ☞ The orientation of J5 is opposite that of J24. When properly connected to J5, the programming cable lies naturally across the FPGA Config LEDs and the dual seven-segment display.

2. Launch the Quartus II software, and open the **Programmer** window (Tools menu).

3. Click **Add File** and select the following programming file:

   *<Nios II kit path>***/examples/factory_recovery/niosII_stratixII_2s60_ES/config_controller.pof**.

4. In the **Programmer**, check the **Program/Configure** box, and click **Start** to reprogram the EPM7128AE device.

5. Press the Factory Config button to perform a power-on reset and reconfigure the Stratix II device from flash memory. You should see the Factory LED turned on and activity on LEDs D0 through D7.

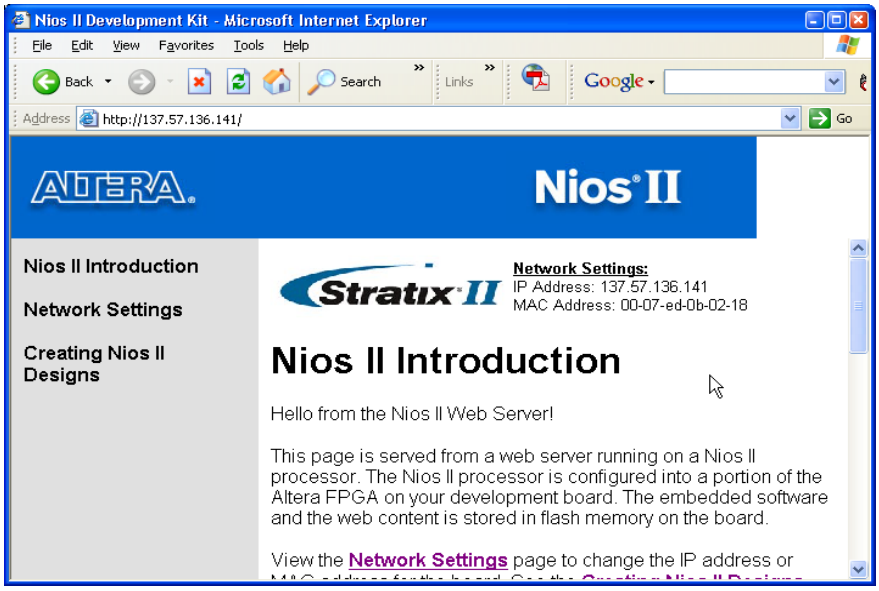
Your board is now reconfigured to the default factory condition.

Appendix C. Connecting to the Board via Ethernet

Introduction

The Nios development board is factory-programmed with a reference design that implements a web server, among other functions as shown in Figure C–1. The sections below describe how to connect a host computer to the board's Ethernet port, assign an IP address to the board, and browse to the web server from the host computer.

Figure C–1. Web Server Reference Design



Connecting the Ethernet Cable

The Nios II development kit includes an Ethernet (RJ45) cable and a male/female RJ45 crossover adapter. Before you connect these components, you must decide how you want to use the network features of your board. Select one of the two following connection methods:

1. *LAN Connection* — To use your Nios development board on a LAN (for example, connecting to an Ethernet hub) do the following:

    a. Connect one end of the RJ45 cable to the Ethernet connector on the development board (RJ1).

b. Connect the other end to your LAN connection (hub, router, wall plug, etc.).

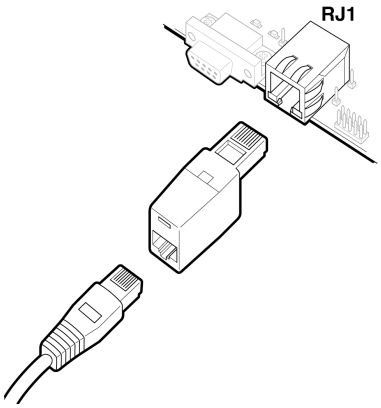
2. *Point-to-Point Connection* — To use your Nios development board connected directly to a host computer point-to-point (not on a LAN), do the following:

   a. Connect one end of your RJ45 cable to the female socket in the crossover adapter.

   b. Insert the male end of the crossover adapter into RJ1 on the Nios development board.

   c. Connect the other end of the RJ45 connector directly to the network (Ethernet) port on your host computer (see Figure C–2 on page C–2).

Figure C–2. Point-to-Point Connection



Connecting the LCD Screen

Your Nios II development kit was delivered with a two-line x 16-character LCD text screen. The web-server software displays useful status and progress messages on this display. If you wish to use the network features of the board, connect the LCD screen to the Expansion Prototype Connector (J12). See the *Nios II Development Kit, Getting Started User Guide* for details.

Obtaining an IP Address

In order to function on a network (either LAN or point-to-point), your board must have an IP address. This section describes the methods to assign an IP address to your board.

LAN Connection

If you have connected your board to a LAN, the board will either obtain a dynamic IP address using DHCP, or a static IP address stored in flash memory. If you do not know whether or not your LAN supports DHCP, it is easiest to try DHCP first.

DHCP

Upon reset, the web server will attempt to acquire an IP address via the DHCP protocol. The board will continue to attempt DHCP self-configuration for two minutes. You can determine if DHCP has succeeded, or if it is still in progress, by reading status messages on the LCD screen. If your LAN does not support DHCP then DHCP configuration will ultimately fail, and the web server will default to a static IP address.

If DHCP succeeds, the board will display a success message and the IP address on the LCD screen. The web server is now ready to display web pages. See "Browsing to Your Board" on page C–5 to continue.

Static IP Address

If the DHCP process fails, the board will use a static IP address stored in flash memory. You need to obtain a safe IP address in your LAN's subnet from your system administrator. Once you know a safe IP address, you can assign it to your board using the steps below.

These steps send IP configuration data to the board via an Altera JTAG download cable, such as the USB-Blaster cable.

1. Install the Nios II development tools, connect the JTAG download cable, and apply power to the board, as described in the *Nios II Development Kit, Getting Started User Guide*.

2. Choose **Start > Programs > Altera > Nios II Development Kit > Nios II SDK Shell** to open the Nios II SDK Shell. A shell window appears with a command prompt.

3. Press the SW9 button labeled Factory Config on the board.

4. At the Nios II SDK Shell command prompt, type:

```
nios2-terminal<Enter>
```

This command opens a terminal connection via the JTAG download cable to a monitor program running on the board. The monitor program displays status messages and text instructions that tell you how to set the IP address for your board.

5. Press the `!` key to abort the DHCP process and display a prompt. If you don't abort the DHCP process, it will fail after two minutes, and eventually a prompt will appear.

The monitor's prompt is the + character. You can enter `h<Enter>` at the prompt for a complete list of supported commands.

6. At the prompt, type `xip:<`*safe IP address*`><Enter>`

   The `xip` command saves the IP address in flash memory. In general, you will only need to assign an IP address to your board once. However, you may change it at any time by issuing another `xip` command. You can also use the commands `xsubnet` and `xgateway` to assign subnet and gateway addresses, but setting these addresses is not usually necessary.

7. Type `xdhcp:off<Enter>` to disable the board from attempting to obtain the IP address using DHCP in the future. (You can re-enable DHCP later, using the `xdhcp:on` command.)

8. Type CTRL+C to terminate the JTAG terminal session and disconnect from the monitor program, then close the Nios II SDK Shell.

9. Press the SW8 button labeled *CPU Reset* to reboot the Nios II processor and start the web server using the new IP address. The LCD screen will display the static IP address assigned to the board, along with other status messages.

The web server is now ready to display pages using the IP address you assigned. See "Browsing to Your Board" on page C–5 to continue.

Point–to–Point Connections

All boards are factory programmed with a default IP address of 10.0.0.51 stored in flash memory. The 10.0.0.x subnet is conventionally reserved for development, test, and prototyping. If DHCP fails or is aborted, the board will use this static IP address. The LCD screen displays status messages to indicate when the web server starts running using the default IP address.

Your host computer and the development board are the only two devices connected to this simple point-to-point network. For most host operating systems, it is necessary to assign your host computer an IP address on the same subnet as the board. For example, the address 10.0.0.1 will work fine. Any address in the 10.0.0.x subnet will work, and there is no possibility of conflicting with another device on the network. After modifying the host computer's IP address, your computer is ready to connect to the web server. See "Browsing to Your Board" on page C–5 to continue.

If you don't have the ability to change the IP address of your host computer, you could change the IP address of the board to match the subnet of the host computer. For example, if your computer's IP address is 1.2.3.4, then you could assign the address 1.2.3.5 to your board. To change the board IP address, follow the steps in "Static IP Address" on page C–3.

Every time you reset the board, the web server will attempt to obtain an IP address via DHCP, which takes two minutes to time out. You can abort the DHCP process, or disable DHCP entirely by using the steps in "Static IP Address" on page C–3.

Browsing to Your Board

Once your board has a valid IP address (obtained from either DHCP self-configuration or from flash memory), you can access the board via a web browser (e.g., Microsoft Internet Explorer). To browse this site, open a web browser and type the IP address of the board (four numbers separated by decimal-points) as a URL directly into the browser's **Address** input field. You can determine your board's IP address by reading the messages displayed on the LCD screen