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ISL6558EVAL1Z - Multi-Phase Power Conversion For Routers and PC Peripherals Up To 100A

Abstract

This application note highlights design considerations for a 150W power supply using Intersil's ISL6558 4-Phase Controller and ISL6612A Synchronous-Rectified Driver. A step-by-step design procedure for a 12V-to-1.5V@100A with 83% efficiency converter based on these two chips is described; all formulae are applicable for a multi-phase interleaved DC-DC buck converter. Thereafter, experimental results with discussion give users a deeper understanding of the performance of the reference design and the advantages of the ISL6558 and ISL6612A. Some operation and modification tips of the evaluation board are included.

Introduction

The changing computer performance landscape has brought about the need for flexible power solutions. Peripheral performance continues to increase as higher speed bus interfaces are made available. Router designs continue to grow in complexity as on-board processors must perform more functions while continuing to increase the speed of data transfer. This translates to higher demands on the DC-DC converters which supply them.

Intersil's Endura™ multi-phase controllers (HIP63xx and ISL65xx) and synchronous-rectified buck MOSFET drivers (ISL66xx) are suitable for the multi-channel interleaved DC-DC buck converter implementation, as shown in Figure 1, and provide superior performance solutions to meet the above market demands.

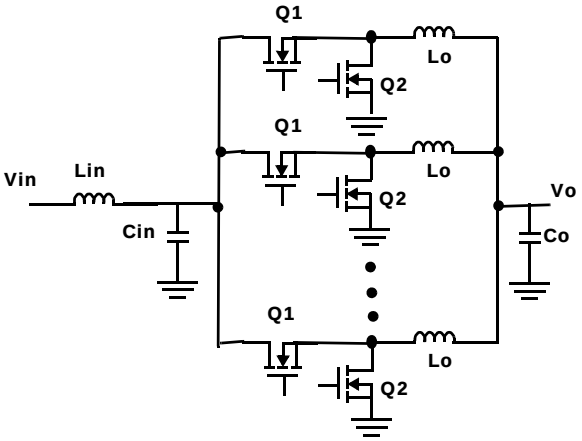


FIGURE 1. MULTI-PHASE INTERLEAVED BUCK CONVERTER

This application note first gives a brief introduction of Intersil's four-phase controller ISL6558 and synchronous-rectified driver ISL6612A. A step-by-step design procedure for a 12V-to-1.5V@100A, 500kHz, and 83% efficiency converter using the interleaved approach follows. It includes all the fundamental formulae to design a multi-phase interleaved DC-DC buck converter. Thereafter, experimental results with discussion give users a deeper understanding of the performance of the reference design and the advantages of both ICs. Term Definition, Reference, Schematics, and Layout are included at the end of this application note.

Intersil's ISL6558 and ISL6612A

The ISL6558 controller coupled with some ISL6612A single-channel driver ICs form the basic building blocks for applications which demand high current and rapid load transient speed.

The ISL6558 regulates the output voltage and balances load currents for two to four synchronous-rectified buck converter channels; its internal structure is shown in Figure 2. The internal 0.8V reference allows output voltage selection down to that level with a 1% system accuracy over-temperature. The current-channel balance loop provides a better thermal balance among all phases. Output voltage droop, or active voltage positioning, is optional. Overvoltage and overcurrent monitors and protection functions of the IC provide a safe environment for microprocessor or other load. The controller is available in a 16 Lead SOIC package and a space economical 5mmx5mm^2 20 Lead QFN package. For more detailed descriptions of the ISL6558 functionality, refer to the device datasheet [1]

The ISL6612A is a driver IC capable of delivering up to 2A of gate-charge current for rapidly switching both MOSFETs in a synchronous-rectified bridge. The ISL6612A accepts a single logic input to control both upper and lower MOSFETs. Its Tri-State® feature, working together with Intersil's Multi-Phase PWM controllers, helps prevent a negative transient on the output voltage when the output is being shut down. This eliminates the Schottky diode that is used in some systems for protecting the microprocessor from reversed-output-voltage damage. Furthermore, adaptive shoot-through protection is provided on both switching edges to provide optimal dead time and minimize conduction losses. Bootstrap circuitry permits greater enhancement of the upper MOSFET. For a more detailed description of the ISL6612A, refer to the device data sheet [2]. In addition, the ISL6614A/ISL6610 dual-channel driver IC provides equivalent functionality with some space savings [3].

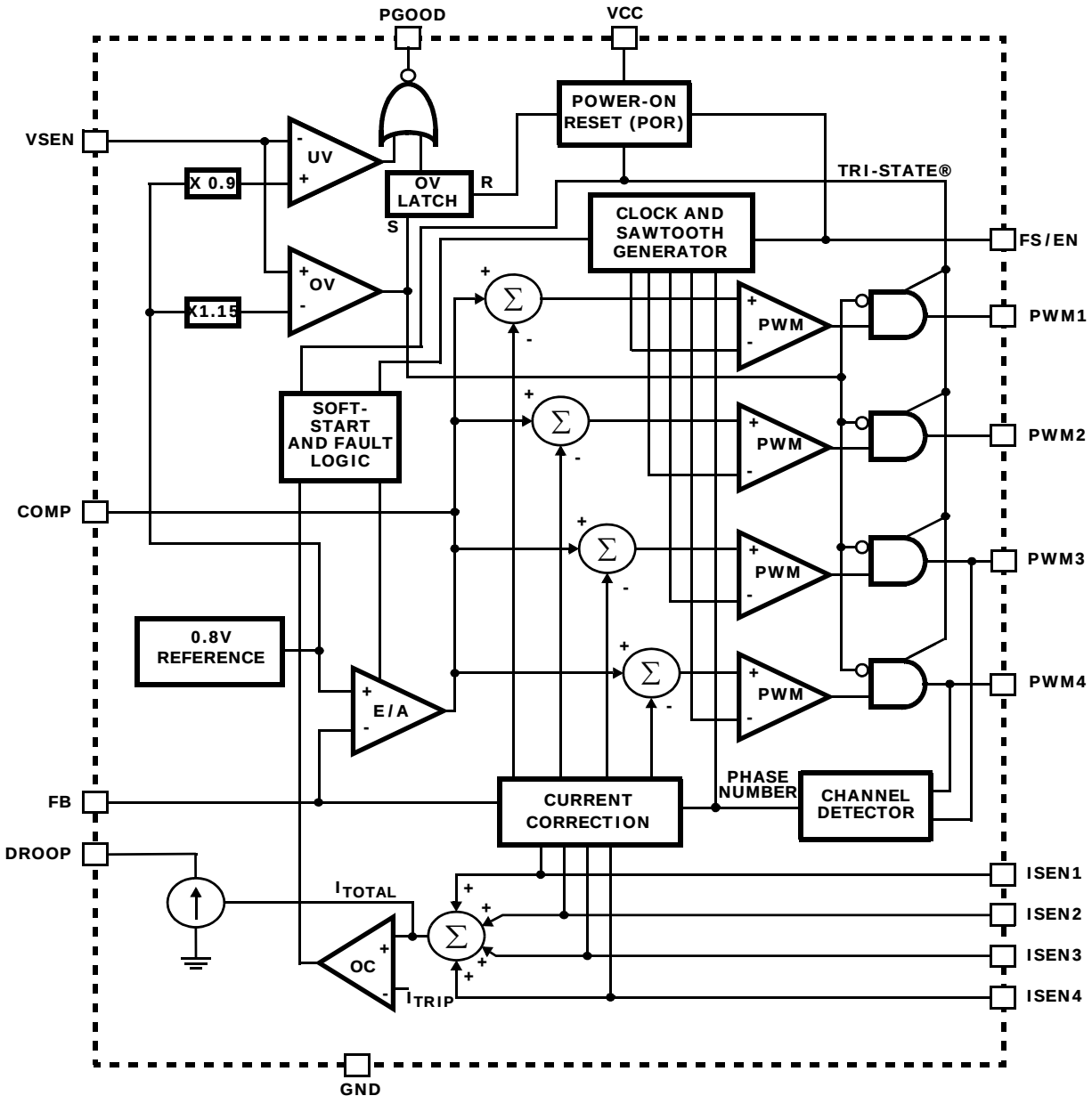


FIGURE 2. ISL6558 INTERNAL STRUCTURE

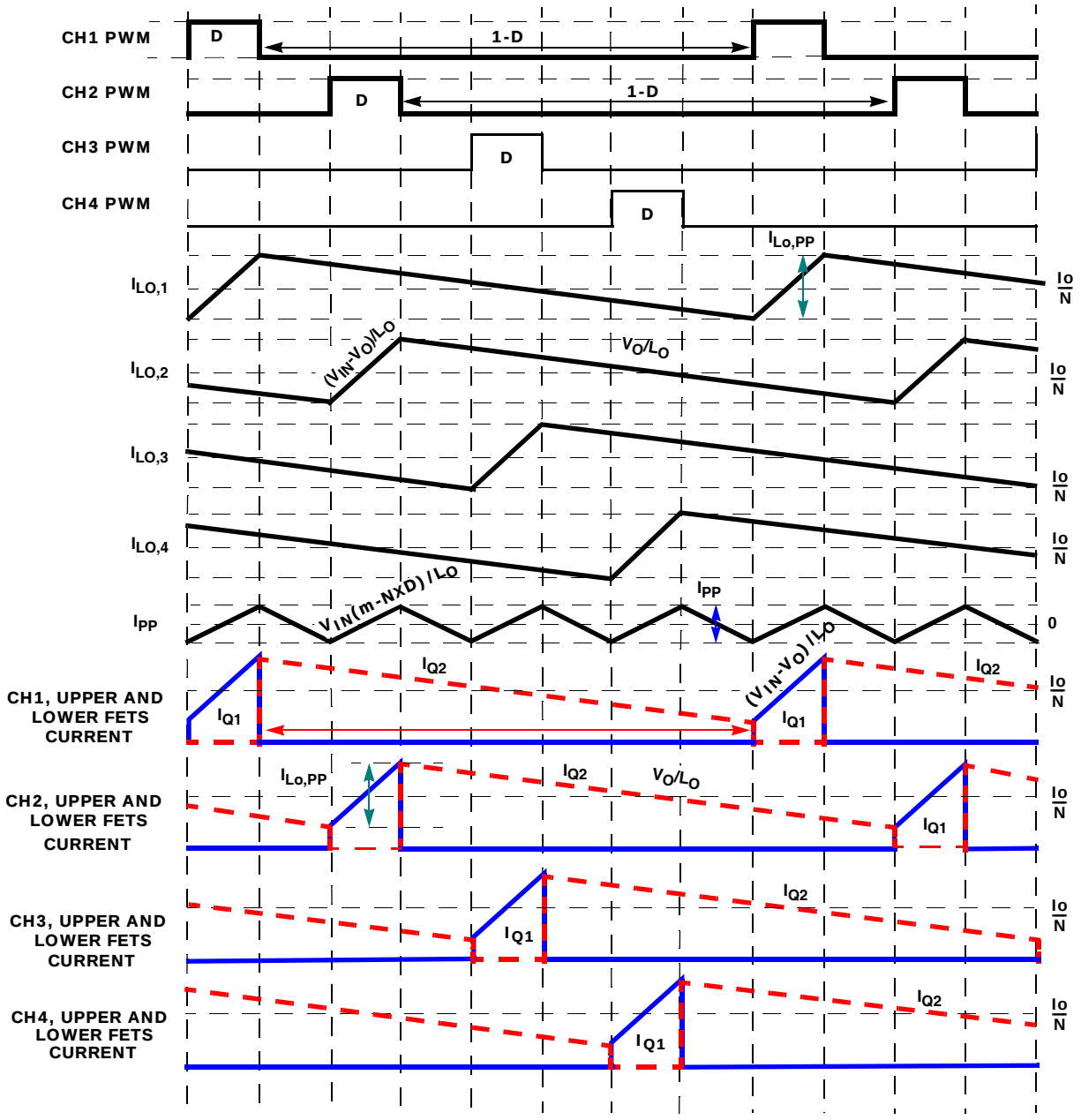
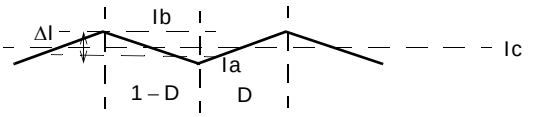


FIGURE 3. FOUR-CHANNEL INTERLEAVED DC-DC BUCK CONVERTER TIMING DIAGRAM

Converter Design

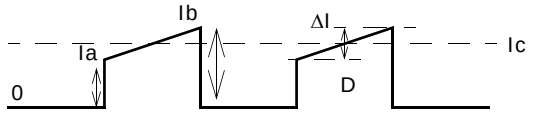
This section summarizes a step-by-step procedure for a 12V-to-1.5V@100A power supply for high current and high transient speed applications. The terms used in all equations are defined at the end of this application note, unless otherwise stated in the text. Some fundamental formulae to calculate RMS values of triangular and trapezoid waveforms and to derive most equations in this application note are defined in the following.

CASE 1



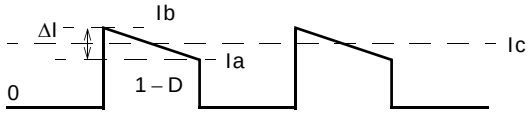
$$Irms1 = \sqrt{Ic^2 + \frac{\Delta I^2}{12}}$$

CASE 2



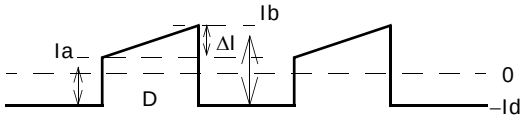
$$Irms2 = \sqrt{\left(Ic^2 + \frac{\Delta I^2}{12}\right) \bullet D}$$

CASE 3



$$Irms3 = \sqrt{\left(Ic^2 + \frac{\Delta I^2}{12}\right) \bullet (1 - D)}$$

CASE 4



$$Irms4 = \sqrt{Ic^2 \bullet (D - D^2) + \frac{\Delta I^2}{12} \bullet D}$$

where

$$Ic = \frac{Ia + Ib}{2}$$

$$Id = Ic \bullet D$$

$$\Delta I = Ib - Ia$$

DETERMINE NUMBER OF PHASES, SWITCHING FREQUENCY, AND DUTY CYCLE

The first step in designing a multi-phase converter is to determine the number of phases. This determination depends heavily on the cost analysis, which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board; whether through-hole components are permitted on either side; and the total board space available for power-supply circuitry. Generally speaking, the most economical solution will be for each phase to handle between 15A and 20A. All surface mount designs will tend toward the lower end of this current range; if through-hole MOSFETs can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 30A per phase, but these designs typically require heat sinks and forced air to cool the MOSFETs. Paralleling MOSFETs in each leg is another way to push per-phase currents even higher, but the power and thermal stresses on each driver should be evaluated carefully. In such a case, a 5V driver such as Intersil's ISL6609 could be considered. See "DRIVER LOSSES CALCULATION" on page 8. In the reference design, all four phases of the ISL6558 are used to deliver 100A of total output current.

There are a number of variables to consider when choosing the switching frequency for a particular application. The size of the converter, the overall losses of magnetics components, the switching losses of power MOSFETs, the desired efficiency, the transient response, and the maximum achievable duty cycle should all be under consideration. It requires an iterative process, monitoring changes of the above parameters, to obtain an optimum switching frequency for a particular application. Equations presented in this paper can be used to develop a MathCAD worksheet that helps obtain a rough idea of the range of optimum frequencies and efficiencies for a particular application. Note that the higher the switching frequency, the higher the loop bandwidth (typically 1/10 to 1/3 of the switching frequency) potentially achieved, resulting in fewer output capacitors to meet the same transient performance.

Equation 1 defines the duty cycle of each channel, and it should be no greater than 75% (maximum duty cycle of the ISL6558) at the minimum operational input line and the maximum fully loaded output. The drops due to the PCB resistances are included in the equation, and they are very significant portions especially for high current applications.

$$D = \frac{Vo + (R_{Q2} + R_{Lo} + R_{Bo}) \bullet \frac{Io}{N}}{V_2 + (R_{Q2} - R_{Q1}) \bullet \frac{Io}{N}} \qquad \text{(EQ. 1)}$$

where

$$V_2 = V_{IN} - (R_{Lin} + R_{Bin}) \bullet I_{IN} - \left(\frac{Io}{N} - I_{IN}\right) \bullet ESR_{IN}$$

$$Vo = Vo_{NL} - V_{DROOP} \bullet \frac{Io}{Io_{max}}$$

$$I_{IN} = \frac{Vo \bullet Io}{\eta \bullet V_{IN}}$$

In Equation 1, Vo_{NL} is the output voltage at no load, V_{IN} is the input voltage, N is the number of active channels, I_{IN} and Io are the input and output currents, respectively. R_{Q1} and R_{Q2} are the $r_{DS(ON)}$'s of upper and lower FETs, respectively. R_{Lin} and R_{Lo} are the equivalent resistances of input and output inductors, respectively. R_{Bin} and R_{Bo} are the input and output PCB resistances (including the connectors resistances), respectively.

OUTPUT FILTER DESIGN

The switching of each channel in a multi-phase converter is timed to be symmetrically out of phase with each of the other channels. In an N-phase converter, each channel switches 1/N cycle after the previous channel and 1/N cycle before the following channel. As a result, the N-phase converter has a combined ripple frequency N times the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of active phases. Increased ripple frequency and lower current ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification. Note that the higher the inductor ripple current, the higher the switching and conduction losses of each-channel's bridge MOSFETs. See "Lower MOSFET Power Calculation" on page 7 and "Upper MOSFET Power Calculation" on page 8.

Equation 2 represents an individual channel's peak-to-peak inductor current. Equation 3 represents the combined ripple current filtered by the output capacitors.

$$I_{Lo,PP} = \frac{V_1 \bullet (1-D)}{Lo \bullet Fsw} \quad \text{(EQ. 2)}$$

where $V_1 = Vo + \frac{Io}{N} \bullet (R_{Q1} + R_{Lo} + R_{Bo})$

$$I_{PP} = \frac{V_1}{Lo \bullet Fsw}\left(\frac{(N \bullet D - m + 1) \bullet (m - N \bullet D)}{N \bullet D}\right) \quad \text{(EQ. 3)}$$

for $m - 1 \le N \bullet D \le m$

$m = ROUNDUP(N \bullet D, 0)$

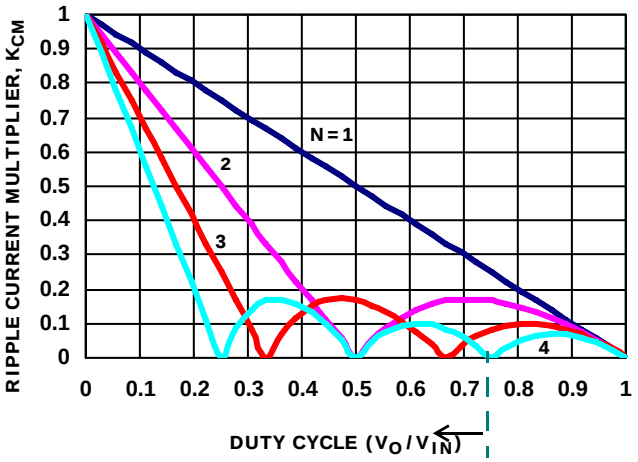


FIGURE 4. RIPPLE CURRENT MUTIPLIER VS. DUTY

In Equation 3, m is the nearest integer that is rounded up from the product of the number of active channels and the individual channel duty cycle, and it represents the maximum number of channels having positive slopes within any time interval. In the reference design, m is one. If the total ripple current (I_{PP}) is normalized to the parameter K_{NORM}, i.e, $I_{Lo,PP}$ at zero duty cycle, then the ripple current multiplier (K_{CM}) can be defined as in Equation 5, which is a function of channel duty cycle, number of active channels, and m.

$$K_{NORM} = \frac{V_1}{Lo \bullet Fsw} \quad \text{(EQ. 4)}$$

$$K_{CM} = \frac{(N \bullet D - m + 1) \bullet (m - N \bullet D)}{N \bullet D} \quad \text{(EQ. 5)}$$

In addition to Equation 3, the total output ripple current can be determined by the product of the ripple current multiplier (K_{CM}) read from Figure 4 and the normalization factor, K_{NORM}.

The RMS and peak currents through the single-channel inductor are defined in Equations 6 and 7, respectively. As a rule of thumb, the total output ripple current should set around 10% to 20% of full load; the required channel inductor value then can be derived from Equation 3, rearranged in Equation 8.

$$I_{Lo,RMS} = \sqrt{\left(\frac{Io}{N}\right)^2 + \frac{I_{Lo,PP}^2}{12}} \quad \text{(EQ. 6)}$$

$$I_{Lo,PEAK} = \frac{Io}{N} + \frac{I_{Lo,PP}}{2} \quad \text{(EQ. 7)}$$

$$Lo = \frac{V_1}{I_{PP} \bullet Fsw}\left(\frac{(N \bullet D - m + 1) \bullet (m - N \bullet D)}{N \bullet D}\right) \quad \text{(EQ. 8)}$$

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each individual channel, as defined in Equation 3, and its RMS value is defined in Equation 9.

$$Io_{RMS} = \sqrt{\frac{I_{PP}^2}{12}} \quad \text{(EQ. 9)}$$

Besides being able to handle the heat that is generated by their equivalent series resistance (ESR), the output capacitors should be designed to meet the output voltage ripple and load transient requirements. For high dI/dt loads, the output voltage ripple will be within the limits when the requirements for the load transient are met.

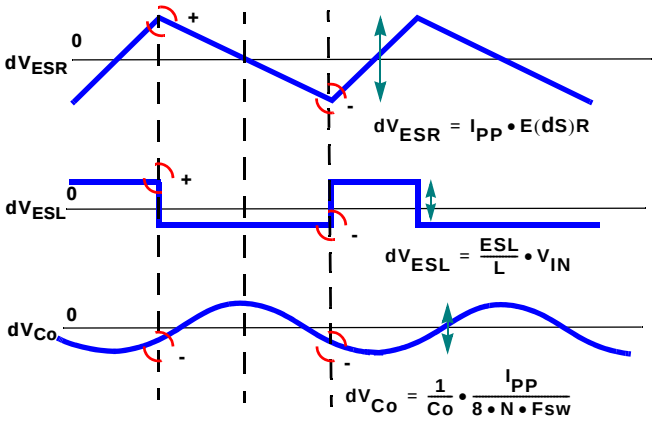


FIGURE 5. OUTPUT VOLTAGE RIPPLE COMPONENTS

The output voltage ripple can be conservatively approximated by Equation 10. The first two terms (dV_{ESR} and dV_{ESL}) contributed by the equivalent series resistance (ESR) and the equivalent series inductance (ESL) of the output capacitors are the dominant ones and are normally accurate enough to estimate the ripple voltage. The last term (dV_{Co}) contributed by the output capacitance (Co) is normally much smaller and can be neglected since the peak of the dV_{Co} happens at the ripple current zero crossing and does not align with the peak of dV_{ESR}, as shown in Figure 5.

$$Vo_{RIPPLE} \approx I_{PP} \bullet ESR + \frac{ESL}{Lo} \bullet V_{IN} + \frac{1}{Co} \bullet \frac{I_{PP}}{8 \bullet N \bullet Fsw} \quad \text{(EQ. 10)}$$

The ESL of a capacitor is not usually listed in databooks. It can be practically approximated with Equation 11:

$$ESL = \frac{1}{Co} \bullet \frac{1}{(2\pi \bullet F_{RES})^2} \quad \text{(EQ. 11)}$$

where F_{RES} is the resonant frequency that produces the lowest impedance of the capacitor. The dV_{ESL} term in Equation 10 is usually filtered out with low ESR ceramic capacitors.

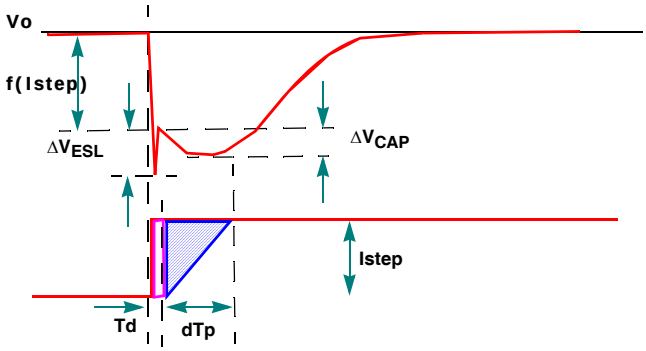


FIGURE 6. TRANSIENT RESPONSE

At the very edge of the transient, the equivalent ESL of all output capacitors induces a spike, as defined in Equation 12 for a given dI/dt, that adds on the top of the existing voltage dip/overshoot due to the effective ESR and capacitance of output capacitors.

$$\Delta V_{ESL} = ESL \bullet \frac{dI}{dt} \quad \text{(EQ. 12)}$$

Thus, the overall load transient can be conservatively approximated with Equation 13, in which the last term can be normally dropped out if the very edge of the transient is the dominant peak, as shown in Figure 6.

$$\Delta V_{TRAN} \approx f(Istep) + \Delta V_{ESL} + \Delta V_{CAP} \quad \text{(EQ. 13)}$$

where

$$f(Istep) = Istep \frac{\sqrt{1 + (2\pi \bullet f_c \bullet Co \bullet ESR)^2}}{2\pi \bullet f_c \bullet Co}$$

$$f(Istep) \approx Istep \bullet ESR \quad \text{for} \quad fc \gg \frac{1}{2\pi \bullet ESR \bullet Co}$$

$$f(Istep) \approx \frac{Istep}{2\pi \bullet f_c \bullet Co} \quad \text{for} \quad fc \ll \frac{1}{2\pi \bullet ESR \bullet Co}$$

$$\Delta V_{CAP} = \Delta V_{HUMP} \quad \text{for} \quad \text{step-down transients}$$

$$\Delta V_{CAP} = \Delta V_{SAG} \quad \text{for} \quad \text{step-up transients}$$

f_c = System Closed-Loop Bandwidth

The last term in Equation 13 is a direct consequence of the amount of output capacitance. After the initial spike, all the excessive charge is dumped into the output capacitors on step-down transients causing a temporary hump at the output; the output capacitors deliver extra charge to meet the load demand on step-up transients causing a temporary sag before the output inductors catch the load. The approximate response time intervals for removal and application of a transient load are defined by dTn and dTp, respectively, plus Td contributed by the propagation delay of the error amplifier of the controller. The critical inductances (Lcr1 and Lcr2) are the largest inductance that gives the fastest responses for step-down and step-up load transients, respectively [6].

$$\Delta V_{HUMP} \approx \frac{Istep \bullet (dTn + 2Td)}{2 \bullet Co} \quad \text{(EQ. 14)}$$

where

$$dTn = \frac{Istep \bullet L}{N \bullet V_1} \quad \text{for} \quad L \geq Lcr1$$

$$dTn \approx \frac{1}{4f_c} \quad \text{for} \quad L < Lcr1$$

$$Lcr1 = \frac{N \bullet V1}{4 \bullet Istep \bullet f_c}$$

$$\Delta V_{SAG} \approx \frac{Istep \bullet (dTp + 2Td)}{2 \bullet Co} \quad \text{(EQ. 15)}$$

where

$$dTp = \frac{Istep \bullet L}{N \bullet V_3 \bullet (Dmax - D)} \quad \text{for} \quad L \geq Lcr2$$

$$dTp \approx \frac{1}{4f_c} \quad \text{for} \quad L < Lcr2$$

$$V_3 = V_2 - \frac{Io}{N} \bullet R_{Q1}$$

$$Lcr2 = \frac{N \bullet V \bullet (Dmax - D)}{4 \bullet Istep \bullet f_c}$$

INPUT FILTER DESIGN

Another benefit of the interleaved approach is to reduce the input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering the input ripple current and allowing the designer to reduce the cost of input capacitors. Equation 16 defines the RMS value of the ripple current through the input capacitors, where the $K_{IN,CM}$ is the input-capacitor RMS current multiplier with respect to the output current, and the $K_{RAMP,CM}$ is the input-capacitor RMS current multiplier with respect to the inductor current ramp. Figures 7 and 8 plot these multipliers verse the duty cycle.

$$I_{IN,RMS} = \sqrt{K_{IN,CM}^2 \bullet Io^2 + K_{RAMP,CM}^2 \bullet I_{Lo,PP}^2} \quad \text{(EQ. 16)}$$

$$K_{IN,CM} = \sqrt{\frac{(N \bullet D - m + 1) \bullet (m - N \bullet D)}{N^2}} \quad \text{(EQ. 17)}$$

$$K_{RAMP,CM} = \sqrt{\frac{m^2(N \bullet D - m + 1)^3 + (m-1)^2(m - N \bullet D)^3}{12N^2D^2}} \quad \text{(EQ. 18)}$$

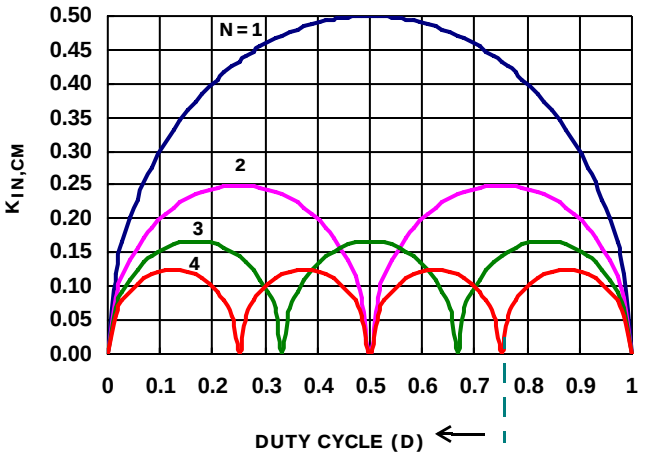


FIGURE 7. INPUT-CAPACITOR RMS CURRENT MUTIPLIER

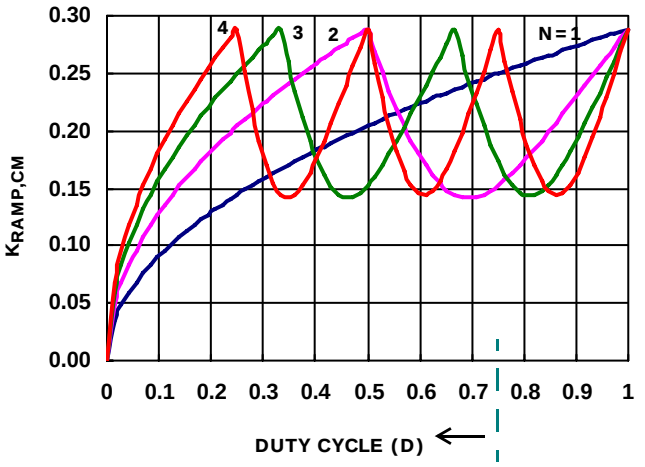


FIGURE 8. RAMP CURRENT MUTIPLIER

Other than being able to absorb the ripple current and dissipate the power defined in Equation 19, the input capacitors should be able to hold the input voltage within its operational limits during normal and dynamic modes.

$$P_{CIN} = I^2_{IN,RMS} \bullet ESR_{IN} \qquad \text{(EQ. 19)}$$

The required input capacitance for normal mode operation is defined in Equation 20.

$$Cin = \frac{Io(N \bullet D - m + 1)(m - N \bullet D)}{\Delta V_{IN,CAP} \bullet N^2 \bullet Fsw} \qquad \text{(EQ. 20)}$$

The $\Delta V_{IN,CAP}$ is the acceptable input voltage ripple contributed by the amount of input capacitance, of which is the input capacitors that filter most of pulsating currents. The peak-to-peak input ripple current through the input capacitors is defined in Equation 21.

$$I_{INCAP,PP} = \frac{Io}{N} + \frac{I_{Lo,PP}}{2} \qquad \text{(EQ. 21)}$$

The overall input voltage ripple induced by the ESR and capacitance of the input capacitors (at Cin) can be estimated with Equation 22. The spikes caused by the ESL of the input capacitors are assumed to be decoupled with low ESL ceramic capacitors.

$$V_{IN,RIPPLE} = \Delta V_{IN,CAP} + I_{INCAP,PP} \bullet ESR_{IN} \qquad \text{(EQ. 22)}$$

For high speed applications with limited input current slew rate (dI_{IN}/dt), the input capacitors provide most of the charge demanded by the converter due to load transients (0% to 100% step). The input capacitance should also meet the inequality relationship in Equation 23 to prevent the input voltage dip from being greater than $\Delta V_{IN,TRAN}$ and out of operational limits.

$$Cin > \frac{Po^2}{2\eta^2\left(\Delta V_{IN,TRAN} - ESR_{IN}\left(\frac{Io}{N} - I_{IN}\right)\right) \bullet V^2_{IN} \bullet \frac{dI_{IN}}{dt}} \qquad \text{(EQ. 23)}$$

An input inductor, defined in Equation 24, is also required to prevent the converter from drawing current at a higher slew rate than what the input source can respond. Thus, the input source will remain within its performance specifications when the converter responds to a high speed load transient.

$$Lin > \frac{1}{Cin}\left(\frac{2Po}{\pi\eta V_{IN} \bullet \frac{dI_{IN}}{dt}}\right)^2 \qquad \text{(EQ. 24)}$$

In addition, the input inductor helps reduce the peak-to-peak input ripple current reflected back to the input source, as approximated in Equation 25, with the assumption of negligible amount of $\Delta V_{IN,CAP}$ in Equation 22.

$$I_{IN,RIPPLE} \approx \frac{(ND - m + 1) \bullet (m - ND) \bullet Io \bullet ESR_{IN}}{Lin \bullet N^2 \bullet Fsw} \qquad \text{(EQ. 25)}$$

LOWER MOSFET POWER CALCULATION

The power dissipated in the lower MOSFET is dominated by the resistive loss due to currents conducted through the channel resistance (R_{Q2}), as defined in Equation 26.

$$P_{LOW,1} = R_{Q2} \bullet I^2_{Q2,RMS}$$

where

$$I_{Q2,RMS} = \sqrt{\left[\left(\frac{I_o}{N}\right)^2 + \frac{I^2_{Lo,PP}}{12}\right] \bullet (1 - D)} \qquad \text{(EQ. 26)}$$

An additional term can be added to the lower-MOSFET loss equation to account for its body-diode conduction loss during the dead time. This term is dependent on the diode forward voltage at a current Io/N, $V_{D(ON)}$, the switching frequency, Fsw, and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction intervals, respectively.

$$P_{LOW,2} = V_{D(ON)} \bullet Fsw \bullet \left[\left(\frac{Io}{N} + \frac{I_{PP}}{2} \right) t_{d1} + \left(\frac{Io}{N} - \frac{I_{PP}}{2} \right) t_{d2} \right] \quad \text{(EQ. 27)}$$

Thus, the total power dissipated in each lower MOSFET is approximated by the summation of Equations 26 and 27, as P_{LOW}. The overall lower MOSFETs' power losses in an N-phase converter is N times P_{LOW}.

$$P_{LOW} = P_{LOW,1} + P_{LOW,2} \quad \text{(EQ. 28)}$$

UPPER MOSFET POWER CALCULATION

Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times; the lower-MOSFET body-diode reverse-recovery charge, Q_{rr}; and the upper MOSFET $r_{DS(ON)}$ conduction loss. A large portion of the upper-MOSFET losses is due to currents conducted across the input voltage (V_{IN}) during switching intervals.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 29, the required time for this commutation is t_1 and the associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN} \bullet \left(\frac{Io}{N} + \frac{I_{Lo,PP}}{2} \right) \bullet \left(\frac{t_1}{2} \right) \bullet Fsw \quad \text{(EQ. 29)}$$

Similarly, the upper MOSFET begins conducting as soon as it begins turning on. In Equation 30, this transition occurs over a time t_2, and the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN} \bullet \left(\frac{Io}{N} - \frac{I_{Lo,PP}}{2} \right) \bullet \left(\frac{t_2}{2} \right) \bullet Fsw \quad \text{(EQ. 30)}$$

A third component involves the lower MOSFET's reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET's body diode can recover all of Q_{rr}, it is conducted through the upper MOSFET across V_{IN}. The power dissipated is simply that in Equation 31:

$$P_{UP,3} = V_{IN} \bullet Q_{rr} \bullet Fsw \quad \text{(EQ. 31)}$$

Finally, the resistive part of the upper MOSFETs is given in Equation 32 as $P_{UP,4}$.

$$P_{UP,4} = R_{Q1} \bullet I^2_{Q1,RMS} \quad \text{(EQ. 32)}$$

where

$$I_{Q1,RMS} = \sqrt{\left[\left(\frac{Io}{N} \right)^2 + \frac{I^2_{Lo,PP}}{12} \right] \bullet D}$$

where R_{Q1} is the on resistance of the upper MOSFET.

The total power dissipated in each upper MOSFET can now be approximated as the summation of Equations 29 through 32, as P_{UP}. The overall upper MOSFETs' power losses in an N-phase converter is N times P_{UP}.

$$P_{UP} = P_{UP,1} + P_{UP,2} + P_{UP,3} + P_{UP,4} \quad \text{(EQ. 33)}$$

DRIVER LOSSES CALCULATION

The driver losses due to the gate charge (Qg) of the MOSFETs should be investigated thoroughly to prevent over stressing, especially in high-switching frequency applications. The switching losses of each-channel driver and its corresponding average driver current due to the gate charge can be estimated with Equations 34 and 35, respectively:

$$P_{DR} = \left(\frac{Qg1 \bullet V^2_{DR\_UP}}{V_{GS1}} + \frac{Qg2 \bullet V^2_{DR\_LOW}}{V_{GS2}} \right) \bullet Fsw \quad \text{(EQ. 34)}$$

$$I_{DR} = \left(\frac{Qg1 \bullet V_{DR\_UP}}{V_{GS1}} + \frac{Qg2 \bullet V_{DR\_LOW}}{V_{GS2}} \right) \bullet Fsw \quad \text{(EQ. 35)}$$

where Qg1, Qg2 and V_{GS1}, V_{GS2} are defined in the MOSFET datasheet and V_{B_UP} and V_{B_LOW} are drive voltages for both upper and lower FETs, respectively.

CONTROL LOOP DESIGN

The overall system can be considered as N voltage-mode buck converters with/without droop in parallel and synchronized operation. The current loop is used to balance currents among all active channels and determine the droop, and it is a slower loop, compared to the voltage loop. Thus, the system can be simplified as shown in Figure 9, for setting up an initial feedback compensation. Equation 36 defines the approximate open-loop transfer function.

$$Ho(S) = G \bullet He(S) \bullet \frac{Zo(S)}{Z_{LO}(S) + Zo(S)} \quad \text{(EQ. 36)}$$

Note that the droop loop is not accounted in Equation 36; however, it can be included in the PSpice simulation as shown in Figure 9.

Possible tune-up might be required for and optimum loop response with a tool such as a Venerable system. Refer to the ISL6557A data sheet [4] for a detailed discussion.

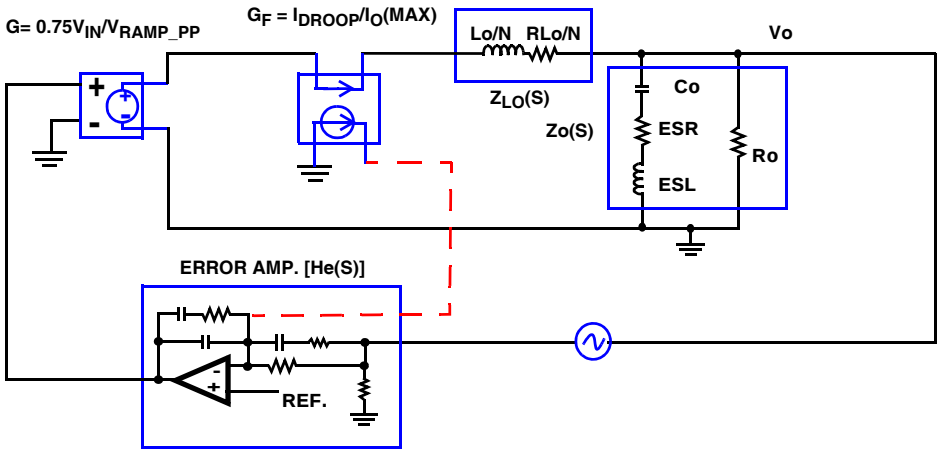


FIGURE 9. SIMPLIFIED LOOP MODEL

SUMMARY OF DESIGN

Table 1 shows the calculation results of critical design parameters for the reference design, a four-channel interleaved DC-DC buck converter.

Table 2 summarizes an approximate power dissipation analysis for the reference design.

TABLE 1. CRITICAL DESIGN PARAMETERS

PARAMETER	CONDITION	VALUE	UNIT
DUTY CYCLE AND SWITCHING FREQUENCY			
D	V_{IN} = 12, Vo(Io = 0) = 1.564V, Io = 100A	14.1	%
Fsw	RT = 226kΩ (measured)	125	kHz
INPUT CAPACITORS			
Cin (min)	V_{IN} = 12, Po = 152W, dI_{IN}/dt = 0.1A/us, η = 0.83, $\Delta V_{IN,TRAN}$ = 1.0V	1000	µF
$I_{IN,RMS}$	V_{IN} = 12.6V, Io = 100A	13.1	A
OUTPUT CAPACITORS			
Co(min)	f_c = Fsw/10 = 12.5kHz, f(step) = 95mV	16700	µF
Io_{RMS}	Lo(Io) = 0.6µH, V_{IN} = 12.6V	3.1	A
ESR(max)	Istep = 100A, f(step) = 80mV	0.8	mΩ
OUTPUT INDUCTORS (ASSUMING EQUAL DISTRIBUTION AMONG OUTPUT INDUCTORS)			
$I_{Lo,PP}$	Lo(Io) = 0.6µH, V_{IN} = 12.6V	19.4	A
I_{PP}	Lo(Io) = 0.6µH, V_{IN} = 12.6V, N = 4	10.0	A
$I_{Lo,Peak}$	Lo(Io) = 0.6µH, V_{IN} = 12.6V	34.7	A
$I_{Lo,RMS}$	Lo(Io) = 0.6µH, V_{IN} = 12.6V	25.6	A
SYNCHRONOUS LOWER FETs			
$I_{Q1,RMS}$	V_{IN} = 12.6V	23.9	A
$I_{Q2,RMS}$	V_{IN}=11V	10.0	A

TABLE 2. FULL-LOAD POWER DISSIPATION BUDGET

ELEMENTS	POWER DISSIPATION AT 100A LOAD		
	11V	12V	12.6V
CALCULATION CONDITIONS			
Switching Frequency	125kHz		
Per-Channel Output Inductor	0.600µH at Full load		
MOSFET $r_{DS(ON)}$ Value	at Tj = +60°C		
PER-CHANNEL LOSSES (xN)			
Upper FETs Conduction	0.573W	0.528W	0.503W
Upper FETs Switching	1.055W	1.152W	1.212W
Lower FETs Conduction	2.215w	2.250W	2.270W
Lower FETs Body-diode Conduction	0.294w	0.293W	0.293W
Output Inductor Copper	0.784W	0.785W	0.786W
Output Inductor Core	0.603W	0.623W	0.634W
Per-Channel Driver	0.432W	0.432W	0.432W
OTHERS (x1)			
Input Inductors Copper	0.547W	0.466W	0.424W
Input Inductors Core	Negligible		
Input Capacitors	0.752W	0.771W	0.776W
Output Capacitors	0.003W	0.0039W	0.0044W
PCB Copper	3.033W	2.953W	2.912W
Miscounted and Error	3.25W	3.1W	3.09W
TOTAL	31.42W	31.55W	31.72W

LAYOUT CONSIDERATIONS

Other than the layout considerations discussed in the ISL6558 data sheet, below are the two possible rules to obtain the best ripple current cancellation effect and

current distribution among capacitors at both the input and output. Refer to [5] for other layout rules.

1. Tie each-channel inductor as close as practical before they are connected to the output capacitors.

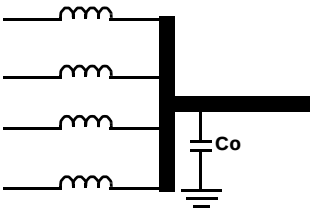


FIGURE 10. OUPTUT FILTER LAYOUT CONFIGURATION

2. Tie all upper FETs as close as practical before they are connected to the input capacitors.

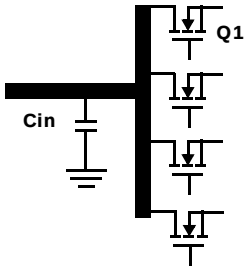


FIGURE 11. INPUT FILTER LAYOUT CONFIGURATION

Experimental Results

The ISL6558EVAL1Z evaluation board is capable of 100A continuous load current and handling 100A/µs or higher speed load transients. The evaluation board meets the design specifications indicated in Table 3.

TABLE 3. ISL6558EVAL1Z PRELIMINARY SPECIFICATIONS

PARAMETER	CONDITION	MIN	TYP	MAX
Input Voltage	VCC12	11V	12V	12.6V
Control Voltage	VCC5	4.5V	5V	5.5V
Transient Regulation	100A Step 100A/µs	1.485V		1.585V
Continuous Load	+25°C with 200LFM		100A	
Transient Slew Rate			100A/µs	
Overcurrent	+25°C with 200LFM		150A	
Minimum Airflow			200 LFM	
Switching Frequency			125kHz	
Efficiency			82.8%	
Undervoltage Rising Threshold			0.92Vo	
Undervoltage Falling Threshold			0.9Vo	
Overvoltage Threshold			1.15Vo	

EVALUATION BOARD OPERATION

TABLE 4. EQUIPMENT LIST

EQUIPMENT	EQUIPMENT DESCRIPTIONS
BOARDS USED	**ISL6558EVAL1Z Rev. B, #1 and #2**
POWER SUPPLIES	1. Hewlett Packard 6653A S/N: 3621A-03425 2. Agilent 20V/100A S/N: US30390609
OSCILLOSCOPE	LeCroy LT364L S/N: 01106
MULTIMETERS	Fluke 8050A S/N: 2466115 and 3200834
LOAD	1. Chroma 63103 S/N: 631030002967 2. Chroma 63103 S/N: 631030003051
CURRENT PROBE AMPLIFIER	LeCroy AP150 SN: 0242
FAN	POPST-MOOREN TYP 4600X (4098547)

- Table 4 summarizes the equipment used for the performance evaluation.
- Apply the input voltage VCC12 (12V) prior to the control voltage VCC5 (5V). This sequencing results in initializing the HIP6001B driver before the ISL6558 starts, and retains the soft-start interval. Vice versa, the ISL6558 could produce maximum duty cycle PWM drive signal, which results in an output overvoltage trip due to lack of soft-start.

EVALUATION BOARD MODIFICATION TIPS

- For 3-phase operation, remove R1 and place JP3 to OFF position.
- For 2-phase operation, remove R1 and R13 and place JP3 and JP2 to OFF position.
- SW1 is used to engage or remove the load transient generator.
- Use R15, R16, R17, and R18 to program the load transient speed. The higher values these resistors, the slower the transient.
- Reduce the winding of Toroidal Cores (L2-L5) by one turn to obtain 400nH output inductance.

EFFICIENCY

The efficiency data, as plotted in Figure 12, are taken with a PAPST-MOTOREN TYP 4600X fan turned on 8” away from the input end of the evaluation board at room temperature. The figure shows that the converter with higher output inductance (650nH) operates at a higher efficiency than that with 400nH output inductance, by 1.5% at full load. The efficiency improvement is at the expense of the transient performance, as illustrated later.

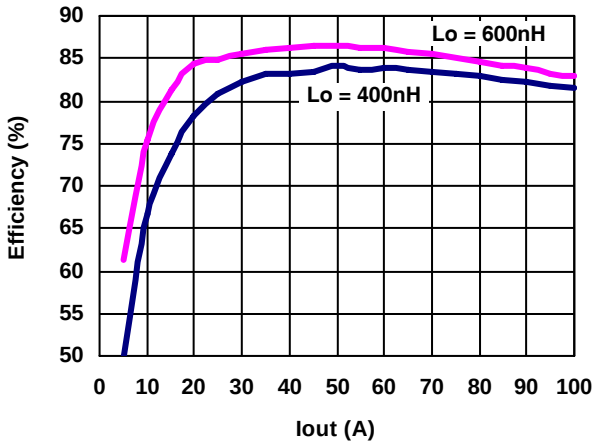


FIGURE 12. EFFICIENCY

OUTPUT SOFT-START AND TURN-OFF

With the input voltage (VCC12) staying within operational limits, when the control voltage VCC5 reaches above the POR rising threshold (4.38V) of the ISL6558, the FS/EN pin is released from ground and the output begins a monotonic rise comprised of 2048 digital steps, as shown in Figure 13. At the end of the soft-start interval, the PGOOD signal transitions to indicate the output voltage is within specification.

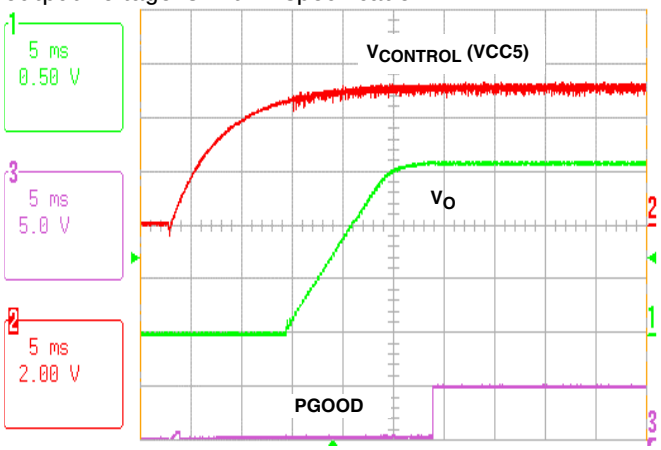


FIGURE 13. SOFT-START WAVEFORMS

As shown in Figure 14, the converter is disabled when the control voltage (VCC5) is pulled below the POR falling threshold (3.88V) of the ISL6558. The PGOOD signal is pulled low indicating the output voltage is out of regulation. The ISL6612A enters Tri-State® and holds both upper and lower drive signals low. The L-C resonant tank is broken and cannot cause negative ringing at the output since the lower FET is turned off, blocking any negative current during the PWM Tri-State® period. When the PWM input signal moves outside the shutdown window, the ISL6612A is re-initialized; i.e., the lower drive stays high and the upper drive stays low.

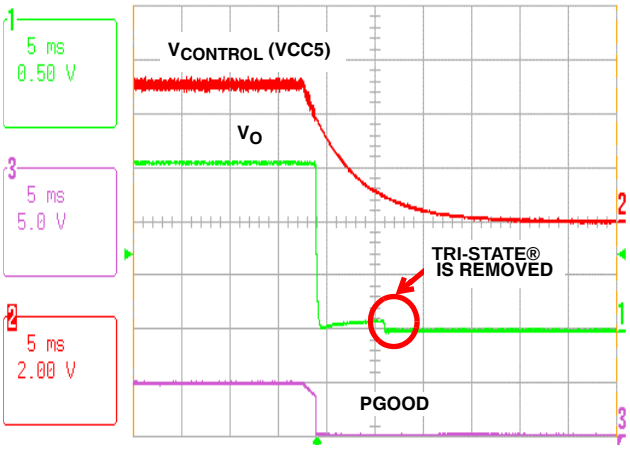


FIGURE 14. TURN-OFF WAVEFORMS

TRANSIENT RESPONSES

A transient load generator is populated on the board to allow users to test high-speed load transients of the converter. Current setting of the generator provides about 120A load step with 100A/µs on the rising edge and 140A/µs on the falling edge with output droop configured. The input current rises/falls at a speed limited by the input inductor and input capacitors during step-up/step-down transients.

The transient performance for two different values of output inductors have been compared and summarized in Table 5. It shows that the lower the output inductance is, the better the transient performance is, but it comes at the expense of lower efficiencies, as illustrated in the section entitled EFFICIENCY. In addition, the asymmetric transient appears in the converter with higher output inductance (Lo = 650nH), as can be easily seen in Figures 19 and 22. This is because 650nH is much greater than its critical inductance [6] (around 400nH or smaller). Without the output droop configured, the output has a much higher peak-to-peak voltage spike, and it requires much more output capacitors to achieve the same transient performance as that with droop setting.

TABLE 5. TRANSIENT RESPONSE

INDUCTANCE VALUE (nH)	STEP-UP/ STEP-DOWN	Vpp (mV)	DROOP	FIGURE
400		116	x	15
400	Step-up	100	x	16
400	Step-down	109	x	17
400		166		18
650		133	x	19
650	Step-up	111	x	20
650	Step-down	119	x	21
650		178		22

1. Transient Response with Lo = 400nH (4 Turns)

Note that the measurement is taken without having the C300 (1000µF) input capacitor on the board. The transient response with 400nH output inductance is shown in Figures 15 to 18.

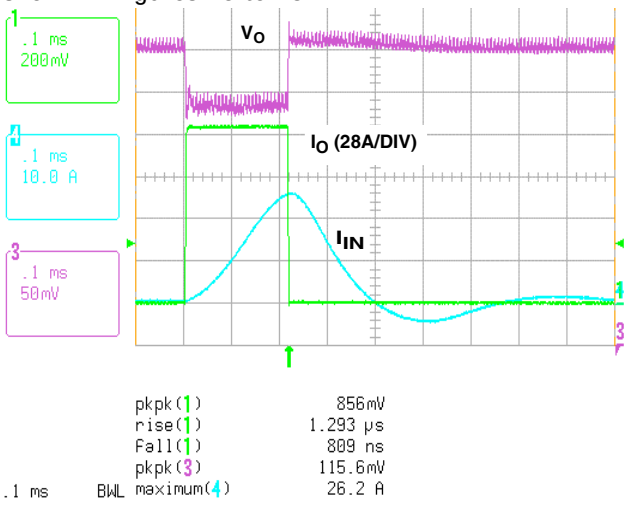


FIGURE 15. TRANSIENT RESPONSE WITH DROOP

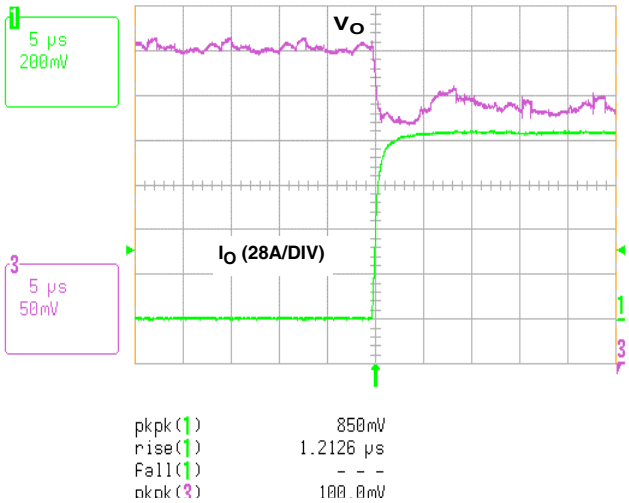


FIGURE 16. EXPANSION OF STEP-UP TRANSIENTS

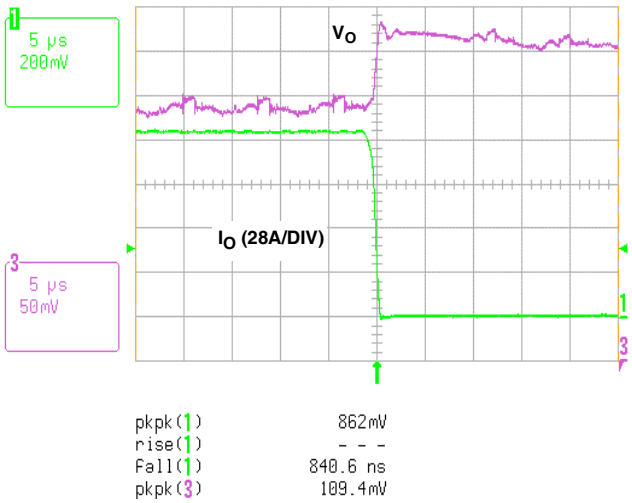


FIGURE 17. EXPANSION OF STEP-DOWN TRANSIENTS

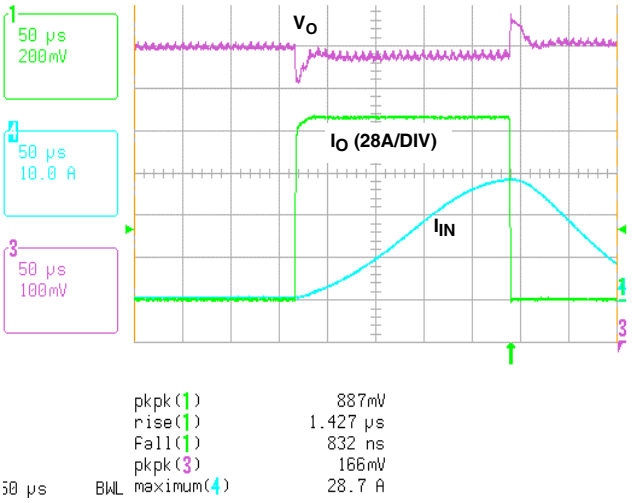


FIGURE 18. TRANSIENT RESPONSE WITHOUT DROOP

2. Transient Response with Lo = 650nH (5 Turns)

Note that the measurement is taken without having the C300 (1000µF) input capacitor on the board. The transient response with 650nH output inductance is shown in Figures 19 to 24.

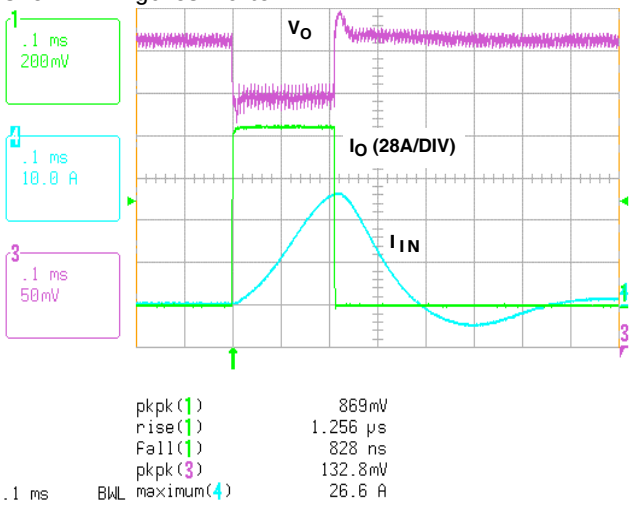


FIGURE 19. TRANSIENT RESPONSE WITH DROOP

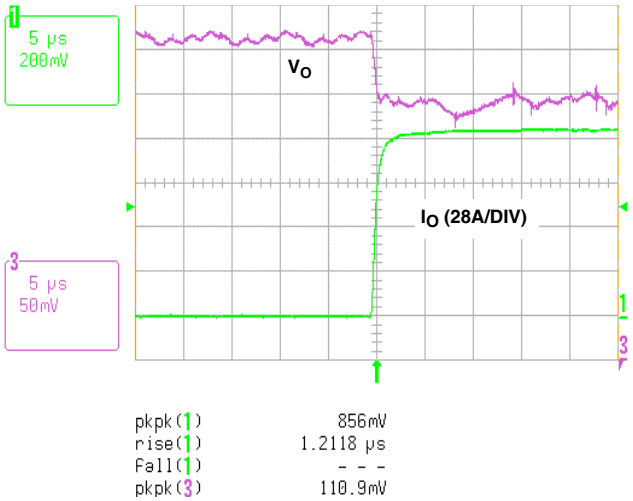


FIGURE 20. EXPANSION OF STEP-UP TRANSIENTS

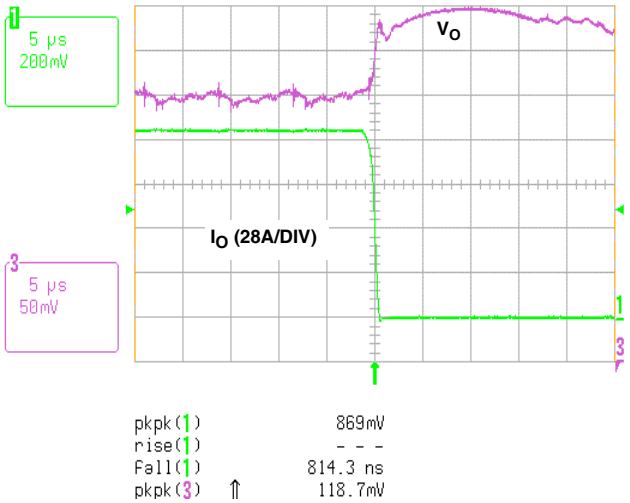


FIGURE 21. EXPANSION OF STEP-DOWN TRANSIENTS

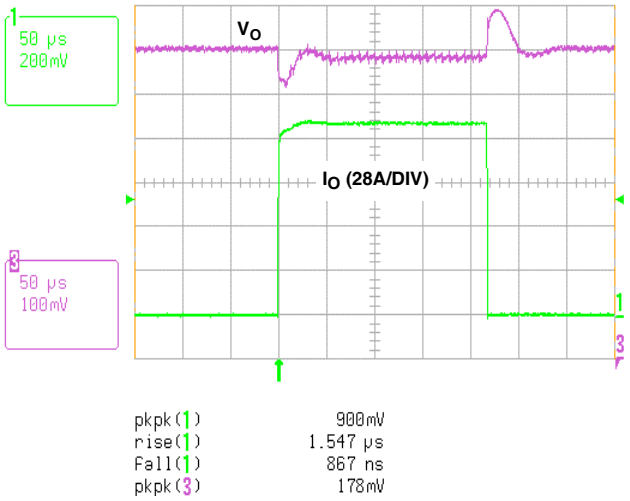


FIGURE 22. TRANSIENT RESPONSE WITHOUT DROOP

3. Transient Response with Lo = 650nH and Added C300 (1000µF)

As shown in Figure 19, the input current is seen to be as high as 26A, which could cause the input source to overcurrent trip. Adding an 1000µF input capacitor parallel to C3 helps supply currents to the converter at load transients and reduces the peak current by much as 10A, as shown in Figure 23. Placing the 1000µF capacitor at the input side of L1 is not as effective on reducing the input peak current as in previous case, as shown in Figure 24. In addition, cutting down the input inductance value, at the cost of higher input current slew rate, is another possible way to reduce the input peak current due to load transients. Note that the effective input inductance seen by the converter is higher than the on-board input inductor due to the long source leads of the bench power supply. Hence, users would see different input current waveforms because of the difference of the effective input inductance of their bench setups.

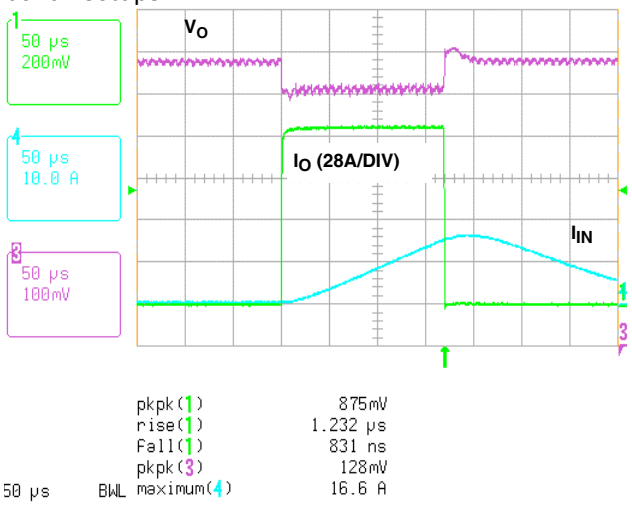


FIGURE 23. TRANSIENT RESPONSE WITH ADDED 1000µF IN PARALLEL WITH C3

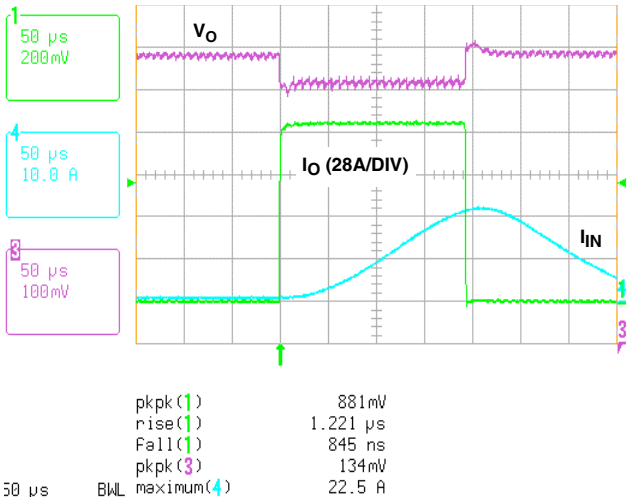


FIGURE 24. TRANSIENT RESPONSE WITH ADDED 1000µF AT INPUT CONNECTORS

OVERCURRENT AND SHORT CIRCUIT

When the converter is momentarily shorted or overloaded, as shown in Figure 25, the converter runs hiccup mode with a very narrow duty cycle and long switching period. PGOOD stays low during the overcurrent period; it indicates the output voltage is within regulation limits after the short is removed and the output completes a soft-start interval.

As shown in Figure 26, the converter can sustain a permanent short circuit remaining in hiccup modes with a frequency of 44Hz. The average load current and the average power dissipation in each power component are reduced significantly; thus, the converter can stay at a short without causing any permanent damage or thermal issues.

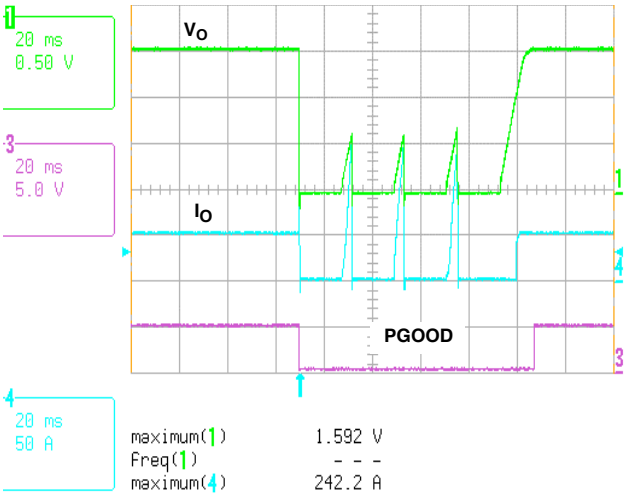


FIGURE 25. OVER-LOADED OUTPUT WAVEFORMS

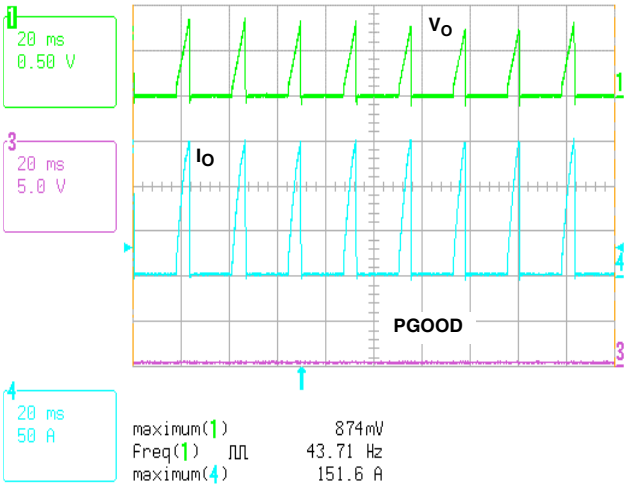


FIGURE 26. SHORT-CIRCUIT WAVEFORMS

OVERVOLTAGE SHUTDOWN

With the COMP pin momentarily tied to a 4V voltage source with respect to the ground, the error voltage jumps high and the duty cycle increases. Thus, the output voltage rises up immediately until it reaches the overvoltage threshold setting the OV latch and triggers the PWM outputs low. PGOOD is pulled low indicating output out of regulation, as shown in Figure 27.

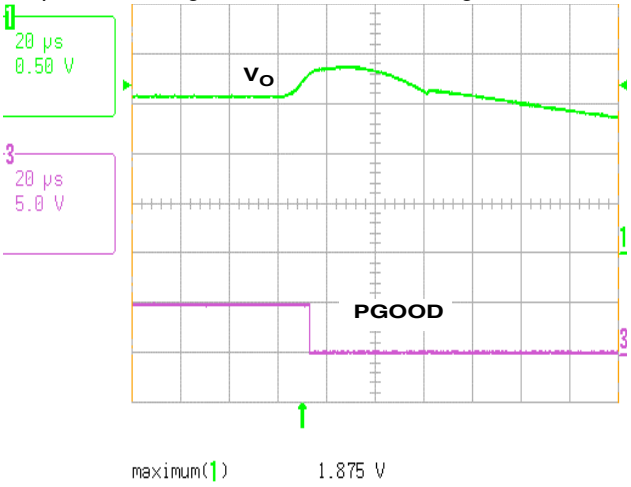


FIGURE 27. OVERVOLTAGE WAVEFORMS

Conclusion

The superior performance of Intersil's ISL6558 4-phase controller, coupled with Intersil's ISL6612A driver, has been demonstrated in the reference design of a 150W interleaved DC-DC buck converter. An efficiency of 83% at 1.527V output and 100A full load has been achieved. The reference design provides an option to implement droop or no droop and allows users to evaluate the transient performance with the on-board load transient generator.

This application note provides a step-by-step design procedure for the multi-phase converter, which allows for easier component selection and customization of this reference design for a broader base of applications. Users can use equations, presented in the section entitled "Converter Design" on page 3, to fully characterize power-train components such as the I/O filters and synchronous rectifiers. By entering these calculations in a worksheet, users can do numerical iterations and choose appropriate components and switching frequency for their applications in an user-friendly manner. Furthermore, the loop response of the system can be roughly approximated using the simplified model.

In addition, extensive experimental results give users a better understanding of the operation of the converter, the ISL6558 four-phase PWM controller, and the ISL6612A synchronous-rectified driver.

TABLE 6. TERM DEFINITIONS

TERM	DEFINITIONS
Cin	Input Capacitance
Co	Output Capacitance
D	Ratio of ON Interval of Upper FET to Single Channel Switching Period, Duty Cycle
Dmax	Maximum Duty Cycle of the Controller
dV_{Co}	Output Voltage Ripple due to Output Capacitance
dV_{ESL}	Ripple Voltage Contributed by ESL of Output Capacitors
dV_{ESR}	Ripple Voltage Contributed by ESR of Output Capacitors
ΔV_{ESL}	Initial Transient Spike due to ESL
$\Delta V_{IN,CAP}$	Allowable Input Voltage Ripple Contributed by the Input Capacitors
$\Delta V_{IN,TRAN}$	Voltage dip at Input Capacitors due to Load Transient
ESL	Overall ESL of Output Capacitors
ESR	Overall ESR of Output Capacitors
ESR_{IN}	Overall ESR of Input Capacitors
f_c	System Closed-Loop Bandwidth
Fsw	Per-Channel Switching Frequency
He	Transfer Function of Error Amplifier
Ho	Open Loop Transfer Function for Simplified Model
I_{DR}	Driver Current
I_{IN}	Input Current
$I_{IN,RMS}$	RMS Current thru Input Capacitors
$I_{IN,RIPPLE}$	Ripple Current thru Input Inductor
$I_{INCAP,PP}$	Peak-to-Peak Current thru Input Capacitors
I_{LO}	Current thru Each-Channel Inductor
$I_{Lo,PEAK}$	Peak Current thru Each-Channel Inductor
$I_{Lo,PP}$	Ripple Current thru Each-Channel Inductor
$I_{Lo,RMS}$	RMS Current thru Each-Channel Inductor
I_{PP}	Overall Ripple Current thru Output Capacitors
Io	Output Load Current
IQ1	Current thru Upper FET, Q1
$I_{Q1,RMS}$	RMS Current thru Upper FET, Q1
IQ2	Current thru Lower FET, Q2
$I_{Q2,RMS}$	RMS Current thru Upper FET, Q2
Istep	Load Transient Step
Lcr1	Critical Inductance for Step-up Load Transient
Lcr2	Critical Inductance for Step-down Load Transient
Lin	Input Inductor
Lo	Inductance of Each-Channel Inductor

TABLE 6. TERM DEFINITIONS (Continued)

TERM	DEFINITIONS
m	Maximum Number of Channels Having Positive Slope within Any Time Interval
N	Number of Active Channels
P_{CIN}	Power Dissipation of Input Capacitors
P_{DR}	Driver Switching Losses
P_{LOW}	Power Dissipation of Per-Channel Lower FET
Po	Output Power
P_{UP}	Power Dissipation of Per-Channel Upper FET
η	Output Efficiency
Qg	Total Gate Charge of Bridge MOSFETs at V_{GS}
Ro	Output Load Resistance
R_{Q1}	Rds(on) of Upper Switch, Q1
R_{Q2}	Rds(on) of Lower Switch, Q2
Vcc	Bias Voltage of Drivers
$V_{D(ON)}$	Body Diode Drop of Lower FET
V_{IN}	Input Voltage
$V_{IN,RIPPLE}$	Input Voltage Ripple Without Input Inductor
Vo	Output Voltage
Vo_{RIPPLE}	Output Voltage Ripple
Zo	Impedance of Output Capacitors and Load

References

Intersil documents are available on the web at http://www.intersil.com.

[1] Intersil's ISL6558 Data Sheet, File No. FN9027.

[2] Intersil's ISL6612A, ISL6613A Data Sheet, File No. FN9159.

[3] Intersil's HIP6602A Data Sheet, File No. FN4902.

[4] Intersil's ISL6557A Data Sheet, File No. FN9058.

[5] "PCB Design Guidelines For Reduced EMI." Texas Instrument: SZZA009, November 1999.

[6] Pit-Leong Wong, Fred C. Lee, Peng Xu, and Kaiwei Yao. "Critical Inductance in Voltage Regulator Modules," APEC, 2002, pp. 203-209.

Appendix

1. Schematics of Reference Design and Load Transient Generator.
2. Bill of Materials and Layout of Evaluation Board.

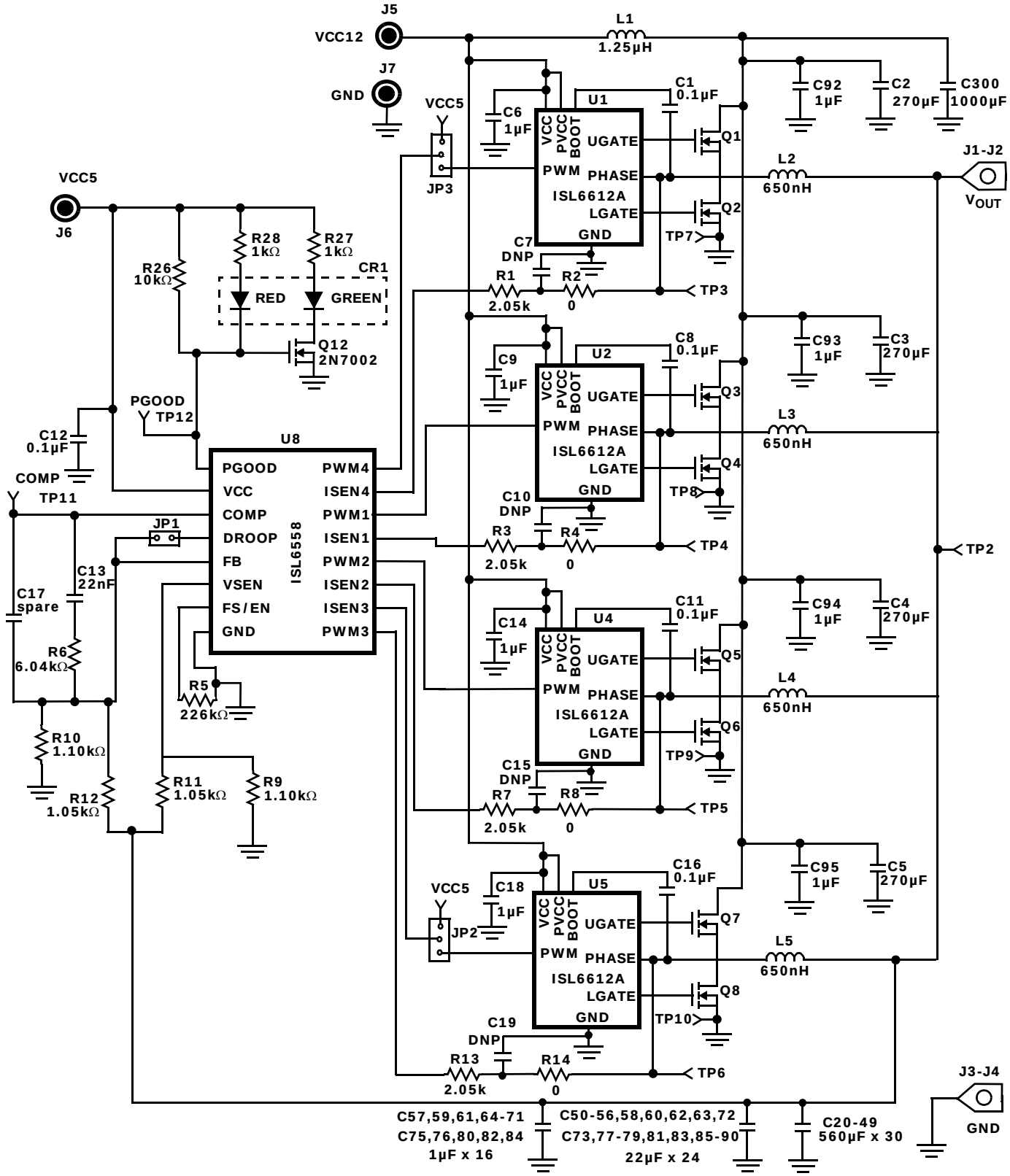


FIGURE 28. REFERENCE DESIGN CIRCUIT

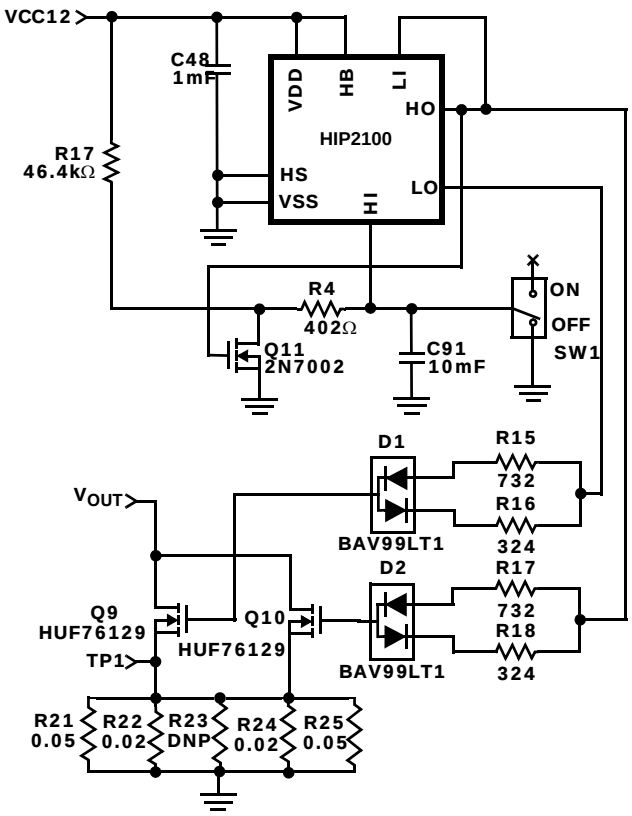


FIGURE 29. LOAD TRANSIENT GENERATOR CIRCUIT

Bill of Materials

QTY	REFERENCE	DESCRIPTION	PACKAGE	VENDOR	PART NO.
1	CR1	RED/GREEN LED	SMT	Lumex	SLL-LXA3025IGC
5	C1, C8, C11, C12, C16	0.1mF, 25V, Y5V, Ceramic Capacitor	0805	Various	
4	C2, C3, C4, C5	270mF, 16V, Organic Capacitor	Radial	OS-CON	16SP270M
25	C6, C9, C14, C18, C57, C59, C61, C64-71, C74-76, C80, C82, C84, C92, C93, C94, C95	1.0mF, 25V, Y5V, Ceramic Capacitor	1206	Various	
5	C7, C10, C15, C17, C19	Spare	603		
1	C13	22nF, 25V, X7R, Ceramic Capacitor	0603	Various	
30	C20-C49	560mF, 4V, Organic Capacitor	Radial	Sanyo	4SP560M
24	C50-56, C58, C60, C62, C63, C72, C73, C77-79, C81, C83, C85-90	22mF, 6.3V, X5R, Ceramic Capacitor	1206	Various	
1	C91	10mF, 6.3V, X5R,Ceramic Capacitor	1206	Various	
1	C300	1000mF, 16V, Aluminum Capacitor	Radial	Panasonic	EEUFC1C102
2	D1, D2	Dual Diode	SOT23	Various	BAV99

Bill of Materials (Continued)

QTY	REFERENCE	DESCRIPTION	PACKAGE	VENDOR	PART NO.
1	JP1	1-Position Header	100mil Centers	Berg	68000-236
1		Jumper		Berg	71363-102
2	JP2,JP3	3-Position Jumper Header	100mil Centers	Berg	68000-236
2		Jumpers		Berg	71363-102
4	J1-J4	Terminal Connector	Solder Mount	Burndy	KPA8CTP
2	J5,J6	Female Banana Connector, Red	Screw On	Johnson Components	111-0702-001
1	J7	Female Banana Connector, Black	Screw On	Johnson Components	111-0703-001
1	L1	1.25mH, T60-26 core, 5T AWG 16	Thru Hole	Various	
4	L2, L3, L4, L5	650nH, T68-8A/90 core,5T AWG14	Thru Hole	Various	
4	Q1, Q3, Q5, Q7	Power MOSFET	TO-263AB	Intersil	HUF76143S3S
4	Q2, Q4, Q6, Q8	Power MOSFET	TO-263AB	Intersil	HUF76145S3S
2	Q9, Q10	Power MOSFET	TO-252AA	Intersil	HUF76129D3S
2	Q11, Q12	General Purpose MOSFET	SOT23	Various	2N7002
4	R1, R3, R7, R13	Resistor,2.05kW,1%,1/10W	0603	Various	
4	R2, R4, R8, R14	Resistor, Jumper 0W,1/10W	0603	Various	
1	R5	Resistor,226kW,1%,1/10W	0603	Various	
1	R6	Resistor,6.04kW,1%,1/10W	0603	Various	
2	R9, R10	Resistor,1.10kW,1%,1/10W	0603	Various	
2	R11, R12	Resistor,1.05kW,1%,1/10W	0603	Various	
2	R15, R17	Resistor,732W,1%,1/10W	0603	Various	
2	R16, R18	Resistor,324W,5%,1/10W	0603	Various	
1	R19	Resistor,46.4kW,5%,1/10W	0603	Various	
1	R20	Resistor,402W,1%,1/10W	0603	Various	
2	R21, R25	Resistor,0.050W,1%,1W	2512	Vishay	WSL2512R050FB43
2	R22, R24	Resistor,0.020W,1%,1W	2512	Vishay	WSL2512R020FB43
1	R23	Spare	2512		
1	R26	Resistor,10kW,1%,1/10W	0603	Various	
2	R27, R28	Resistor,1.0kW,1%,1/8W	0805	Various	
1	SW1	Switch,DPST	SMT	C&K Components	GT11MSKE
2	TP1, TP2	Probe Socket	Thru Hole	Tektronix	1314353-00
6	TP3, TP4, TP5, TP6, TP11, TP12	Small Test Point	Thru Hole	Jolo	SPCJ-123-01
4	TP7, TP8, TP9, TP10	Large Test Point	Thru Hole	Keystone	1514-2
4	U1, U2, U4, U5	Synchronous Buck Driver IC	8 Lead SOIC	Intersil	ISL6612A
1	U8	Multi-phase Buck Controller IC	16 Lead SOIC	Intersil	ISL6558CB
1	U6	MOSFET Driver IC	8 Lead SOIC	Intersil	HIP2100IB

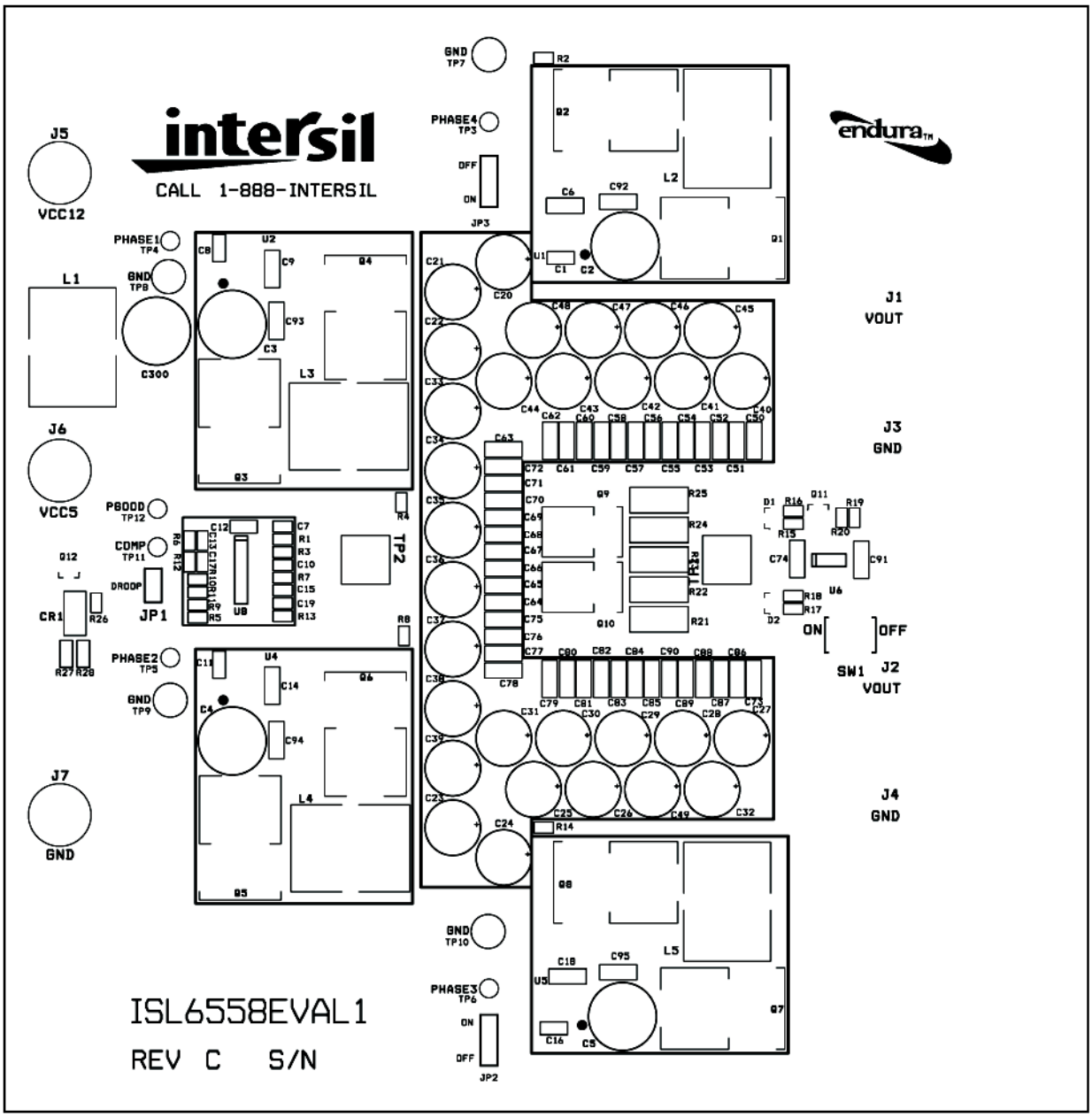


FIGURE 30. TOP SILKSCREEN

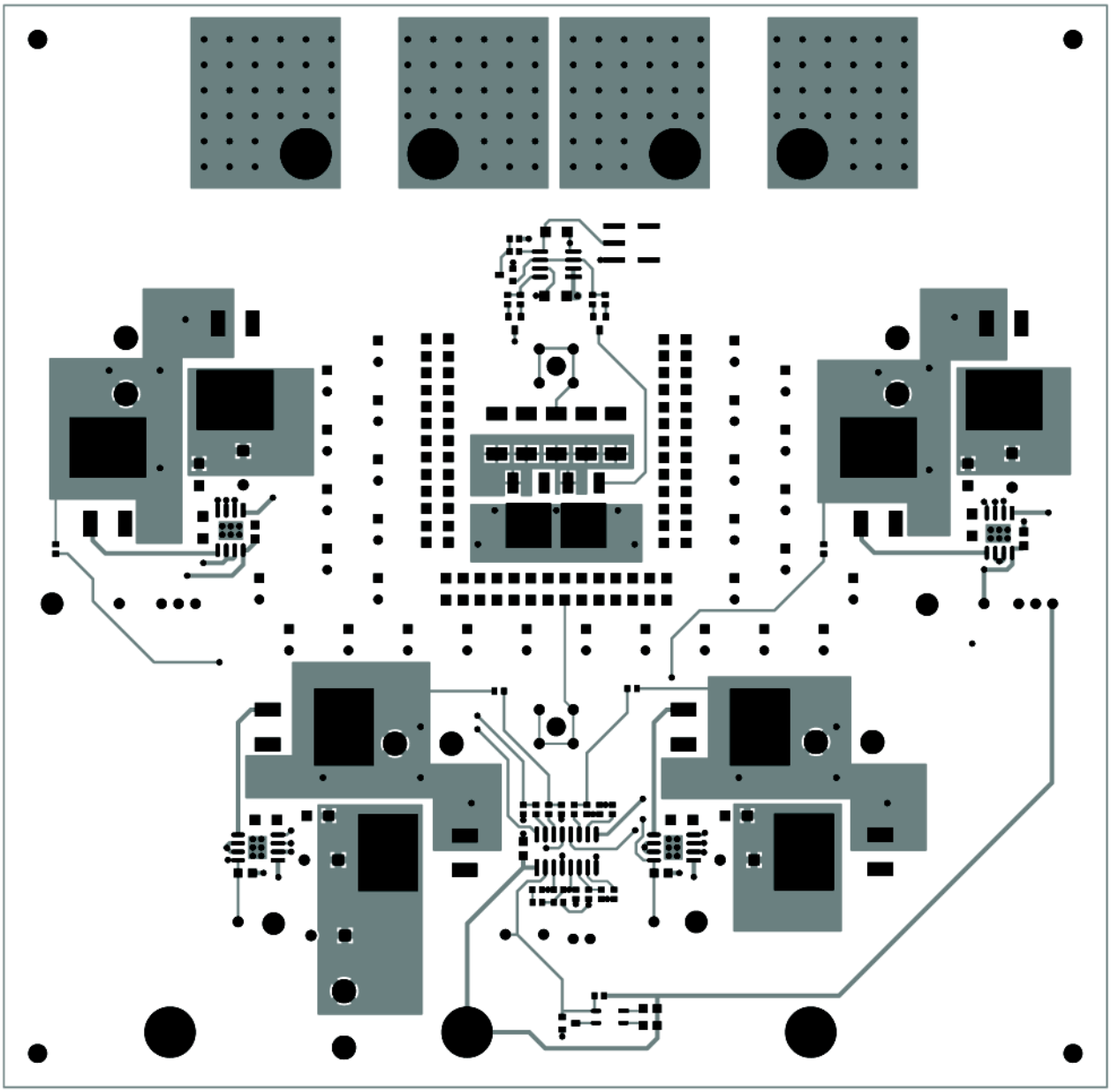


FIGURE 31. LAYER 1 TOP COPPER

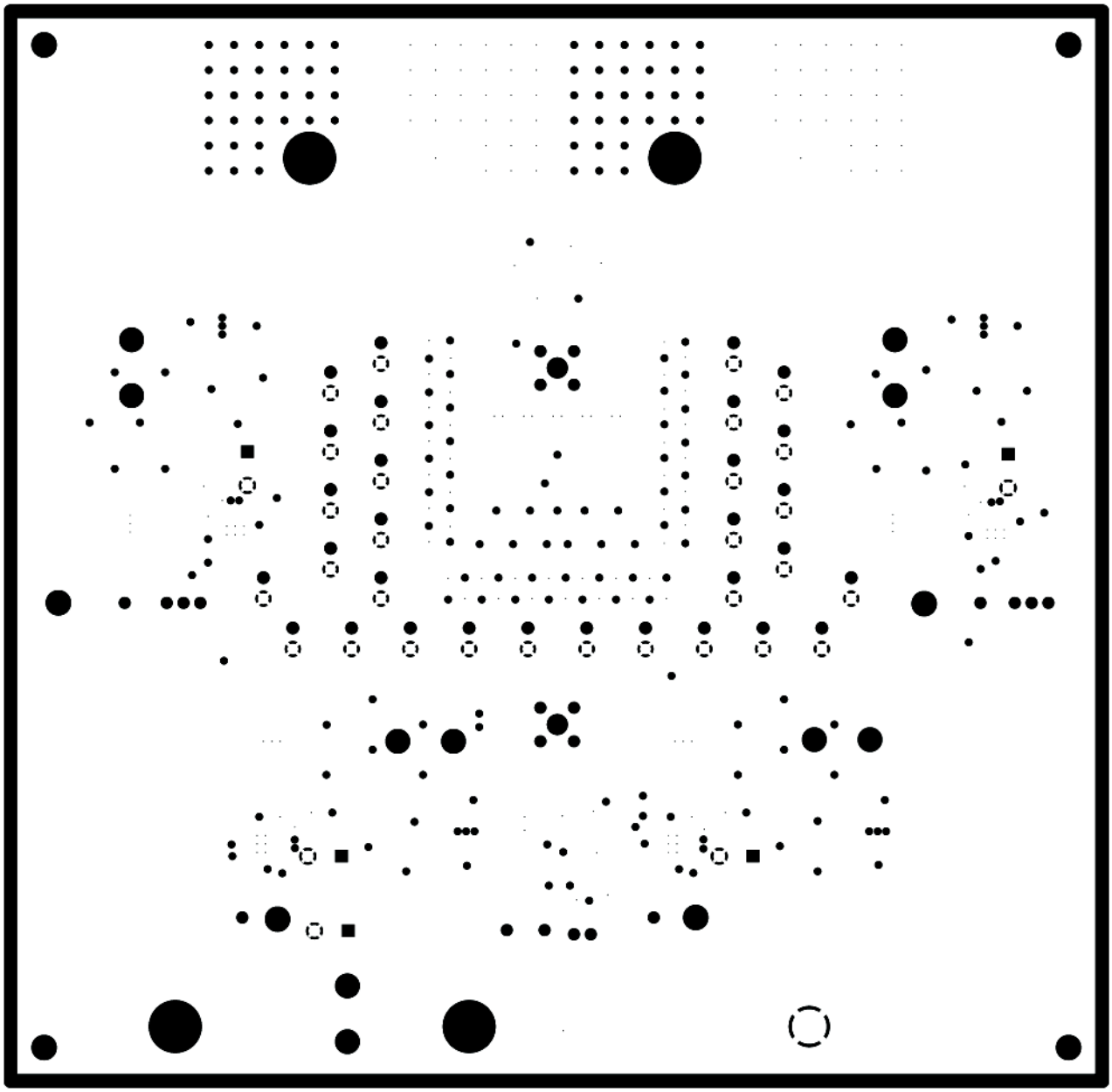


FIGURE 32. LAYER 2 GROUND PLANE

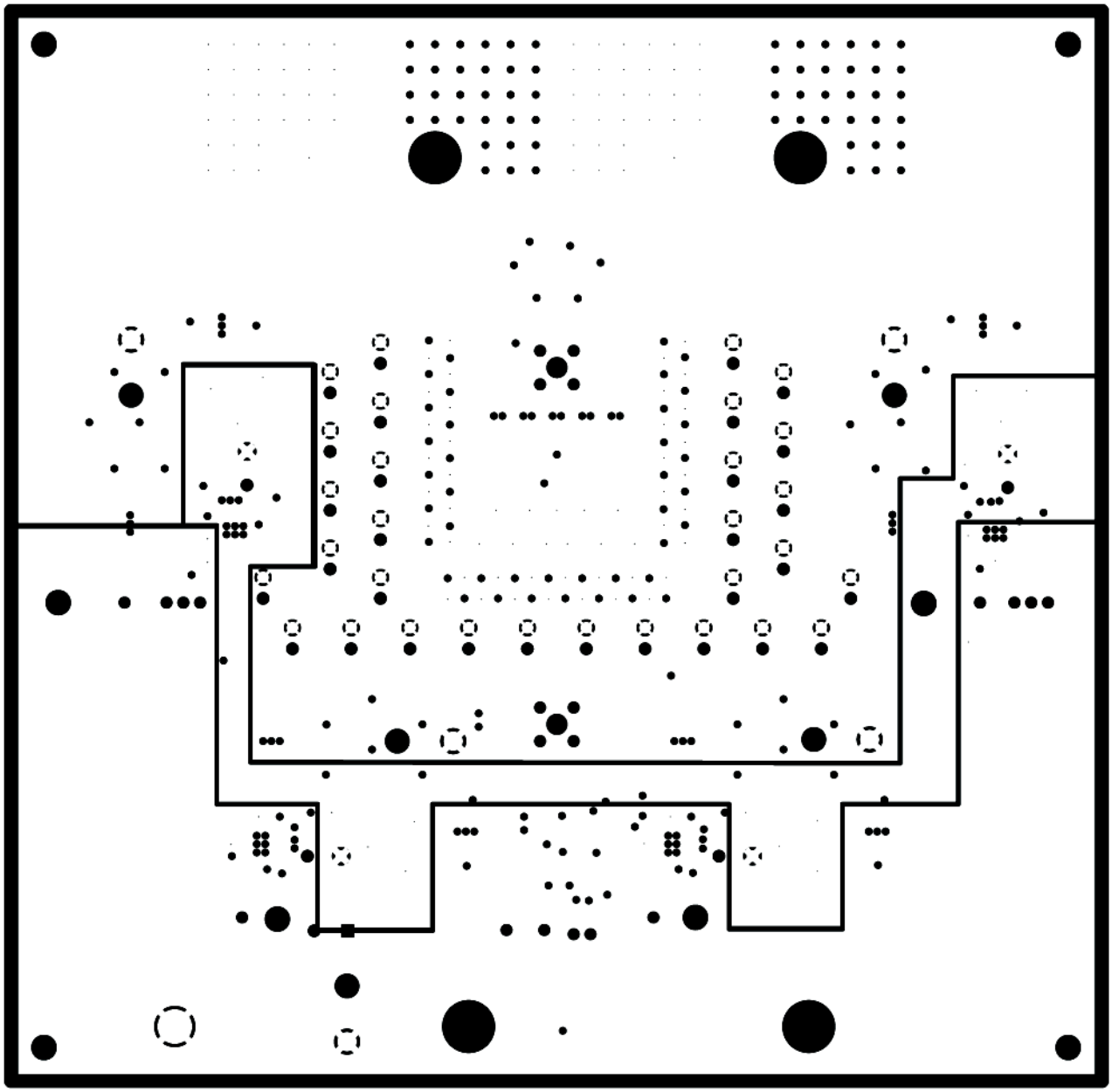


FIGURE 33. LAYER 3 POWER PLANE

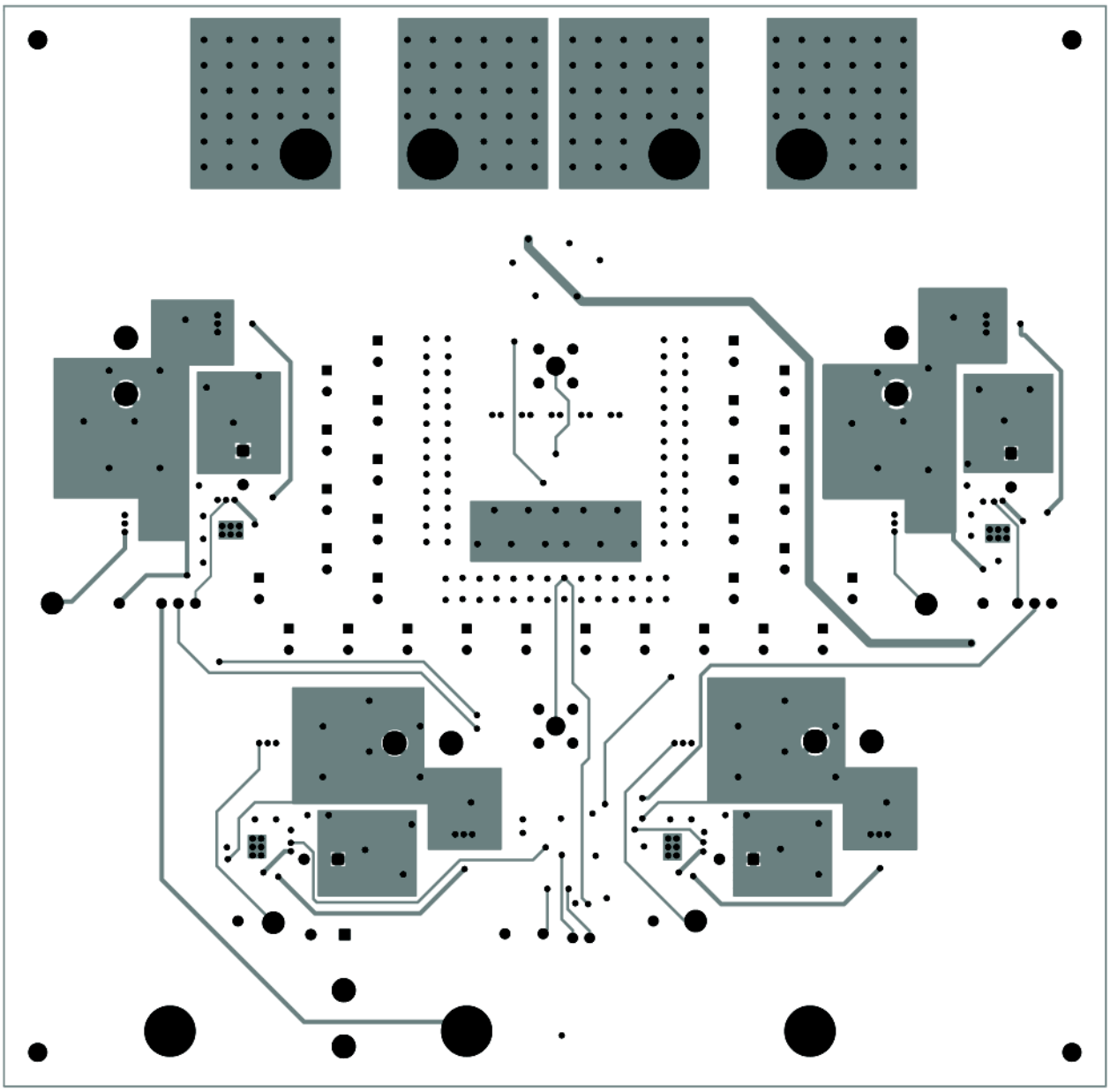


FIGURE 34. LAYER 4 BOTTOM COPPER