Si5318-EVB

EVALUATION BOARD FOR Si5318 SONET/SDH PRECISION CLOCK MULTIPLIER IC

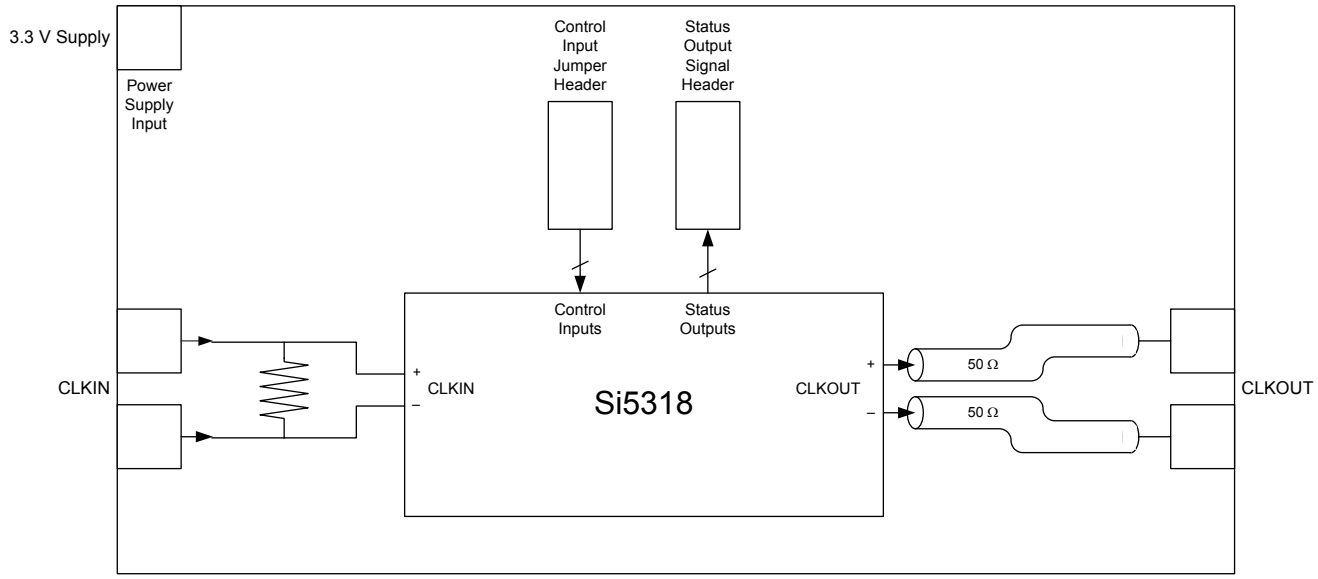
Description

The Si5318-EVB is the customer evaluation board for the Si5318 SONET/SDH Precision Port Card Clock IC. This board is supplied to customers for evaluation of the Si5318 device. The board provides access to signals associated with normal operation of the device.

Features

- Single supply at 3.3 V
- Differential I/Os ac coupled on board
- Differential inputs terminated on board
- Control input signals are switch configurable
- Status outputs brought out to headers for easy access.

Function Block Diagram



1. Functional Overview

The Si5318-EVB is the customer evaluation board for the Si5318 SONET/SDH Precision Port Card Clock IC. It is supplied to customers for evaluation of the Si5318 device. The board provides access to signals associated with normal operation of the device.

1.1. Power Consumption

Typical supply current draw for the Si5318-EVB is 140 mA.

1.2. Si5318 Control Inputs

The control inputs to the Si5318 are each routed from the center pin of a SPDT switch, JP5, to the Si5318 device. Additionally, the switches at JP5 are connected to GND on one side of the switch and to VDD33 on the other side. This arrangement allows easy configuration of each input to either a high or low state. To further reduce the coupling of noise into the device through these control inputs, the signals are routed on internal layers between ground planes.

1.3. RSTN/CAL Settings for Normal Operation and Self-Calibration

The RSTN/CAL signal is an LVTTL input to the Si5318 and has an on-chip pulldown mechanism. This pin must be set high for normal operation of the Si5318 device.

Setting RSTN/CAL low forces the Si5318 into the reset state. A low-to-high transition of RSTN/CAL enables the part and initiates a self-calibration sequence.

The Si5318 device initiates self-calibration at powerup if the RSTN/CAL signal is held high. A self-calibration of the device also can be manually initiated by momentarily pushing and then releasing the RSTN/CAL switch, SW1.

Manually initiate self-calibration after changing the state of the BWSEL[1:0].

Whether manually initiated or automatically initiated at powerup, the self-calibration process requires a valid input clock. If the self-calibration is initiated without a valid clock present, the device waits for a valid clock before completing the self-calibration. The Si5318 clock output is set to the lower end of the operating frequency range while the device waits for a valid clock. After the clock input is validated, the calibration process runs to completion, the device locks to the clock input, and the clock output shifts to its target frequency. Subsequent losses of the input clock signal do not require re-calibration. If the clock input is lost after self-calibration, the device enters Digital Hold mode. When the input clock returns, the device re-locks to the input clock without performing a self-calibration.

1.4. Status Signals

The status outputs from the Si5318 device are each routed to one pin of a two-row header. The signals are arranged so that each signal has a ground pin adjacent to the signal pin for reference. The row of signal pins is marked with an “S”, and the row of ground pins is marked with a “G”.

Visible indicators, D1 and D2, are added to the LOS and CAL_ACTV signals. The LEDs glow when the signal is active. The LOS LED D1 is illuminated when the device does not recognize a valid clock input. The CAL_ACTV LED, D2, is illuminated when the device is calibrating to an input clock.

1.5. Differential Clock Input Signals

The differential clock inputs to the Si5318-EVB board are ac coupled and terminated on the board at a location near the SMA input connectors, J1 and J2. The termination components are located on the top side of the board resistors. The termination circuit consists of two 50 Ω and a 0.1 µF capacitor, such that the positive and negative inputs of the differential pair each see a 50 Ω termination to “ac ground,” and the line-to-line termination impedance is 100 Ω.

For single-ended operation, supply a signal to one of the differential inputs (usually the positive input). The other input should be shorted to ground using an SMA shorting plug. The on-board termination circuit provides a 50 Ω termination to ac-ground for each leg of the differential pair.

1.6. Differential Clock Output Signals

The differential clock outputs from the Si5318 device are routed to the perimeter of the circuit board using 50 Ω transmission line structures. The capacitors that provide ac-coupling are located near the clock output SMA connectors, J4 and J5.

1.7. Internal Regulator Compensation

The Si5318-EVB contains pad locations for a resistor and a capacitor between the VDD25 node and ground. The resistor pads are populated with a 0 Ω resistor. The capacitor pads are populated with a low ESR 33 µF tantalum capacitor. This is the suggested compensation circuit for Si5318 devices.

The acceptable range for the time constant at this node is 15 µs to 50 µs. The capacitor used on the board is a 33 µF capacitor with an ESR of .8 Ω. This yields a time constant of 26.4 µs.

1.8. Default Jumper Settings

The default jumper settings for the Si5318-EVB board are given in Table 1.

Table 1. Si5318-EVB Assembly Rev. A Default Jumper/Switch Settings

Location	Signal	State	Notes
JP5	VALTIME	0	100 ms Validation Time
	BWSEL[0]	0	Loop Filter Bandwidth = 800 Hz
	BWSEL[1]	1	Loop Filter Bandwidth = 800 Hz
	INFRQSEL[0]	1	Clock IN = 19.44 MHz
	INFRQSEL[1]	0	Clock IN = 19.44 MHz
	INFRQSEL[2]	0	Clock IN = 19.44 MHz
	FRQSEL[0]	0	Clock Out = 155.52 MHz
	FRQSEL[1]	1	Clock Out = 155.52 MHz
	DBLBW	0	Selected bandwidth not doubled
	FXDDELAY	0	Fixed Delay disabled

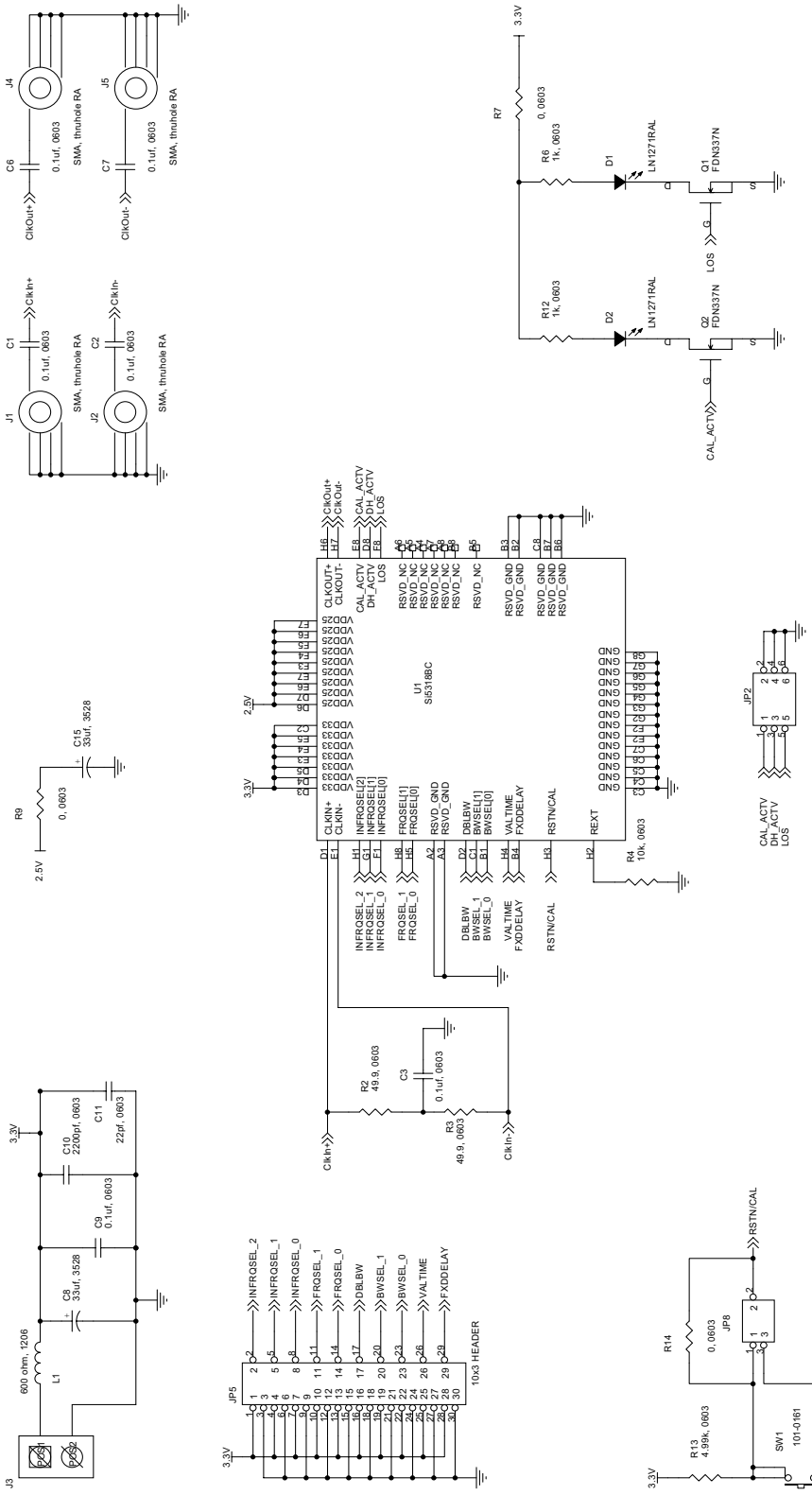
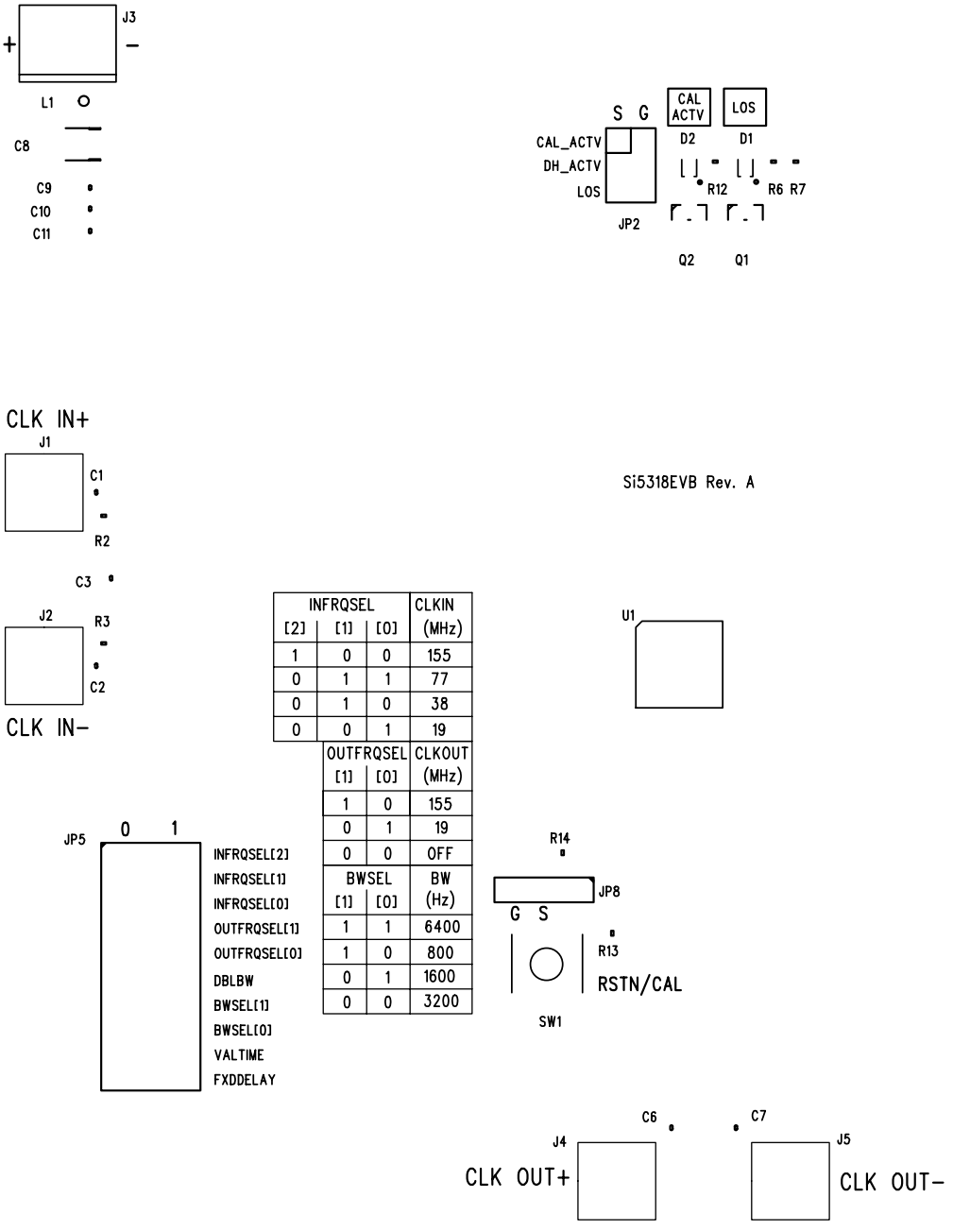


Figure 1. Si5318-EVB Schematic

2. Bill of Materials

Reference	Description	Manufacturer	Part Number
C1,C2,C3,C6,C7,C9	0.1 µf, 0603	Venkel	C0603X7R160-104KNE
C15,C8	33 µf, 3528	Venkel	TA6R3TCR336KBR
C10	2200pf, 0603	Venkel	C0603X7R160-222KNE
C11	22pf, 0603	Venkel	C0603C0G500-220KNE
D1, D2	LED, SM, red	Panasonic	LN1271RA2
JP8	1x3 HEADER		
JP2	HEADER 3x2		
JP5	10x3 HEADER		
J1,J2,J4,J5	SMA, thruhole RA	Johnson Components	142-0701-301
J3	power connector, 2 pin	Phoenix Contact	140-A-111-02 1729018
L1	600 Ω, 1206	Murata	BLM31A601S
Q1,Q2	MOS, SM, FDN337N	Fairchild	FDN337N
R13	4.99 kΩ, 0603	Venkel	CR0603-16W-4991FT
R2,R3	49.9 Ω, 0603	Venkel	CR0603-16W-49R9FT
R9, R14, R7	0, 0603	Venkel	CR0603-16W-000T
R4	10 kΩ, 0603	Venkel	CR0603-16W-1002FT
R6, R12	1 k, 0603	Venkel	CR0603-16W-1001FT
SW1	101-0161	Mouser	101-0161
U4	Si5318_revA	Silicon Laboratories	Si5318-A-BC



INFRQSEL [2]	[1]	[0]	CLKIN (MHz)
1	0	0	155
0	1	1	77
0	1	0	38
0	0	1	19

OUTFRQSEL [1]	[0]	CLKOUT (MHz)
1	0	155
0	1	19
0	0	OFF

BWSEL [1]	[0]	BW (Hz)
1	1	6400
1	0	800
0	1	1600
0	0	3200

Figure 2. Si5318-EVB Top Silkscreen

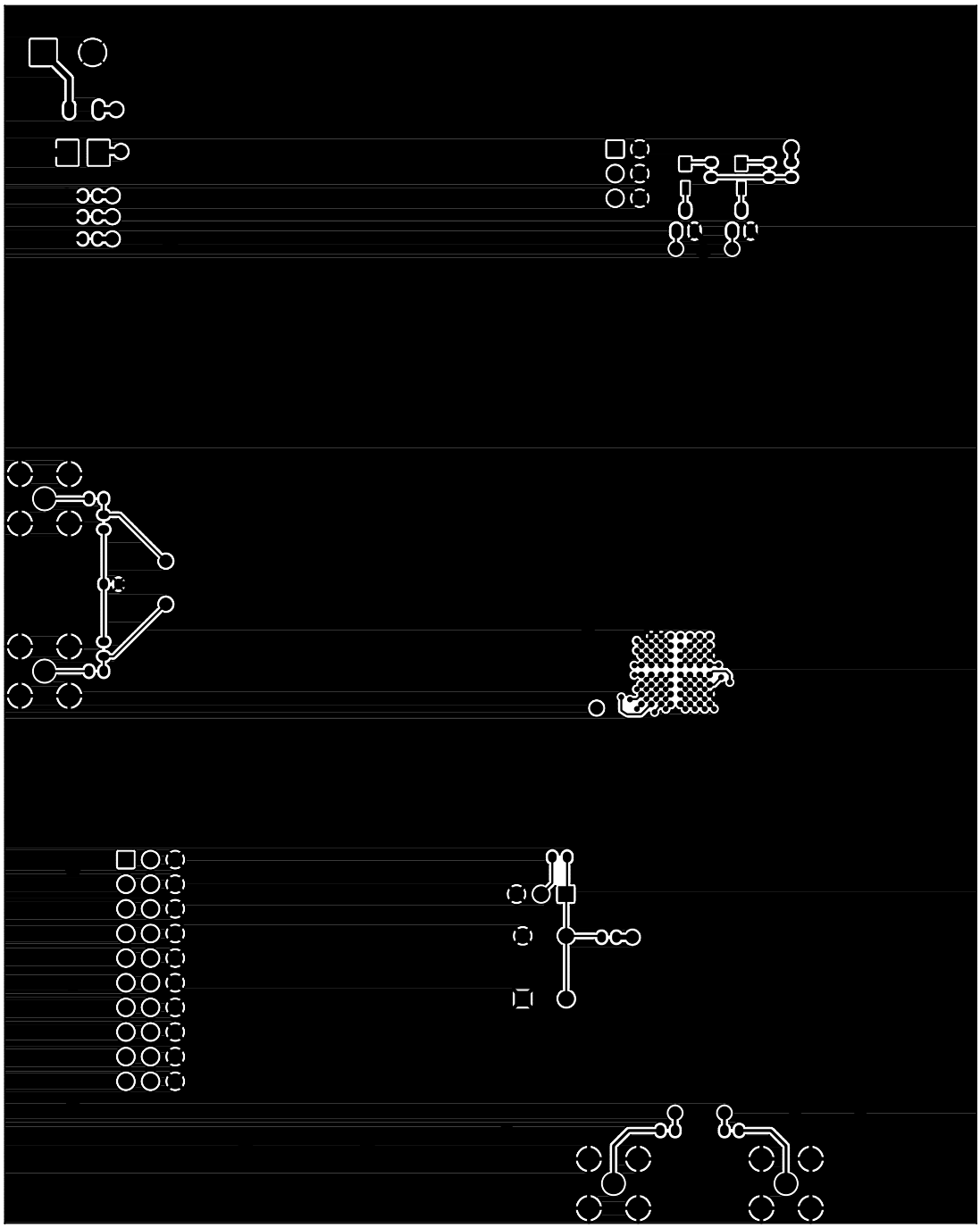


Figure 3. Si5318-EVB—Layer 1, Component Side

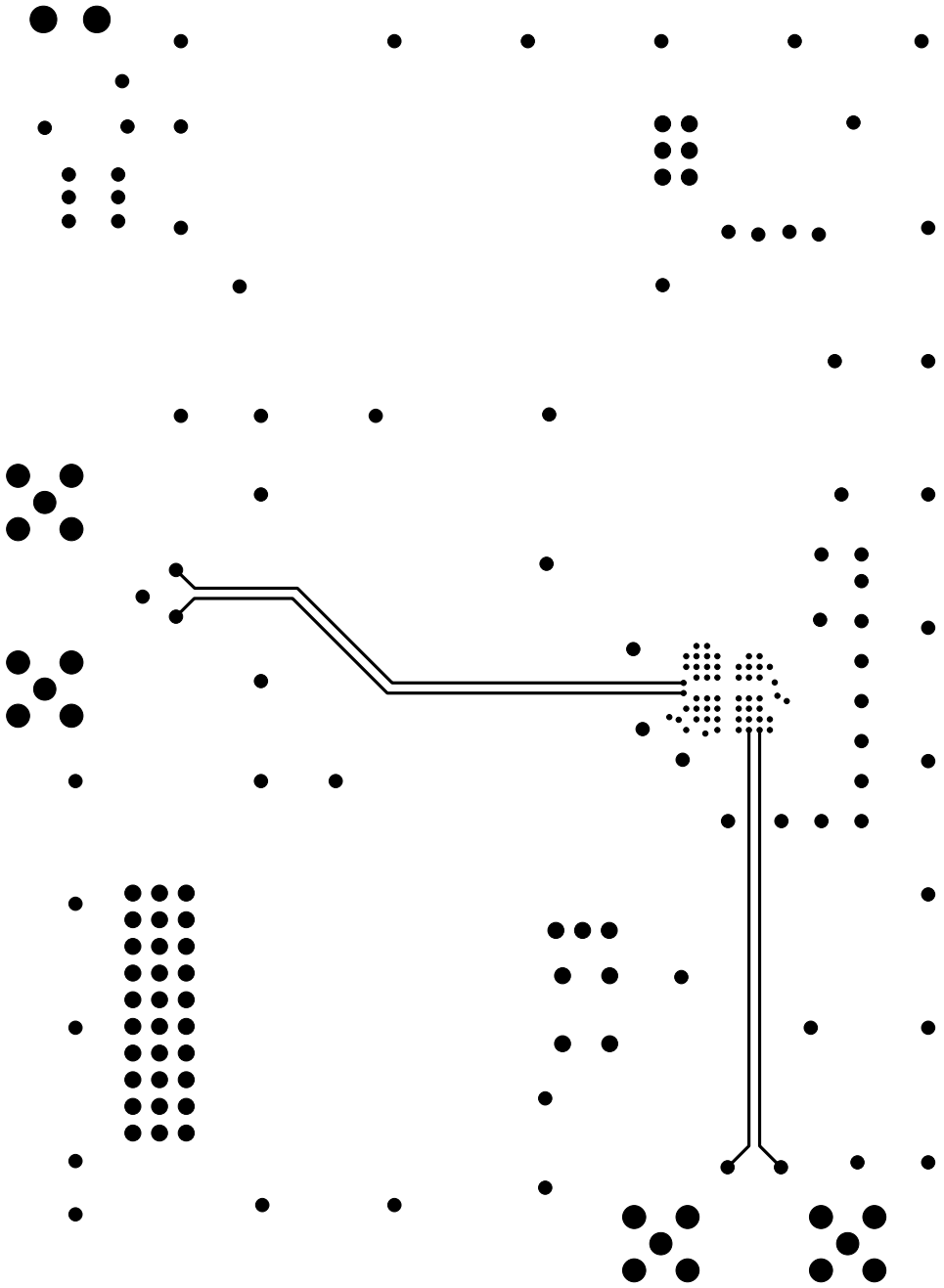


Figure 4. Si5318-EVB—Layer 2, High Speed Signals

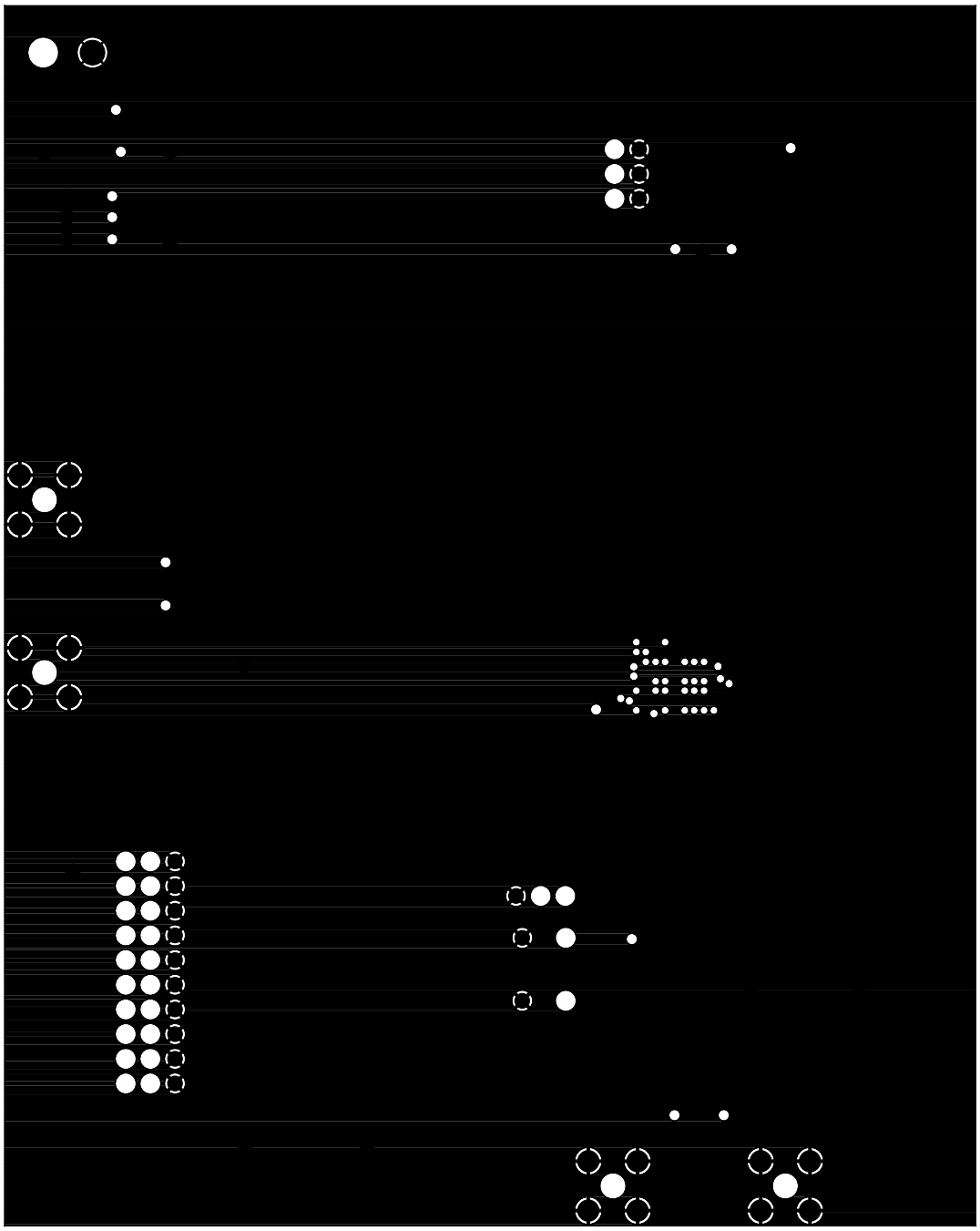


Figure 5. Si5318-EVB—Layer 3, GND

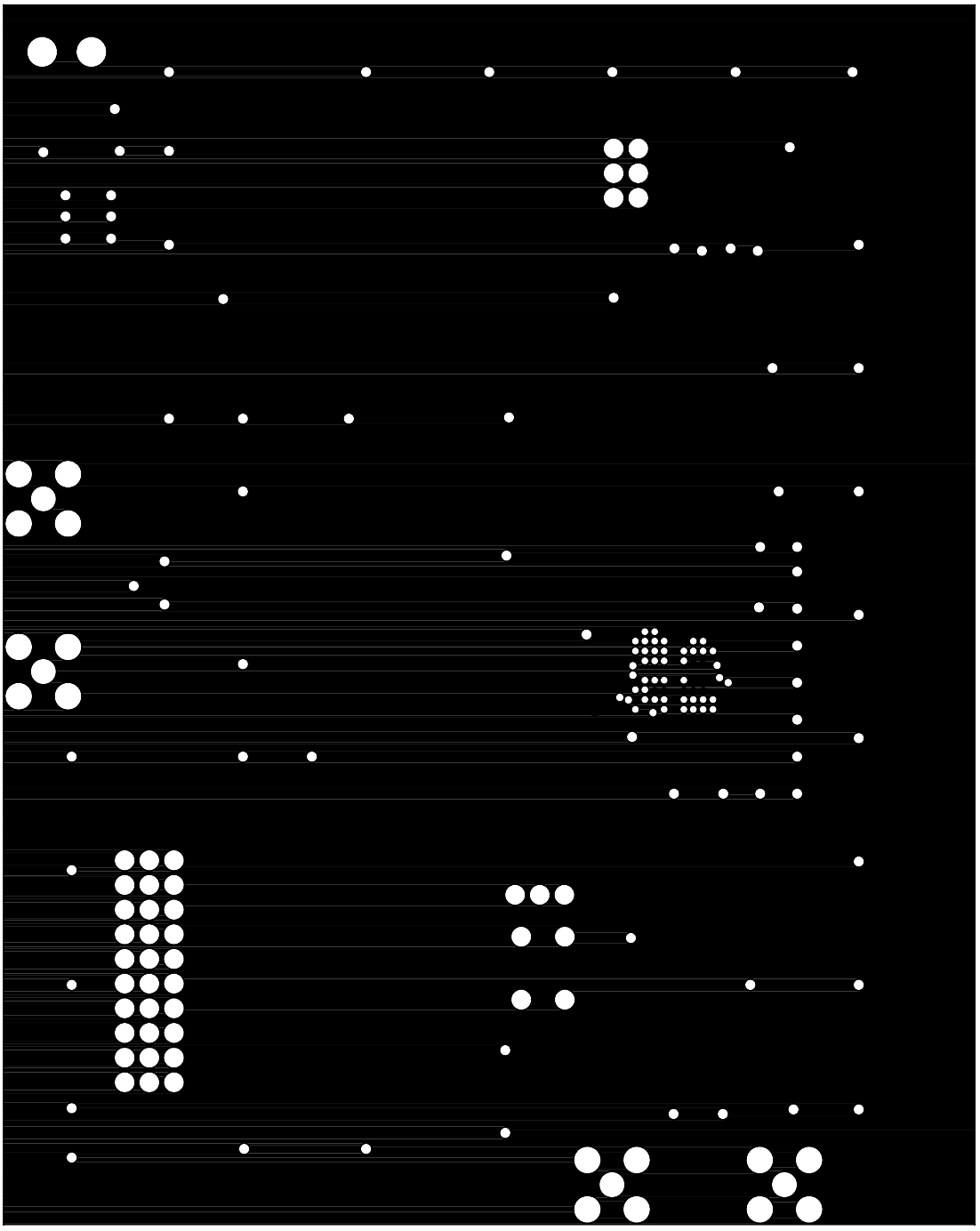


Figure 6. Si5318-EVB—Layer 4, VDD 2.5

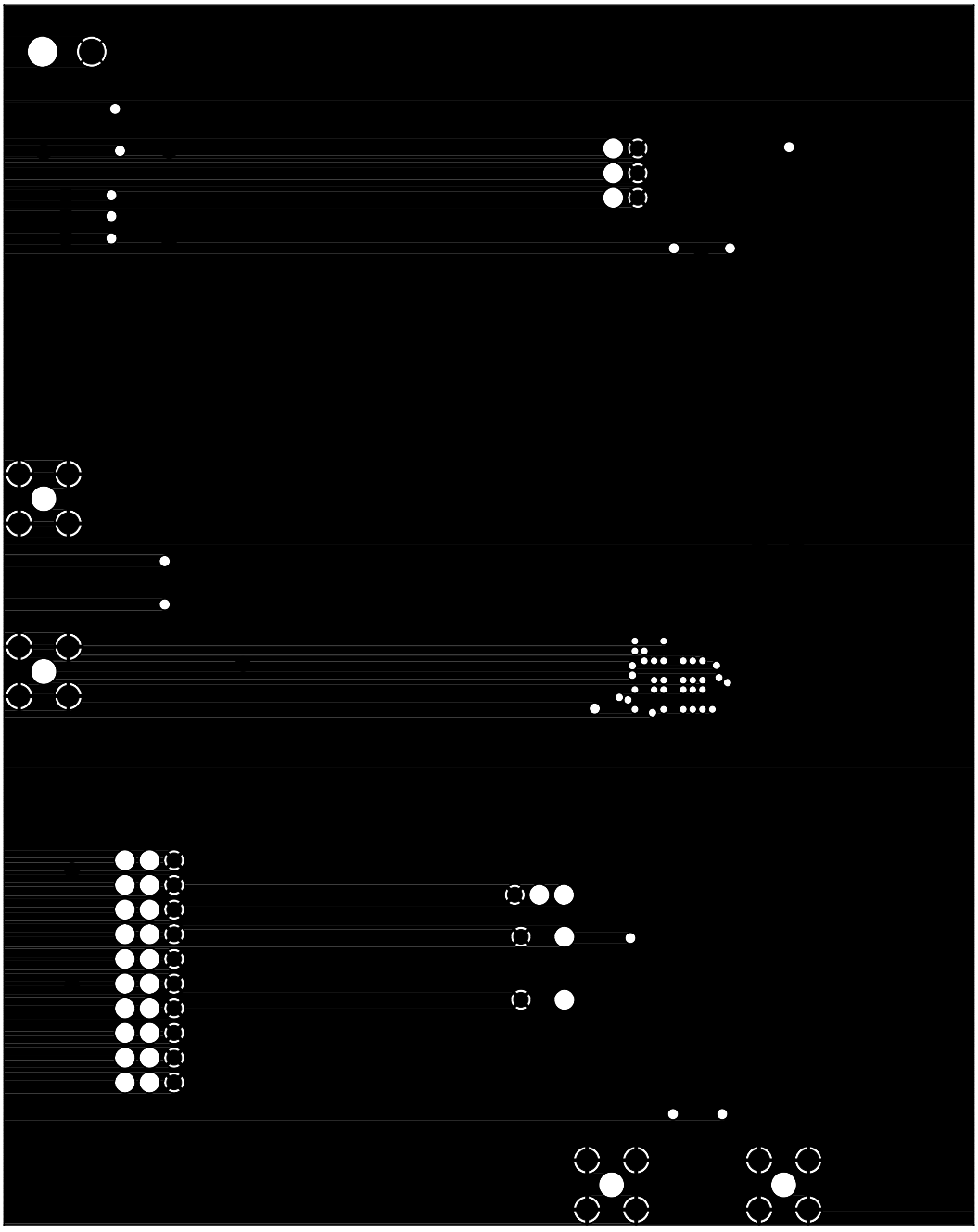


Figure 7. Si5318-EVB—Layer 5, GND

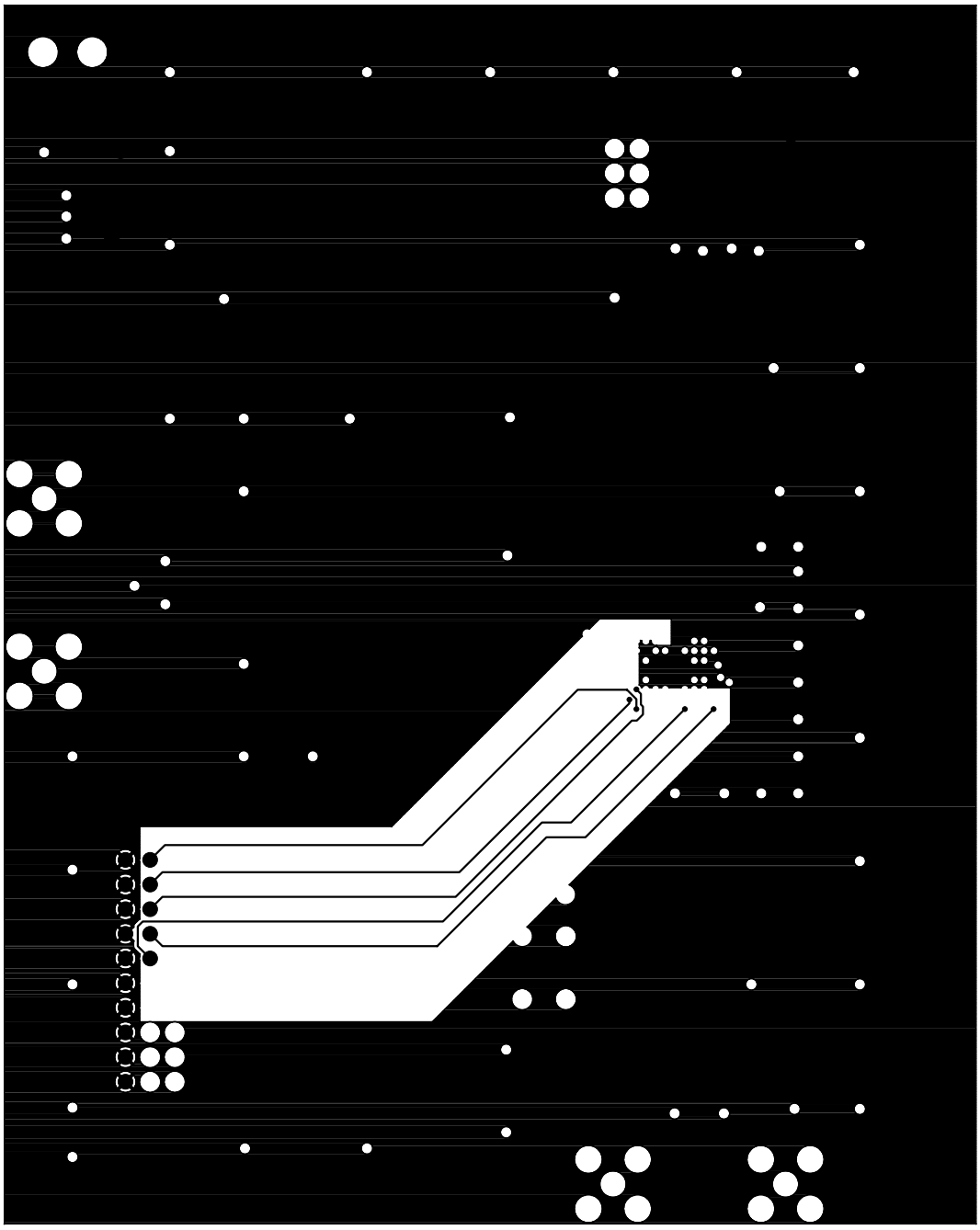


Figure 8. Si5318-EVB—Layer 6, VDD 3.3

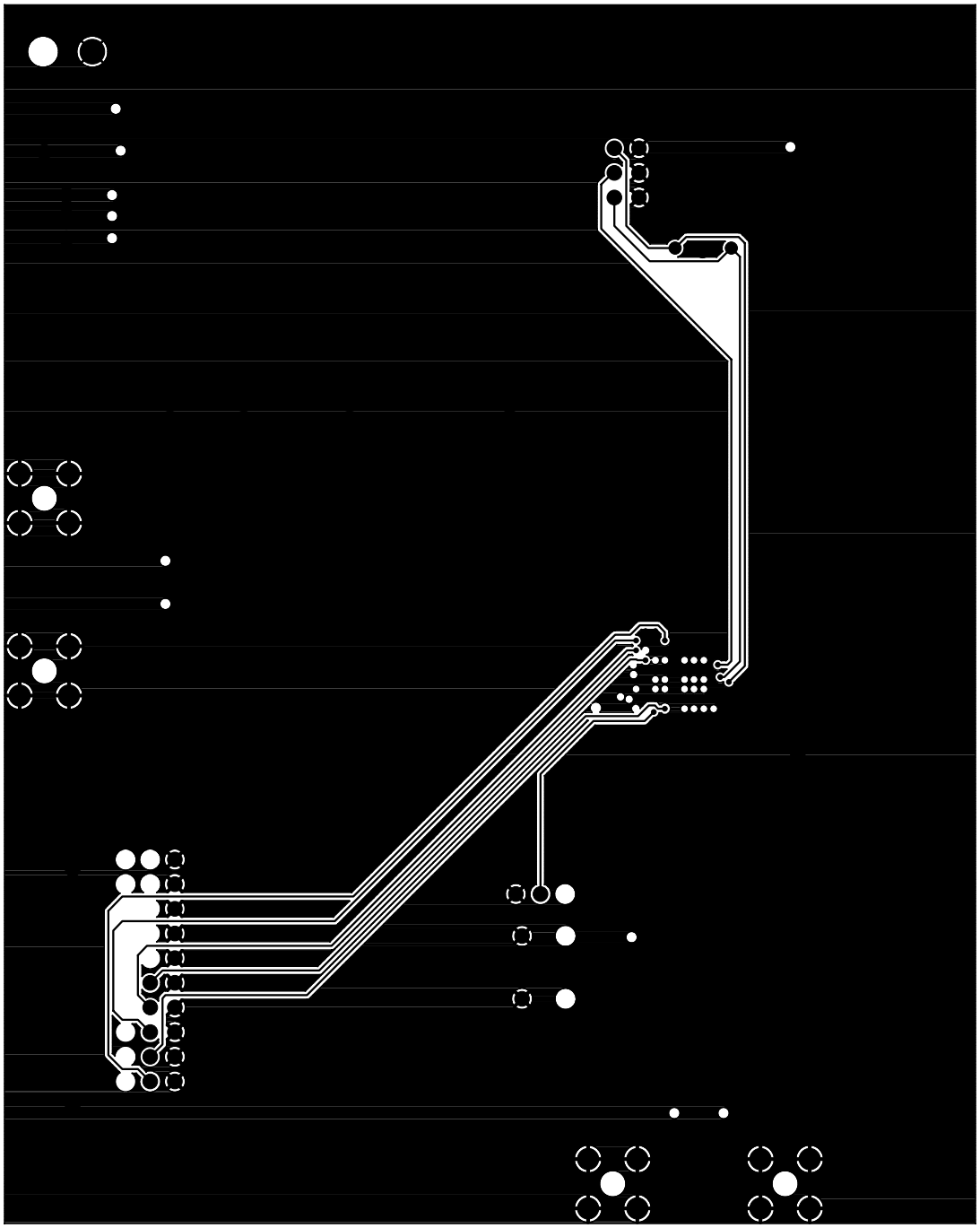


Figure 9. Si5318-EVB—Layer 7, GND

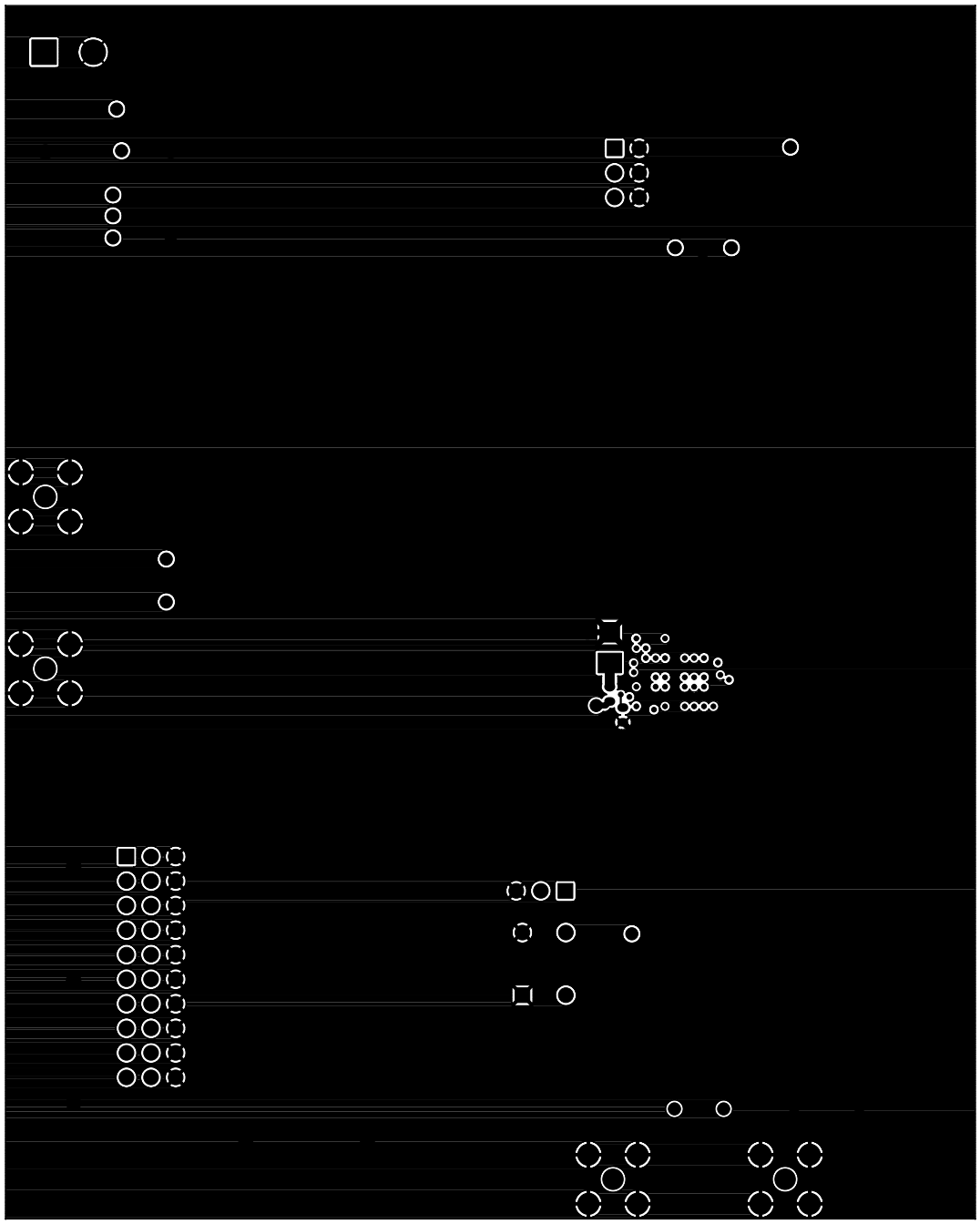


Figure 10. Si5318-EVB—Layer 8, Bottom

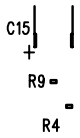


Figure 11. Si5318-EVB Bottom Silkscreen

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