



## EVALUATION BOARD FOR THE Si5321 SONET/SDH PRECISION CLOCK MULTIPLIER IC

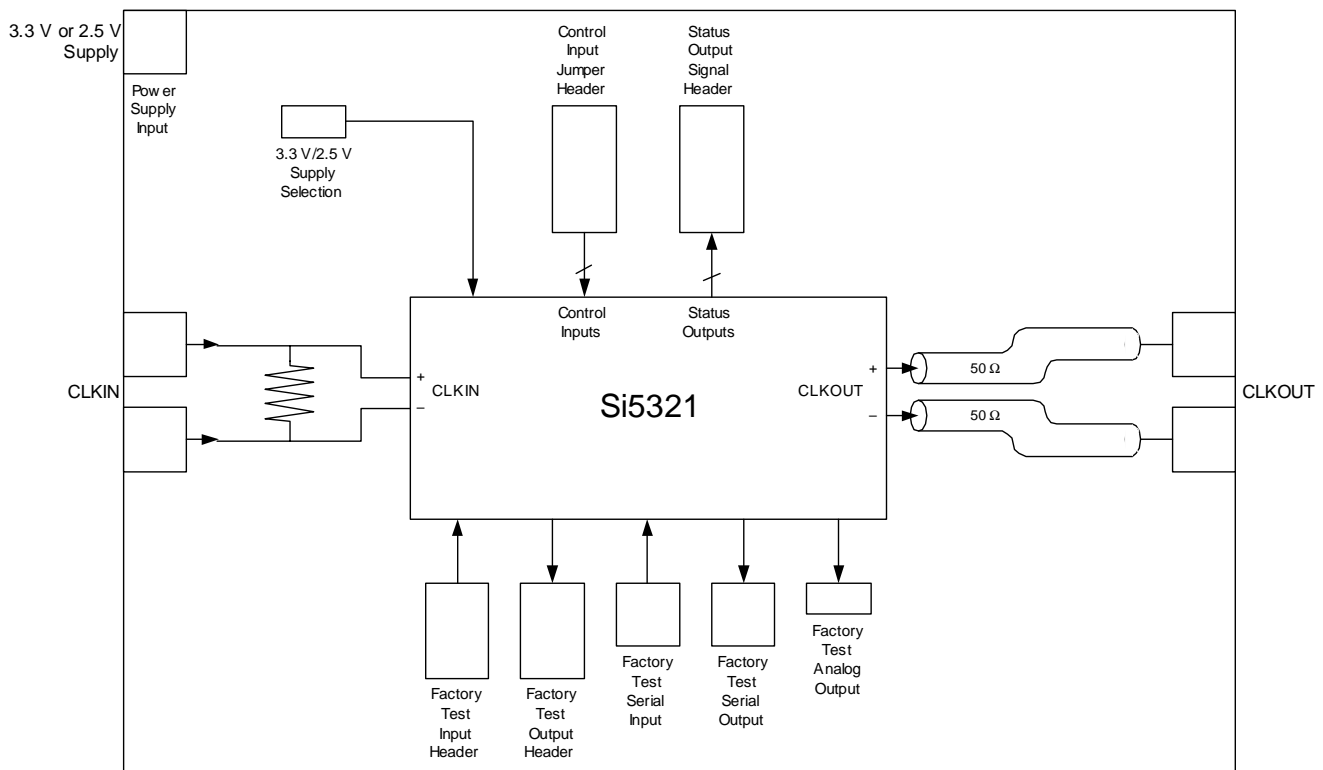
### Description

The Si5321-EVB is the customer evaluation board for the Si5321 SONET/SDH Precision Port Card Clock IC. This board is supplied to customers for evaluation of the Si5321 device. The board provides access to signals associated with normal operation of the device and signals that are reserved for factory testing purposes.

### Features

- Single supply at either 3.3 or 2.5 V (jumper configurable)
- Differential I/Os ac coupled on board
- Differential inputs terminated on board
- Control input signals are switch configurable
- Status outputs brought out to headers for easy access.

### Function Block Diagram



## Functional Overview

The Si5321-EVB is the customer evaluation board for the Si5321 SONET/SDH Precision Port Card Clock IC. It is supplied to customers for evaluation of the Si5321 device. The board provides access to signals associated with normal operation of the device and signals that are reserved for factory testing purposes.

## Power Supply Selection and Connections

The Si5321-EVB board is switch selectable for operation using either a single 3.3 V or a single 2.5 V supply.

For operation using a 3.3 V supply, configure the board as follows:

1. Remove power supply connections from the VDD and GND terminals of the board's power connector, J3.
2. Remove the connection between VDD33 and VDD25 by removing the jumper on header JPI.
3. Set VSEL33 high by sliding the switch on the VSEL33 (JP6) to the side marked "1".
4. Connect the power supply ground lead and 3.3 V supply lead to the GND and VDD terminals of the board's power connector, J3.

For operation using a 2.5 V supply, configure the board as follows:

1. Remove power supply connections from the VDD and GND terminals of the board's power connector, J3.
2. Set VSEL33 low by sliding the switch on the VSEL33 (JP6) to the side marked "0".
3. Connect VDD33 and VDD25 by installing a jumper between one of the 3.3 V pins and one of the 2.5 V pins on header JPI.
4. Connect the power supply ground lead and 2.5 V supply lead to the GND and VDD terminals of the board's power connector, J3.

## Power Consumption

Typical supply current draw for the Si5321-EVB is 110 mA.

## Si5321 Control Inputs

The control inputs to the Si5321 are each routed from the center pin of a SPDT switch, JP5, to the Si5321 device. Additionally, the switches at JP5 are connected to GND on one side of the switch and to VDD33 on the other side. This arrangement allows easy configuration of each input to either a high or low state. To further reduce the coupling of noise into the device through these control inputs, the signals are routed on internal layers between ground planes.

## RSTN/CAL Settings for Normal Operation and Self-Calibration

The RSTN/CAL signal is an LVTTTL input to the Si5321 and has an on-chip pulldown mechanism. This pin must be set high for normal operation of the Si5321 device.

Setting RSTN/CAL low forces the Si5321 into the reset state. A low-to-high transition of RSTN/CAL enables the part and initiates a self-calibration sequence.

The Si5321 device initiates self-calibration at powerup if the RSTN/CAL signal is held high. A self-calibration of the device also can be manually initiated by momentarily pushing the RSTN/CAL switch, SWI and then releasing.

Manually initiate self-calibration after changing the state of either the BWSEL[1:0] control inputs or the FEC[1:0] inputs.

Whether manually initiated or automatically initiated at powerup, the self-calibration process requires a valid input clock. If the self-calibration is initiated without a valid clock present, the device waits for a valid clock before completing the self-calibration. The Si5321 clock output is set to the lower end of the operating frequency range while the device waits for a valid clock. After the clock input is validated, the calibration process runs to completion, the device locks to the clock input, and the clock output shifts to its target frequency. Subsequent losses of the input clock signal do not require re-calibration. If the clock input is lost after self-calibration, the device enters Digital Hold mode. When the input clock returns, the device re-locks to the input clock without performing a self-calibration.

## Status Signals

The status outputs from the Si5321 device are each routed to one pin of a two-row header. The signals are arranged so that each signal has a ground pin adjacent to the signal pin for reference. The row of signal pins is marked with an "S", and the row of ground pins is marked with a "G".

Visible indicators are added to the LOS and CAL\_ACTV signals. The LEDs glow when the signal is active and the LED enable switch is set to ON. The LOS LED is illuminated when the device does not recognize a valid clock input. The CAL\_ACTV LED is illuminated when the device is calibrating to an input clock.

## Differential Clock Input Signals

The differential Clock inputs to the Si5321-EVB board are ac coupled and terminated on the board at a location near the SMA input connectors. The termination components are located on the top side of the board. The termination circuit consists of two 50  $\Omega$

and a 0.1  $\mu\text{F}$  capacitor, such that the positive and negative inputs of the differential pair each see a 50  $\Omega$  termination to “ac ground,” and the line-to-line termination impedance is 100  $\Omega$ .

For single-ended operation, supply a signal to one of the differential inputs (usually the positive input). The other input should be shorted to ground using an SMA shorting plug. The on-board termination circuit provides a 50  $\Omega$  termination to ac-ground for each leg of the differential pair.

### Differential Clock Output Signals

The differential clock outputs from the Si5321 device are routed to the perimeter of the circuit board using 50  $\Omega$  transmission line structures. The capacitors that provide ac-coupling are located near the clock output SMA connectors.

### Internal Regulator Compensation

The Si5321-EVB contains pad locations for a resistor and a capacitor between the VDD25 node and ground. The resistor pads are populated with a 0  $\Omega$  resistor. The capacitor pads are populated with a low ESR 33  $\mu\text{F}$  tantalum capacitor. This is the suggested compensation circuit for Si5321 devices.

There are two considerations for selecting this combination of compensation resistor and capacitor. First, is the stability of the regulator. The second is noise filtering.

The acceptable range for the time constant at this node is 15  $\mu\text{s}$  to 50  $\mu\text{s}$ . The capacitor used on the board is a 33  $\mu\text{F}$  capacitor with an ESR of .8  $\Omega$ . This yields a time constant of 26.4  $\mu\text{s}$ . The designer could decide to use a 330  $\mu\text{F}$  capacitor with an ESR of .15  $\Omega$ . This yields a time constant of 49.5  $\mu\text{s}$ . Each of these cases provide a compensation circuit that makes the output of the regulator stable.

The second issue is noise filtering. For this, more capacitance is usually better. For the two cases described above, the 330  $\mu\text{F}$  case provides greater noise filtering. However, the large case size of the 330  $\mu\text{F}$  capacitor might make it impractical for many applications. The Si5321 device is specified with the 33  $\mu\text{F}$  cap.

### Default Jumper Settings

The default jumper settings for the Si5321-EVB board are given in Table 1. These settings configure the board for operation from a 3.3 V supply.

**Table 1. Si5321-EVB Assembly Rev B-01 Default Jumper/Switch Settings**

| Location | Signal      | State                | Notes                                    |
|----------|-------------|----------------------|------------------------------------------|
| JP6      | VSEL33      | 1                    | Internal Regulator enabled               |
| JP1      | VDD33       | Open                 | 3.3 V plane not connected to 2.5 V plane |
| JP5      | VALTIME     | 0                    | 100 ms Validation Time                   |
|          | FEC[0]      | 0                    | No FEC scaling                           |
|          | FEC[1]      | 0                    | No FEC scaling                           |
|          | FEC[2]      | 0                    | No FEC scaling                           |
|          | BWSEL[0]    | 0                    | Loop Filter Bandwidth = 800 Hz           |
|          | BWSEL[1]    | 1                    | Loop Filter Bandwidth = 800 Hz           |
|          | INFRQSEL[0] | 1                    | Clock IN = 19.44 MHz                     |
|          | INFRQSEL[1] | 0                    | Clock IN = 19.44 MHz                     |
|          | INFRQSEL[2] | 0                    | Clock IN = 19.44 MHz                     |
|          | FRQSEL[0]   | 1                    | Clock Out = 622.08 MHz                   |
|          | FRQSEL[1]   | 1                    | Clock Out = 622.08 MHz                   |
|          | FRQSEL[2]   | 0                    | Clock Out = 622.08 MHz                   |
|          | BWBOOST     | 1                    | Selected bandwidth not doubled           |
| FXDDELAY | 0           | Fixed Delay disabled |                                          |
| JP7      | LED ENABLE  | On                   | LED Indicators enabled                   |



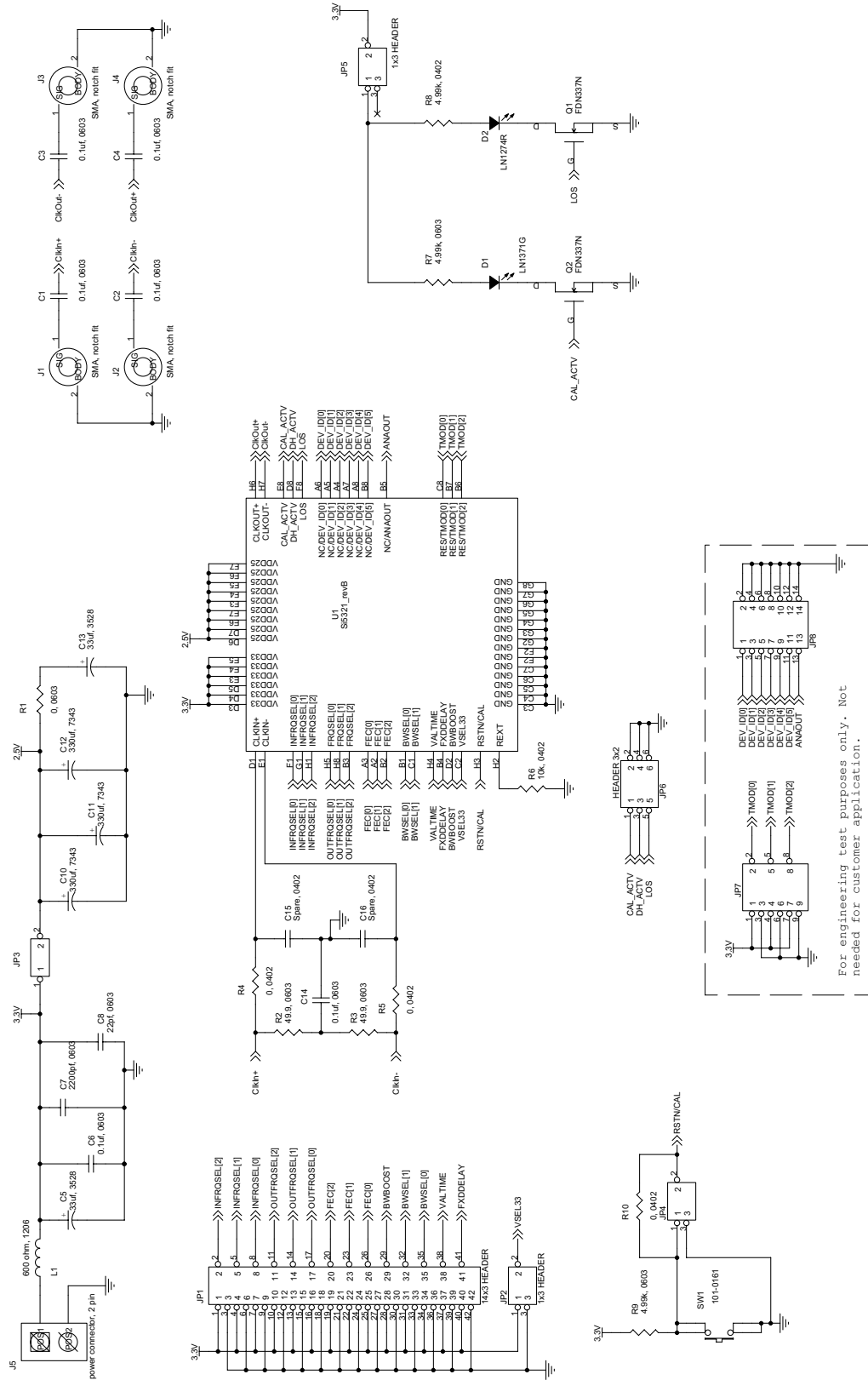


Figure 1. Si5321-EVB Schematic

For engineering test purposes only. Not needed for customer application.

## Bill of Materials

| Reference          | Description            | Manufacturer         | Part Number          |
|--------------------|------------------------|----------------------|----------------------|
|                    |                        |                      |                      |
| C1,C2,C3,C4,C6,C14 | 0.1uf, 0603            | Venkel               | C0603X7R160-104KNE   |
| C5,C13             | 33uf, 3528             | Venkel               | TA6R3TCR336KBR       |
| C7                 | 2200pf, 0603           | Venkel               | C0603X7R160-222KNE   |
| C8                 | 22pf, 0603             | Venkel               | C0603C0G500-220KNE   |
| C10,C11,C12        | 330uf, 7343            | Venkel               | TA6R3TCR337KER       |
| C15,C16            | Spare, 0402            |                      |                      |
| D1                 | LED, SM, green         | Panasonic            | LN1371G              |
| D2                 | LED, SM, red           | Panasonic            | LN1274R              |
| JP1                | 14x3 HEADER            |                      |                      |
| JP2,JP4,JP5        | 1x3 HEADER             |                      |                      |
| JP3                | 1x2 HEADER             |                      |                      |
| JP6                | HEADER 3x2             |                      |                      |
| JP7                | 5x3                    |                      |                      |
| JP8                | 7x2 Header             |                      |                      |
| J1,J2,J3,J4        | SMA, notch fit         | Johnson Components   | 82 SMA-S50-0-45      |
| J5                 | power connector, 2 pin | Phoenix Contact      | 140-A-111-02 1729018 |
| L1                 | 600 ohm, 1206          | MURATA               | BLM31A601S           |
| Q1,Q2              | MOS, SM, FDN337N       | Fairchild            | FDN337N              |
| R1                 | 0, 0603                | Venkel               | CR0603-16W-000T      |
| R3,R2              | 49.9, 0603             | Venkel               | CR0603-16W-49R9FT    |
| R4,R5,R10          | 0, 0402                | Venkel               | CR0402-16W-000T      |
| R6                 | 10k, 0402              | Venkel               | CR0402-16W-1002FT    |
| R7,R8              | 60.4, 0402             | Venkel               | CR0402-16W-60R4FT    |
| R9                 | 4.99k, 0603            | Venkel               | CR0603-16W-4991FT    |
| SW1                | 101-0161               | Mouser               | 101-0161             |
| U1                 | Si5321_revB            | Silicon Laboratories | Si5321-BC            |



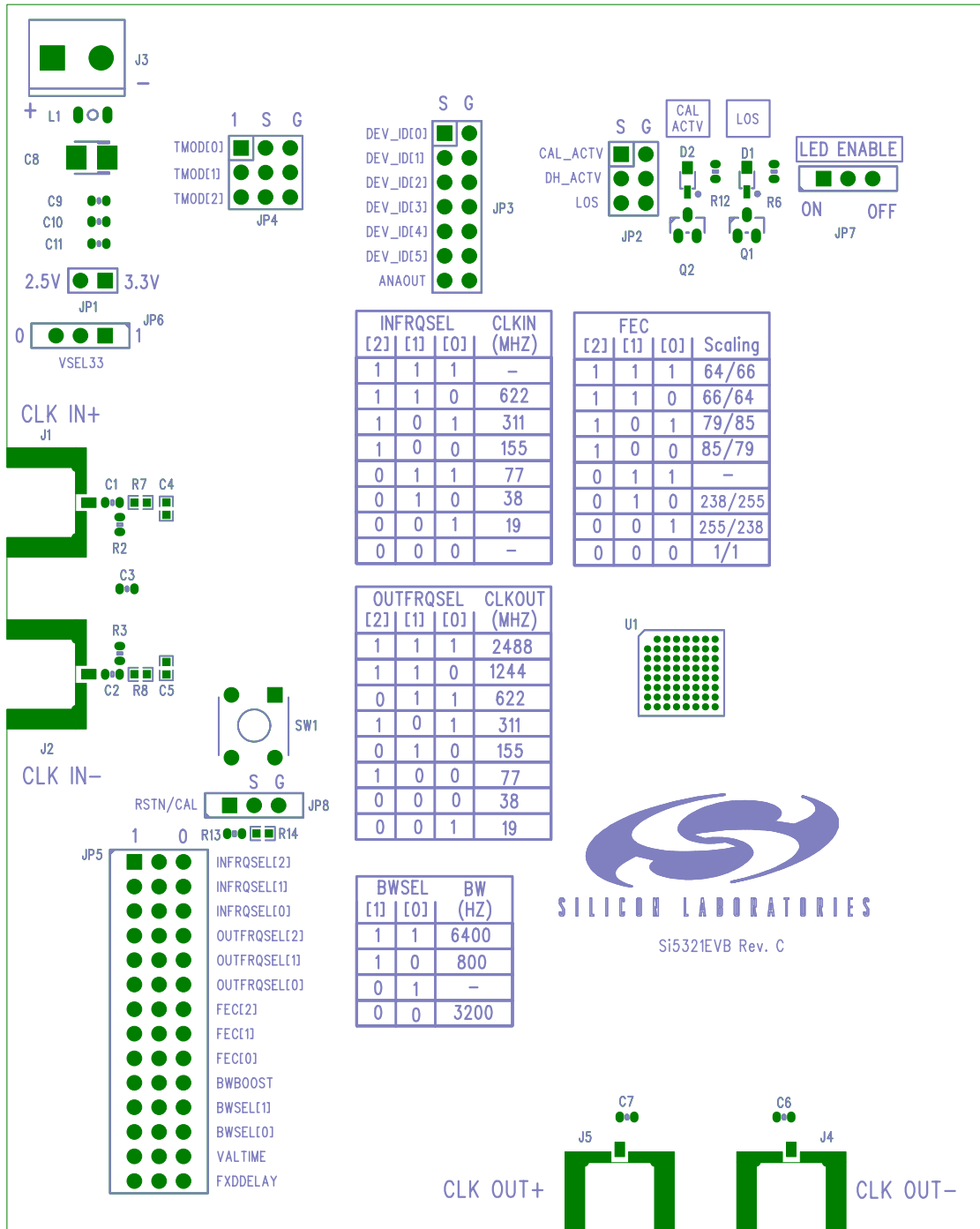


Figure 2. Si5321-EVB Top Silkscreen

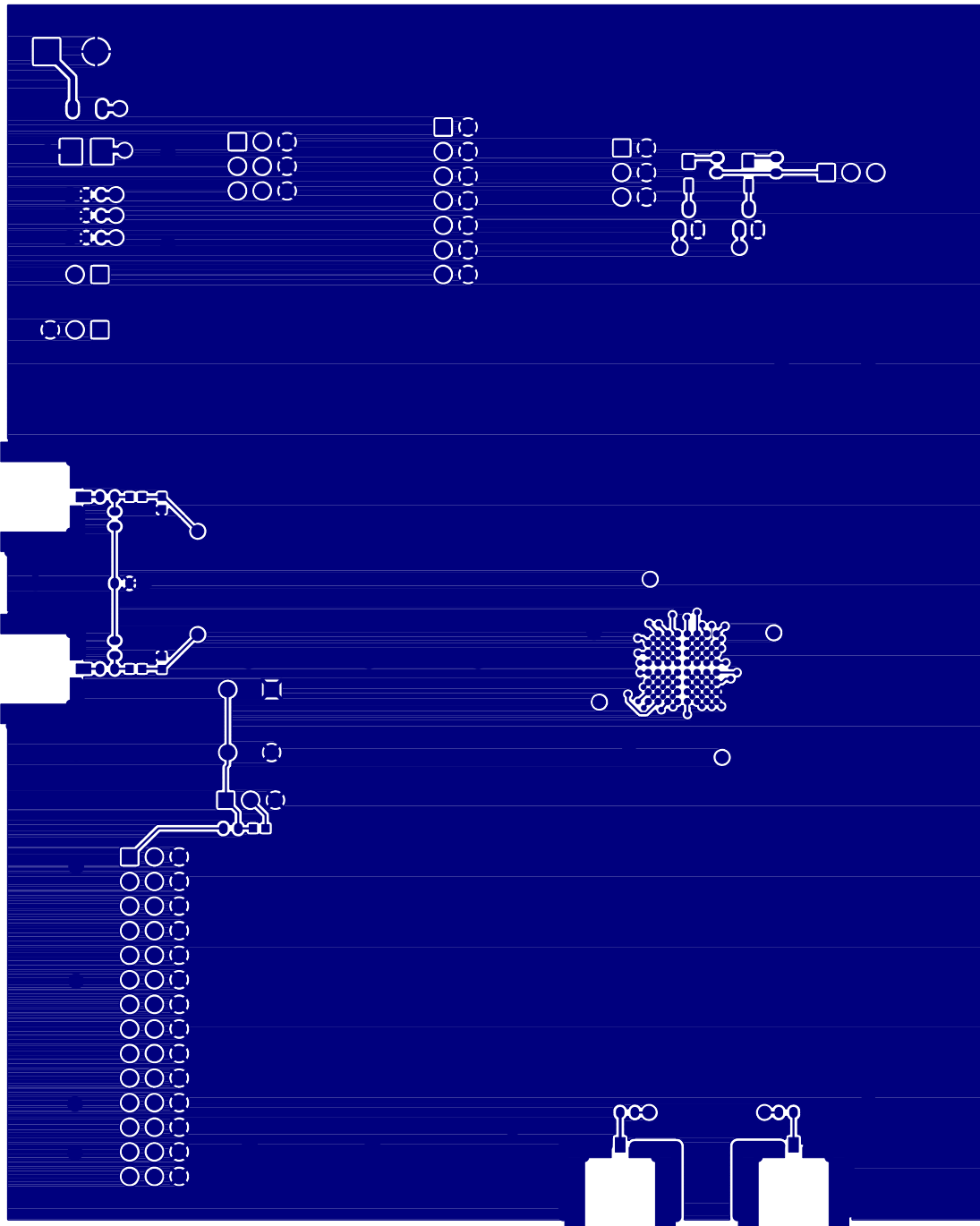


Figure 3. Si5321-EVB—Layer 1, Component Side



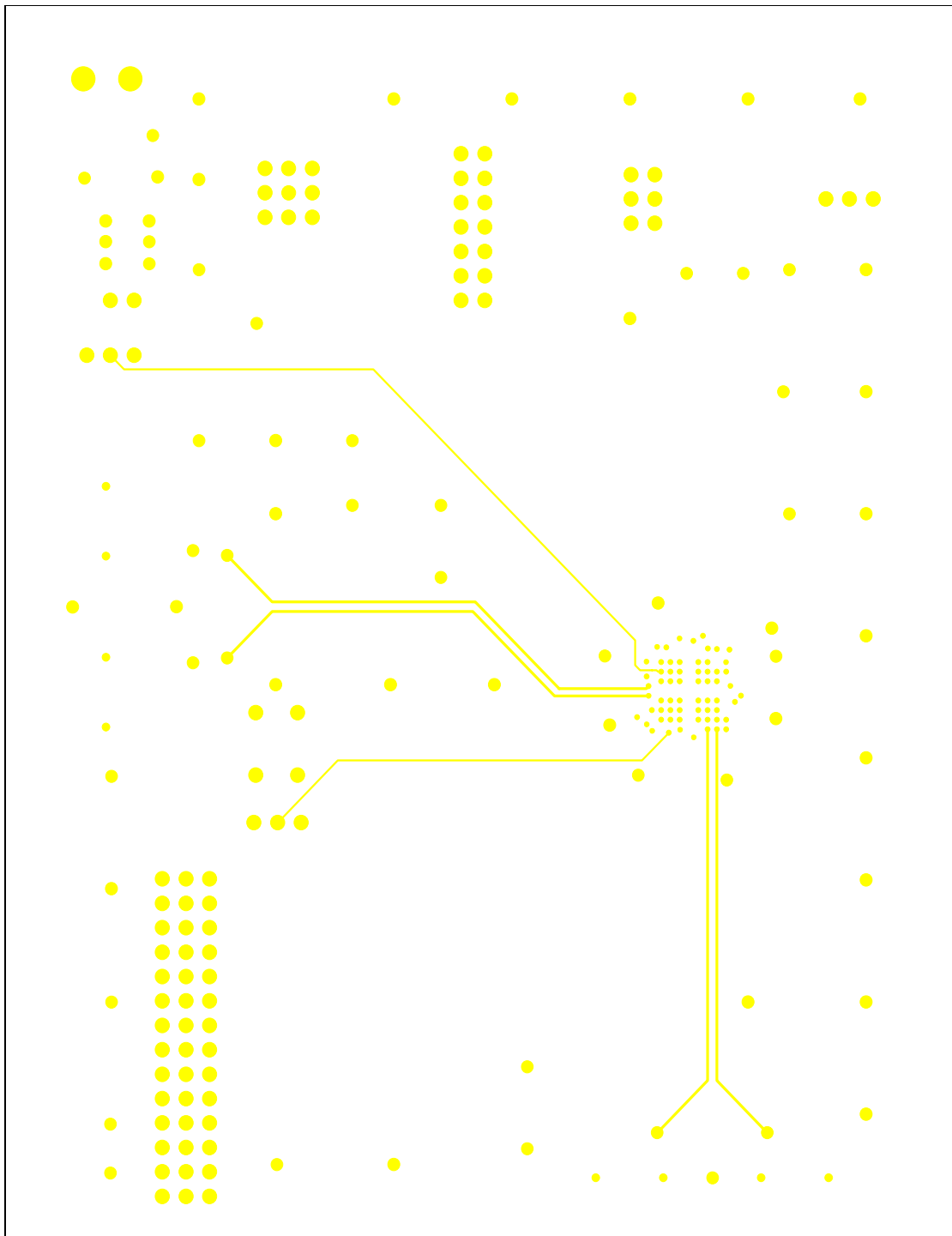


Figure 4. Si5321-EVB—Layer 2, High Speed Signals



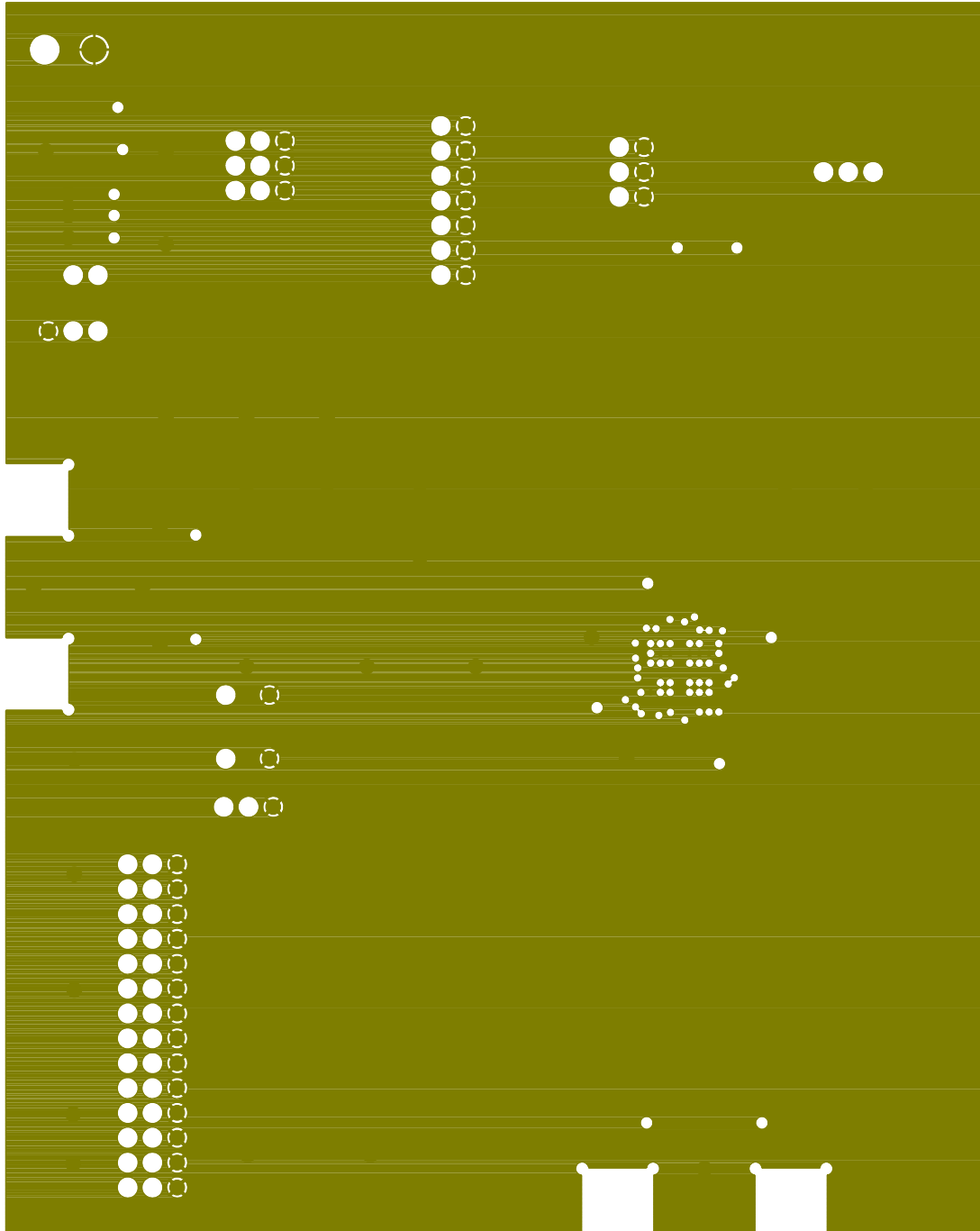


Figure 5. Si5321-EVB—Layer 3, GND



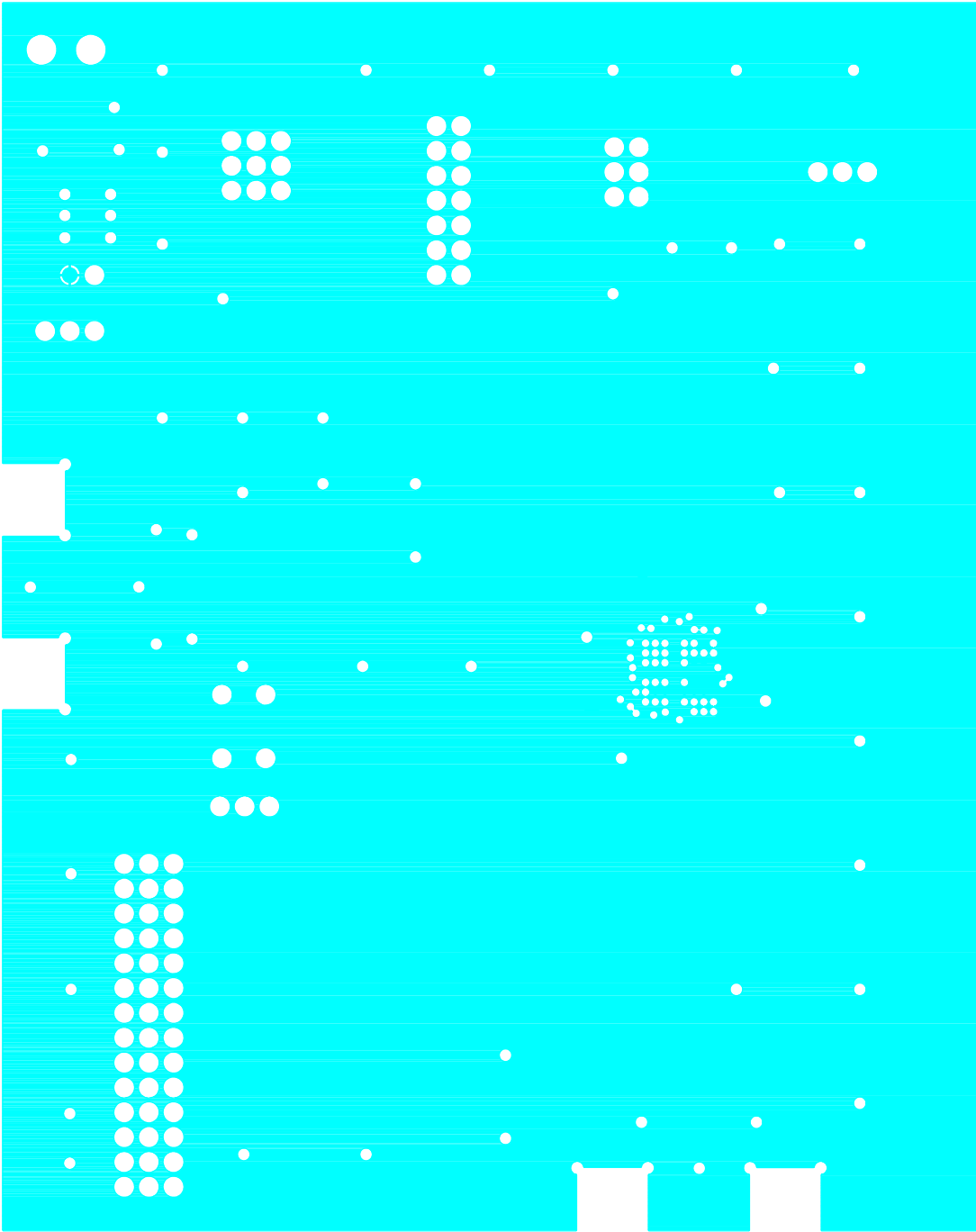


Figure 6. Si5321-EVB—Layer 4, VDD 2.5

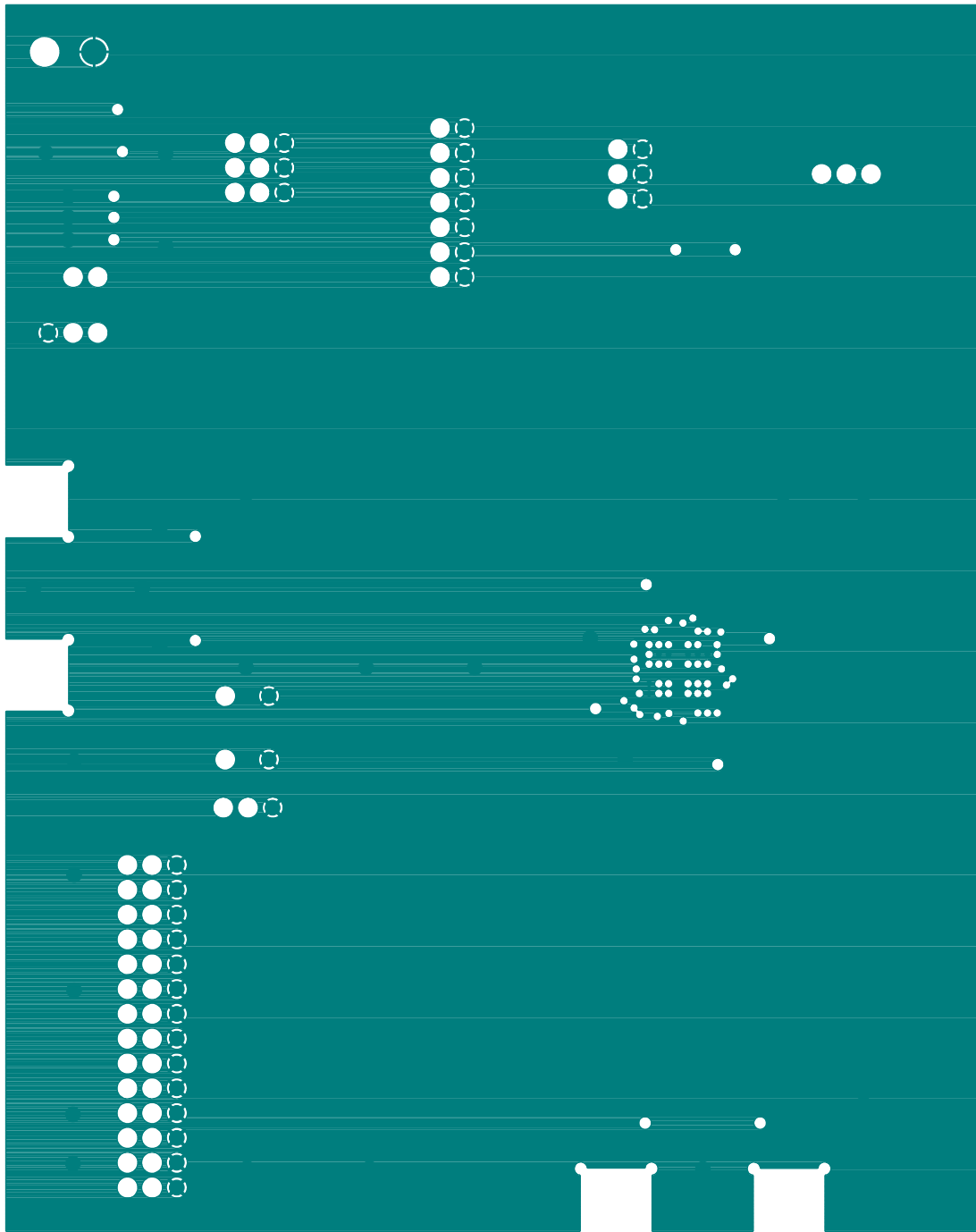


Figure 7. Si5321-EVB—Layer 5, GND



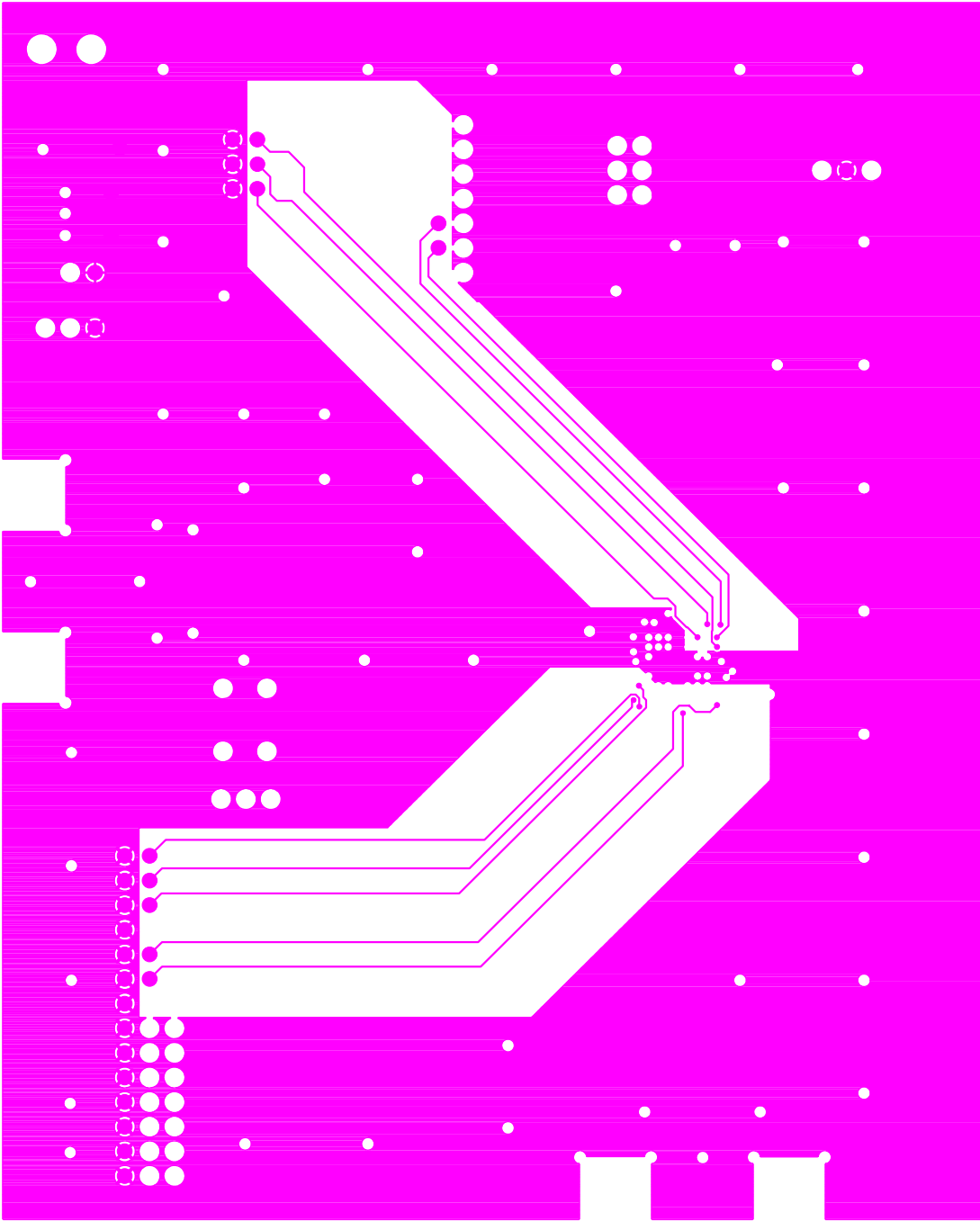


Figure 8. Si5321-EVB—Layer 6, VDD 3.3

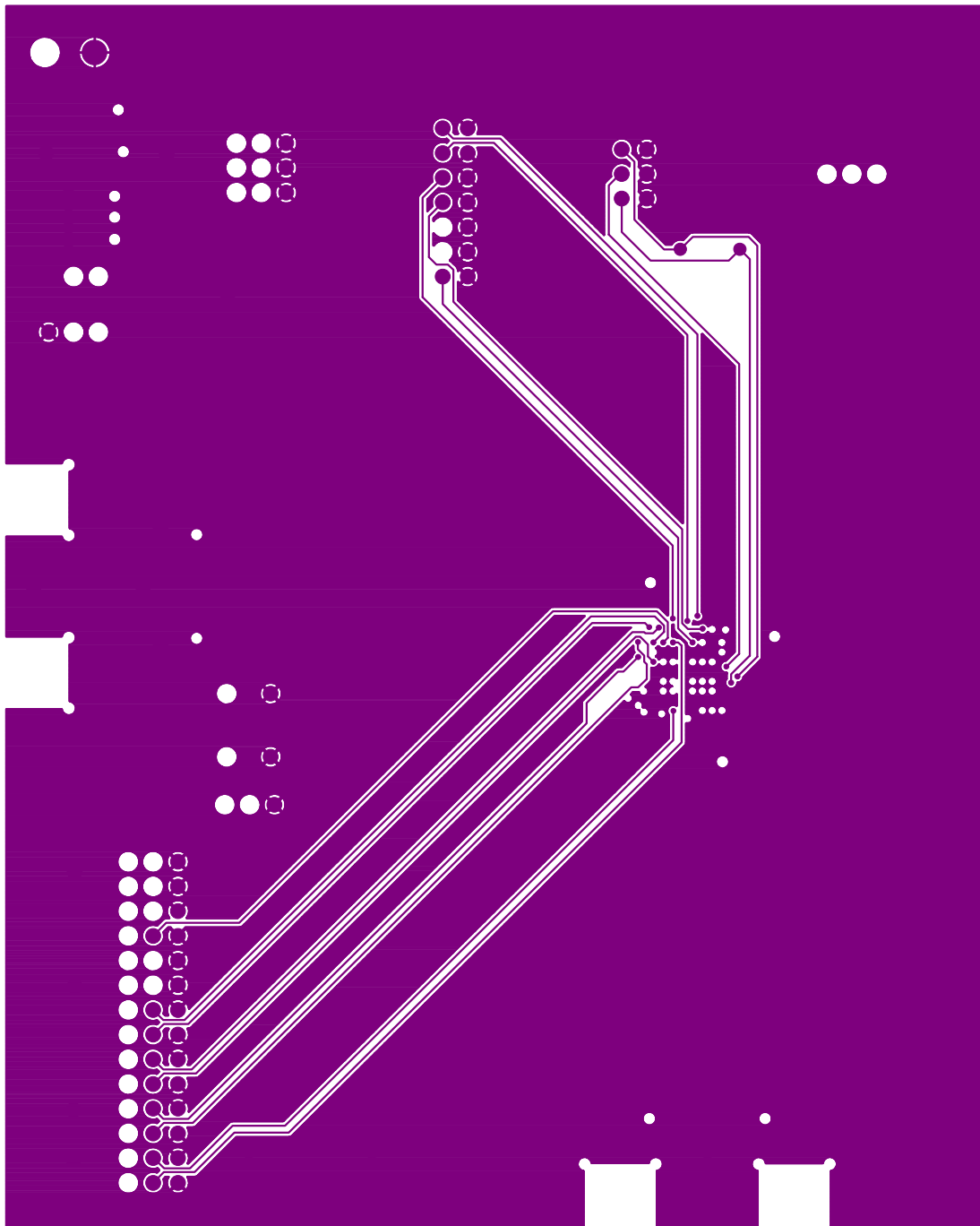


Figure 9. Si5321-EVB—Layer 7, GND



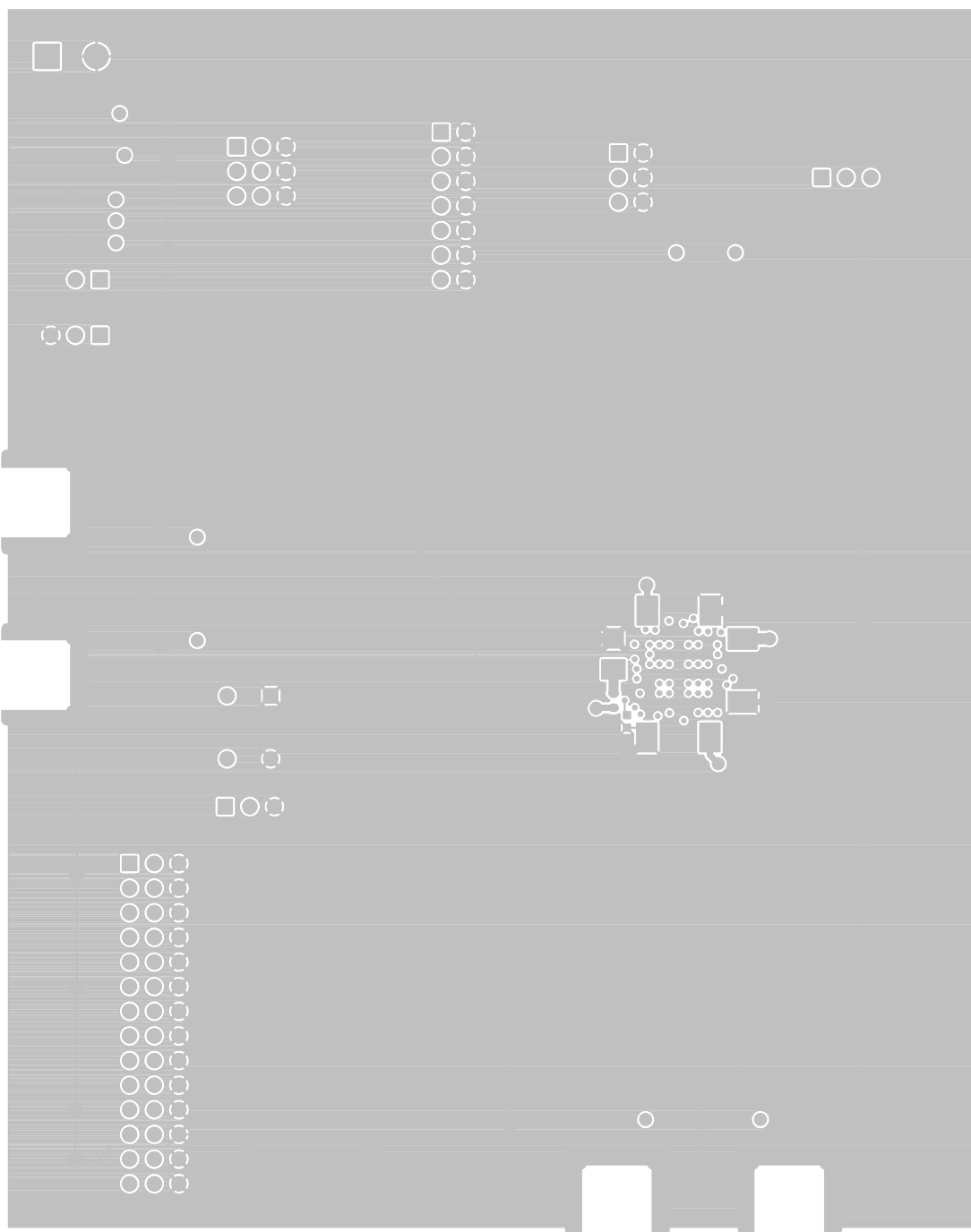


Figure 10. Si5321-EVB—Layer 8, Bottom



# Si5321-EVB

---

## Document Revision Change List

### Revision 0.1 to Revision 0.4

- Updated to reflect Rev. D printed circuit boards.
- Default jumper settings added.

## Evaluation Board Assembly Revision History

| Assembly Level | PCB Rev. | Si5321 Rev. | Assembly Notes            |
|----------------|----------|-------------|---------------------------|
| B-01           | Rev. C   | Rev. B      | Assemble per BOM rev B-01 |



**Notes:**



# Si5321-EVB

---

## Contact Information

Silicon Laboratories Inc.  
4635 Boston Lane  
Austin, TX 78735  
Tel: 1+(512) 416-8500  
Fax: 1+(512) 416-9669  
Toll Free: 1+(877) 444-3032  
Email: [productinfo@silabs.com](mailto:productinfo@silabs.com)  
Internet: [www.silabs.com](http://www.silabs.com)

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders.