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Using the BLVDS04 Demo Kit

The BLVDS04 Demo Kit was designed to allow the user to observe the operation of the DS92LV1023 Serializer and the DS92LV1224 Deserializer. Several configurations are possible. With the purchase of additional kits, multi-drop applications can be modeled.

The kit consists of a backplane card with 4 differential busses, 2 DUT cards; one configured as a serializer and one configured as a deserializer, and 4 adapter cards which can be used to adapt the pin header I/O of the DUT cards to SMB or SMA connectors.

The Backplane card
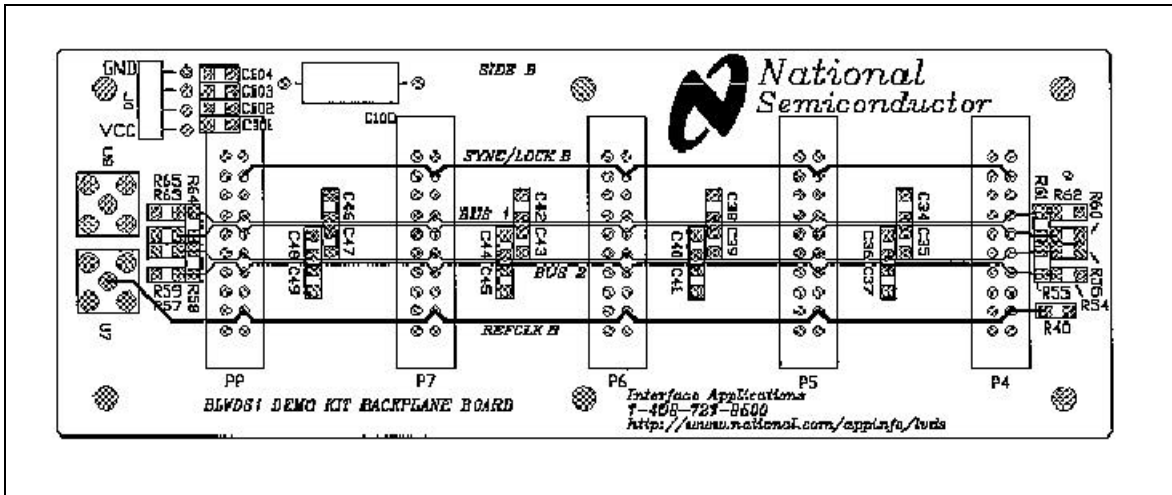
Each side of the backplane card has two differential busses, a REFCLK bus to distribute the REFCLK signal to deserializer cards, and a SYNC/LOCK bus that connects the LOCK* output from deserializers to the SYNC1 input of the serializer.

Each differential bus is designed for a target unloaded impedance of 130 ohms. Since addition of DUT cards and load capacitors will lower this impedance, the busses are terminated in 100 ohms at each end. Each differential bus has 5 'slots' which use 20 pin dip headers to insert DUT cards. Between each of the slots are provisions for adding capacitors to simulate extra loading on the bus. As the bus configuration is changed by adding additional DUT cards or by adding load caps on the bus, the termination resistors should be changed to match the loaded impedance of the bus.
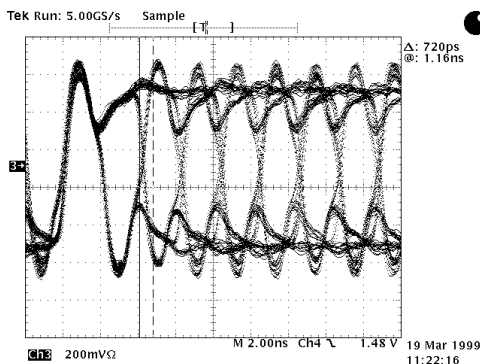
Typical Configuration
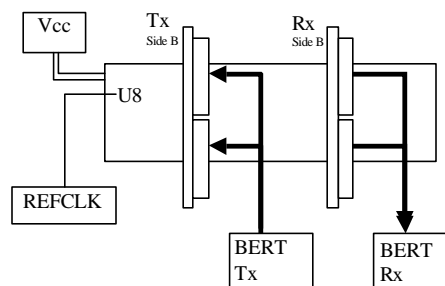
The DUT card

The DUT card can be configured as a serializer card or a deserializer card. The kit comes with 1 card configured as a serializer and 1 card configured as a deserializer.

Serializer Configuration

To configure a card as a serializer, a transmitter (DS92LV1023) must be mounted in the location labeled U2. Additionally jumpers J1, J2, J4 and J5 must be set as follows.
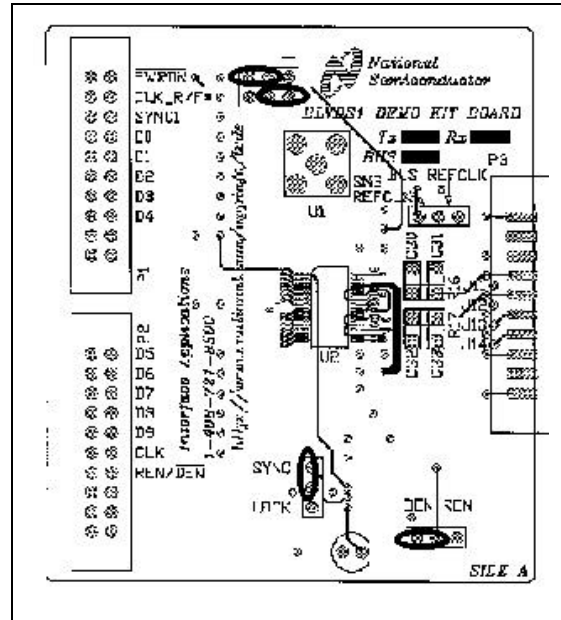
J1 – The setting of J1 controls the TCLKR/F* input. This input can be set statically using J1 or it can be controlled by a data signal through P1 pin 4. Setting TCLK_R/F* high will cause the serializer to use the rising TCLK edge to latch data. Setting TCLK_R/F* low will cause the serializer to use the falling TCLK edge to latch data.

J2 - Connect pins 1-2 to tie PWRDN* high or use a signal through P1 pin 2 to control the serializer PWRDN* pin.

J3 – Controls the REFCLK input source for a deserializer so the setting is a 'don't care' when configured for a serializer.

J4 – J4 should be set in the SYNC position; pins 1-2 connected. This jumper will connect the bus SYNC/LOCK signal to the SYNC1 input of the serializer allowing any deserializers on the bus to request SYNC patterns from the serializer. When using the DS92LV1224, this jumper is optional since the device has random lock capability.

J5 – J5 can be set in the DEN position to permanently enable the serializer or it can be left open and the DEN pin can be driven through pin 14 of connector P2. The REN/DEN* signal is mutually exclusive – that is when the REN/DEN* is high the REN signal to a deserializer is high (deserializer enabled) and the DEN signal to a serializer is low (serializer disabled).

Deserializer Configuration

To configure a DUT card as a deserializer, a receiver (DS92LV1224) must be mounted in the location labeled U3. Additionally, jumpers J1, J2, J3, J4 and J5 must be set as follows.

J1 – The setting of J1 controls the TCLKR/F* input. This input can be set statically using J1 or it can be controlled by a data signal through P1 pin 4. Setting TCLK_R/F* high will cause the deserializer to reference Rout data to the rising RCLK edge. Setting TCLK_R/F* low will cause the deserializer to reference Rout data to the falling RCLK edge.

J2 - Connect pins 1-2 to tie PWRDN* high or use a signal through P1 pin 2 to control the deserializer PWRDN* pin.

J3 – Controls the REFCLK input source for a deserializer. In the SMB REFCLK position (pins 1-2 connected), the REFCLK signal is supplied
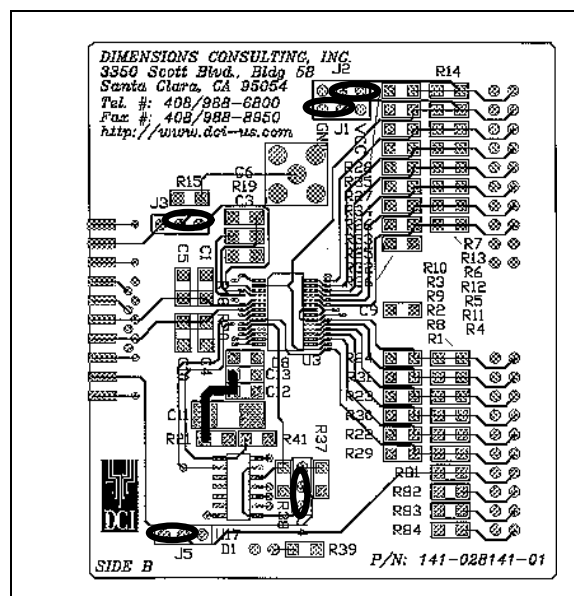
through the SMB connector labeled U1. In the BUS REFCLK position (pins 2-3 connected), the REFCLK signal is supplied from the bus REFCLK channel.

J4 – J4 should be set in the LOCK position; pins 2-3 connected. This jumper will connect the LOCK* output of the deserializer to the bus SYNC/LOCK signal. An open drain inverter is inserted in the line so that multiple deserializers can share the SYNC/LOCK bus. For the DS92LV1224, using this jumper is optional since the device has random lock capability.

J5 – J5 can be set in the REN position to permanently enable the deserializer or it can be left open and the REN pin can be driven through pin 14 of connector P2. The REN/DEN* signal is mutually exclusive – that is when the REN/DEN* is high the REN signal to a deserializer is high (deserializer enabled) and the DEN signal to a serializer is low (serializer disabled).

Optional Terminations

Pads are laid out on side B of the DUT cards to allow for termination of signals to/from the DUT card. If the DUT card is configured as a transmitter there are pads to mount termination resistors to ground. These resistor locations are labeled R22-R35. If the DUT card is laid out as a Receiver series terminations can be added to match or isolate the Rx outputs. Use R1-R14 for series terminations. **Notice that the series terminations are shipped with a shorting trace between the pads. To use the series termination this trace must be cut between the mounting pads.**

BLVDS terminations

Unpopulated pads are also supplied at the BLVDS inputs and outputs. These are provided for experimentation with termination schemes for bus usage and for mounting terminations should the DUT cards be used in a point to point configuration over a cable. Note that the C30 and C32 locations on the A side and the C1 and C4 locations on the B side connect to Vcc providing a convenient location for a pull up termination. Similarly C31 and C33 (A side) and C1 and C4 (side B) connect to GND for a pull down termination.

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Bus Connections

Whether a DUT card is configured as a serializer or a deserializer the BLVDS I/O pins can be connected to any of the 4 busses on the backplane card. The default bus is BUS2 on side A of the backplane card. Other busses can be configured by soldering jumpers and making small cuts to the traces.

To configure a DUT card for Bus2 backplane side B –
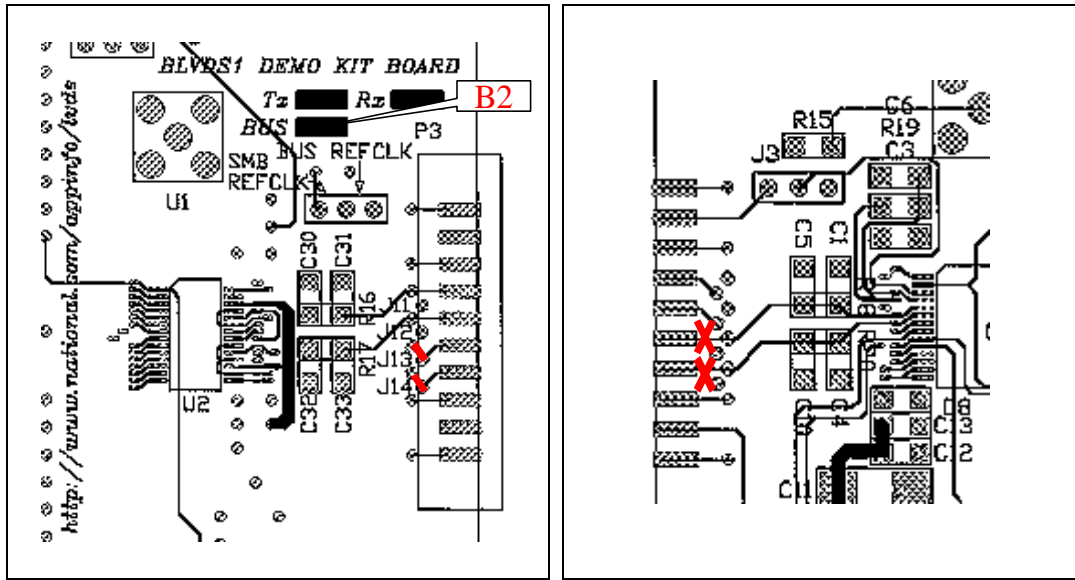
1. Solder jumpers from J13 and J14 to the Bus2 connections on side A of the DUT card.
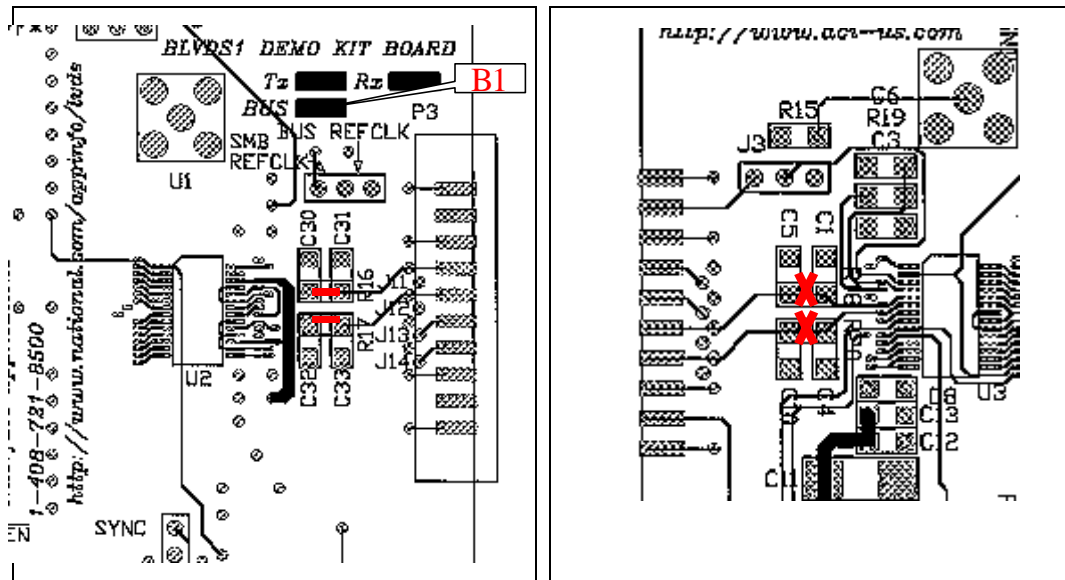2. Cut the traces connecting to Bus2 on side B of the DUT card.

To configure a DUT card for BUS1 side A –
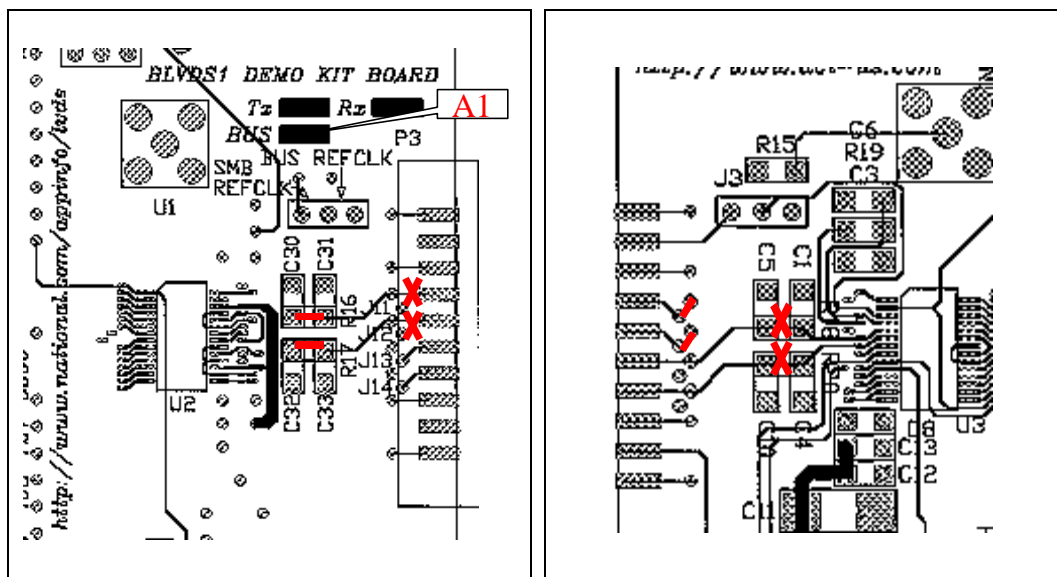
1. On the DUT card, side A, solder a jumper from the R16 pad to the inside pad of C30.

2. On the DUT card, side A, solder a jumper from the R17 pad to the inside pad of C32.
3. On the DUT card, side A, cut the traces from J11 and J12 to the Bus1B connectors.
4. On the DUT card, side B, cut the trace between R18 and the inside pad of C5.
5. On the DUT card, side B, cut the trace between R20 and the inside pad of C10.
6. On the DUT card, side B, solder jumpers from J11 and J12 (DUT card side A) to the DUT card Side B.

To configure a DUT card for BUS1 side B –

1. On the DUT card, side A, solder a jumper from the R16 pad to the inside pad of C30.
2. On the DUT card, side A, solder a jumper from the R17 pad to the inside pad of C32.
3. On the DUT card, side B, cut the trace between R18 and the inside pad of C5.
4. On the DUT card, side B, cut the trace between R20 and the inside pad of C10.

A DUT card should never be configured to connect to more than 1 bus at a time unless the busses have been specially configured to 'daisy chain' the BLVDS signals.

The Adapter Cards

Four adapter cards are supplied with the BLVDS Demo Kit. These cards allow the dip header connections on the DUT cards to be adapted for use with SMB or SMA type connectors. The adapter cards are shipped without the SMB connectors to control the cost of the kit.

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Connector Pinouts

Connector P1			
Pin		Pin	
1	PWRDN*	2	GND
3	CLK_R/F*	4	GND
5	SYNC1	6	GND
7	D0	8	GND
9	D1	10	GND
11	D2	12	GND
13	D3	14	GND
15	D4	16	GND
17	NC	18	GND
19	NC	20	GND

Connector P4, P5, P6, P7, P8			
Pin		Pin	
1	Vcc	2	Vcc
3	REFCLK A	4	SYNC/LOCK B
5	GND	6	GND
7	Bus A1+	8	Bus B1 +
9	Bus A1 -	10	Bus B1 -
11	Bus A2 +	12	Bus B2 +
13	Bus A2 -	14	Bus B2 -
15	GND	16	GND
17	SYNC/LOCK A	18	REFCLK B
19	Vcc	20	Vcc

Connector P2			
Pin		Pin	
1	D5	2	GND
3	D6	4	GND
5	D7	6	GND
7	D8	8	GND
9	D9	10	GND
11	CLK	12	GND
13	REN/DEN*	14	GND
15	NC	16	GND
17	NC	18	GND
19	NC	20	GND

Connector P3 (default pinout)			
Pin		Pin	
1	Vcc	2	Vcc
3	REFCLK A	4	NC
5	GND	6	GND
7	NC	8	NC
9	NC	10	NC
11	Bus A2 +	12	NC
13	Bus A2 -	14	NC
15	GND	16	GND
17	SYNC/LOCK A	18	NC
19	Vcc	20	Vcc

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