

Winbond W6810 Single Channel CODEC

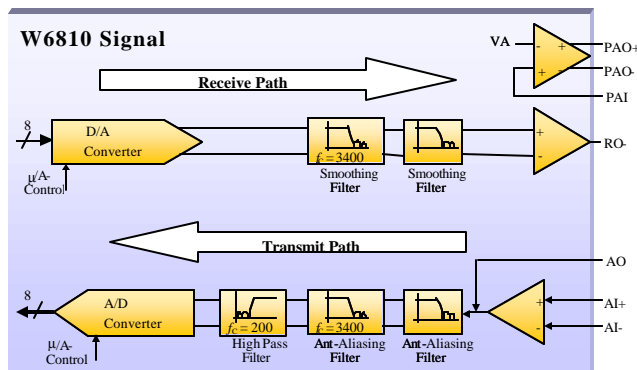
The W6810 single channel CODEC is an analog-to-digital and digital-to-analog converter that complies with the specifications of the ITU-T G.712. The CODEC includes a complete μ -Law and A-Law companders (pin selectable) that are designed to comply with the specifications of the ITU-T G.711.

In order to provide the cleanest signal possible, the W6810 CODEC complies with the ITU-T G.712 recommendation for the Analog to Digital pre filters (also known as anti-aliasing filters) and the Digital-to-Analog post filter (signal smoothing filter).

The W6810 CODEC contains an additional analog power amplifier to drive a higher current output. The power amplifier gain levels can be adjusted by a set of external resistors to drive an output level of up to 6.3V peak-to-peak across a 300- Ω load.

The PCM interface of the W6810 produces 8-bit digital data (μ -Law or A-Law) at a sampling rate of 8kHz and can communicate in four different clock formats, short frame sync, long frame sync, IDL and CGI. The W6810 is available in four different 20-pin packages; PDIP, SOG, SSOP and TSSOP.

For evaluation and prototyping purposes, a development kit, the W6810DK, is available to provide the system designer with a flexible method for developing and testing an application on a single, standalone platform.



Features

- Single supply voltage: 4.5 - 5.5V
- Typical power dissipation of 25mW, power-down of 0.5 μ W
- Fully-differential analog circuit design
- On-chip precision reference voltage of 1.575V for a 0dBm TLP @ 600 Ω
- Push-pull 300 Ω power drivers with external gain adjust
- 8 kHz sample rate
- Master clock rates at 256 kHz, 512 kHz, 1536 kHz, 1544 kHz, 2048 kHz, 2560 kHz and 4096 kHz
- Pin-selectable μ -Law and A-Law companding (full compliance with ITU-T G.711)
- CODEC A/D and D/A filter compliance with ITU-T G.712 specifications
- PCM interface with Short Frame Sync, Long Frame Sync, IDL and GCI timing environments
- Temperature range: Industrial grade (-40 $^{\circ}$ C to 85 $^{\circ}$ C)
- Package: 20-pin PDIP, SOG, SSOP and TSSOP

Benefits

- Low power competitive solution
- System level customization
- Cross reference with other single channel CODEC

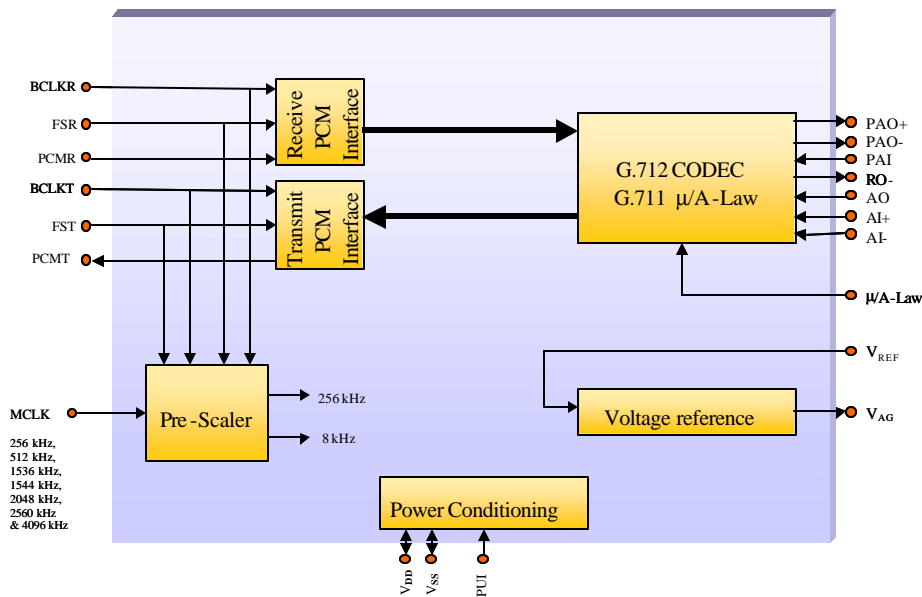
CODEC Applications

- Central office equipment (gateways, switches, routers)
- PBX systems (gateways, switches)
- PABX/SOHO systems
- Local loop card
- SOHO routers
- Fiber-to-the-curb equipment
- Enterprise phones
- Digital telephone systems
- ISDN equipment
- Modems/PC cards

Development System

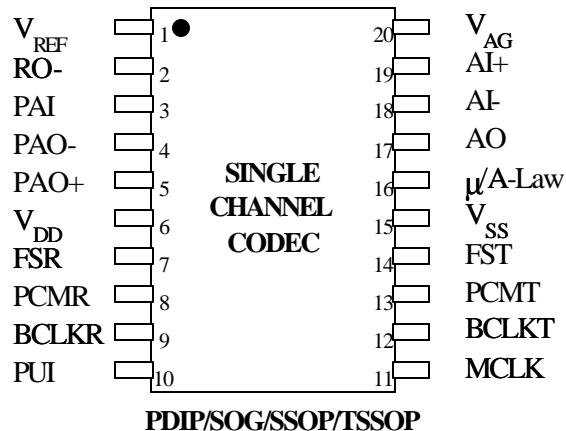
- The W6810DK is a development kit which can be configured in one of the following two modes:
 - **Stand alone** - capable of demo a loop back and prototype a design on a dedicated board space
 - **Back-to-Back** - enables full system test between two platforms

This document contains advanced information and is subject to change at any time.



W6810 Block Diagram

Pin #	Pin Name	Functionality
1	V _{REF}	A bypass for the on-chip 2.5V voltage reference.
2	RO-	Non-Inverting Receive output.
3	PAI	Power amplifier inverted input.
4	PAO-	Inverting Power Amplifier output.
5	PAO+	Non-Inverting Power Amplifier output.
6	V _{DD}	Positive power supply.
7	FSR	Receive Frame Sync input.
8	PCMR	PCM input data receive.
9	BCLKR	Receive bit clock input.
10	PUI	Power up indicator.
11	MCLK	System master clock input.
12	BCLKT	Transmit bit clock input.
13	PCMT	PCM output data transmit pin.
14	FST	Transmit Frame Sync input.
15	V _{SS}	Ground power supply.
16	μ/A-Law	μ-Law /A-Law companding select pin.
17	AO	Transmit gain output.
18	AI-	Inverting Transmit input.
19	AI+	Non-Inverting Transmit input.
20	V _{AG}	Analog signal reference ground output.



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Note: For more details on Winbond's W6810 please refer to the product datasheet.

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