

Soffee

Development P for the Emberlie OK

SJSTERT SOTWARE

Real-Time Code Execution Without **Probes–Works** with All Packages

Standard Chip **Used-No** Bondouts, 100% Electrical Characteristics Guaranteed CAN

C Compiler<sup>®</sup> Included (Leimited Evaluation)

STVD7 Source Level Debugger 5

**Built-In ISP** Programmer

ST72CXXX Devices Supported

Demo Board Included on Design Kit Packages

# ST7C-inDART/D In-Circuit Debugger for STMicroelectronics **ST72CXXX FLASH Devices**

Softes

THILD BE STATE





www.softecmicro.com

www.softeemicro.com

# ST7C-inDART/D In-Circuit Debugger for STMicroelectronics ST72CXXX FLASH Devices

# **Overview**

inDART-ST7 Series In-Circuit Debuggers are powerful entry-level tools for STMicroelectronics ST7-based systems. inDART-ST7 Series In-Circuit Debuggers take advantage of STMicroelectronics' STVD7 (STMicroelectronics Visual Debug) Integrated Development Environment and the ISP (In Situ Programming) feature to program the FLASH memory of the ST7 family of microcontrollers. Together with STVD7, inDART-ST7 Series In-Circuit Debuggers provide you with everything you need to write, compile,

download, in-circuit emulate and debug user code. Full speed program execution allows you to perform hardware and software testing in real time. inDART-ST7 Series In-Circuit Debuggers are connected to the host PC through a parallel port, while the 10-pin probe of the debuggers fits into the target's standard ISP connector.

### STVD7 Integrated **Development Environment**

The inDART-ST7 user interface (common for all of the inDART-ST7 Series In-Circuit Debuggers) is based on the ST7 Visual Debug Integrated Development Environment (STVD7).

STVD7 enables programs to be executed and stopped where desired, while viewing the memory contents. It offers the ability to step through and examine code at the C source level and the Assembly instruction level. You can introduce breakpoints and run or

single-step the executable, while viewing the source and observing current program values. All registers and memory locations are accessible for both read and write operations.

## **Demo Boards**

On Design Kits packages, a full-featured experiment board for a specific ST7 microcontroller is also included. Each demo board includes DIP-switches, jumpers, LEDs, push-buttons, a potentiometer, prototyping area and a standard ISP connector and can be used for evaluation/ experiments in the absence of a target application board.

# What is In Situ Programming (ISP)?

The ISP feature allows you to update the content of FLASH program memory when the chip is already plugged on the application board. ISP programming uses a serial protocol to interface a programming tool like inDART. The ISP feature can be implemented with a minimum number of added components and board area impact. inDART-ST7 Series In-Circuit Debuggers use the standard, 10-pin ST7 ISP [FMP] - Full Merrory Protection connector to program and in-circuit emulate the (EXTIT) · External Interrunt Configuration target device. [WDG SW] Watchdog Activation



for the EmbeddedWorld Web: http://www.softecmicro.com

e-mail: info@softecmicro.com

ST22C254629 Soffee Microsystems inDART ST2 sample.wsp [Debug] sample.eff [main.o]						<u>.</u>	
al Sa Si War E fat Dawy F	and a Cash Span -	Ни з					
2 # C 🛛 🖉 🖧 🖓 🖓	8381 9	+SED	224	E R stext	- K		6 er . + 3 3 14
MB 5 5 0 0 •		19 10 10 10	19-11 2	15	<b>副版</b>	· ·· · · · · · · · · · · · · · · · · ·	
skopenne 📑 🔊	0 /1111111	***********	********		********	*********	*****
E restaur E arobic → B arob	30 -7 The fully   14 Rescine 1 Rescine 1   38 Rescine 1 Rescine 1   34 Rescine 1 Rescine 1   35 Rescine 1 Rescine 1   36 Rescine 1 Rescine 1   37 Rescine 1 Rescine 1   38 Rescine 1 Rescine 1   39 Rescine 1 Rescine 1   30 Rescine 1 Rescine 1   38 Rescine 1 Rescine 1   39 Rescine 1 Rescine 1   30 Rescine 1 Rescine 1	"sort2204.b" bares (s. L) bren (k. P) boss (s. L) tranfdi cras cras cras for beso	16  - 16 5- 1121 3 70 70 70 70	2114 Lessory and a (.a.1440000 - 75100000 - 7510000 - 7510000 - 7510000 - 751000 - 751000 - 75000 - 750000 - 75000 - 750000 - 75000 - 75000 - 75000 -	A to cutou perspheral "refried	с. 03 УС	
I / Perghesal Registers enacts facilities	_	live m		FF SIZHouse	010	200	ALM AL
R 150 The A		100.05		Togen!	Co.rter	942.53	Index existent
0. 15E1 Time 3					-014	s> luxui ra	× UAUS × UAUS
🖹 - E-BLAAR Discondin (6.1-1							
E H M ADDR 14 - Edu - E H M ADDR 14 Extored a Reput		rh cy para		Acares	Acts measure Condition Flage		
- JULIA AUTAS LAND SIA RECTOR		JUI HOART			> fod5 D: foxel FILELENEETC		
	- ADON - ArD Do wetter - 2000 - Convention Complete						

#### **Supported Devices**

STMicroelectronics ST72CXXX (ST72104, 124, 171, 215, 216, 254, 314, 334).

#### **Debugging Capabilities**

- Source level and symbolic debugger;
- Reset, Go, Go From Reset, Go to Cursor,
- Stop, Step Into, Step Over, Step Out;
- Unlimited number of breakpoints · Watch variables, registers and peripherals.

#### **Programming Capabilities**

- Blank Check/Erase/Program/Read/Verify FLASH memory;
- Blank Check/Erase/Program/Read/Verify EEPROM memory
- Blank Check/Erase/Program/Read/Verify Option Bytes.

#### **System Requirements**

- A PC running Windows 9x, 2000 or NT;
- 32 MB of RAM plus 20 MB of HD space;
- One free parallel port.

Electrical And Physical Specifications Operating Voltage: 5 V DC (from target board, via ISP connector) or 9 - 12 V DC (from power connector)

Power Consumption: 10 mA Dimensions: 70 x 55 x 15 mm Weight: 25 g Temperature Range: 0 - 50 °C

#### **Ordering Information**

×

Carusi

Start

Exit

ST7C-INDART/D: standalone inDART-ST7 for the support (debugging/programming) of ST72CXXX devices. Requires a working user target board.

ST7C254-INDART, ST7C334-INDART: Design Kit packages. Include a device-specific demo board, ready to be used with ST7C-INDART/D.

Order Code	In-Circuit Debugger/	Demo Board	
ST7C-INDART/D			
ST7C254-INDART		(*)	
ST7C334-INDART		(**)	

(\*) For ST72C104, 215, 216, 254 (\*\*) For ST72C314, 334

Software Upgrades The latest version of the inDART-ST7

series user interface is always downloadable for free from our web site.



14 MHz Inteina F

Sullware

LVD OT

IT J= PAZ FA0, T1=P37 FB0/PC5

Clear Read-Out Protection Erase Device Program FLASH Memory

Verify FLASH Memory Program Option Bytes Set Read-Out Protection

E B

(wDC HALT) - Walchdog and Halt viola

[LVD] - Low Voltage Detection Selection

(OSC)-Oscillato Selection

[UFU] - Licck Hiter Control

www.softecmicro.com