

### FEATURES

- Buffer memory board for capturing digital data used with high speed ADC evaluation boards to simplify evaluation
- 32 kB FIFO depth at 133 MSPS (upgradable)
- Measures performance with ADC Analyzer™
  - Real-time FFT and time domain analysis
  - Analyzes SNR, SINAD, SFDR, and harmonics
- Simple USB port interface (2.0)
- Supporting ADCs with serial port interfaces (SPI®)
- On-board regulator circuit, no power supply required
  - 6 V, 2 A switching power supply included
- Compatible with Windows® 98 (2nd ed.), Windows 2000, Windows Me, and Windows XP

### EQUIPMENT NEEDED

- Analog signal source and antialiasing filter
- Low jitter clock source
- High speed ADC evaluation board and ADC data sheet
- PC running Windows 98 (2nd ed.), Windows 2000, Windows Me, or Windows XP
- Latest version of ADC Analyzer
- USB 2.0 port recommended (USB 1.1-compatible)

### PRODUCT DESCRIPTION

The high speed ADC FIFO evaluation kit includes the latest version of ADC Analyzer and a buffer memory board to capture blocks of digital data from the Analog Devices high speed analog-to-digital converter (ADC) evaluation boards. The FIFO board is connected to the PC through a USB port and is used with ADC Analyzer to quickly evaluate the performance of high speed ADCs. Users can view an FFT for a specific analog input and encode rate to analyze SNR, SINAD, SFDR, and harmonic information.

The evaluation kit is easy to set up. Additional equipment needed includes an Analog Devices high speed ADC evaluation board, a signal source, and a clock source. Once the kit is connected and powered, the evaluation is enabled instantly on the PC.

Two versions of the FIFO are available. The HSC-ADC-EVALB-DC is used with multichannel ADCs and converters with demultiplexed digital outputs. The HSC-ADC-EVALB-SC evaluation board is used with single-channel ADCs. See Table 1 to choose the FIFO appropriate for your high speed ADC evaluation board.

#### Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

### FUNCTIONAL BLOCK DIAGRAM

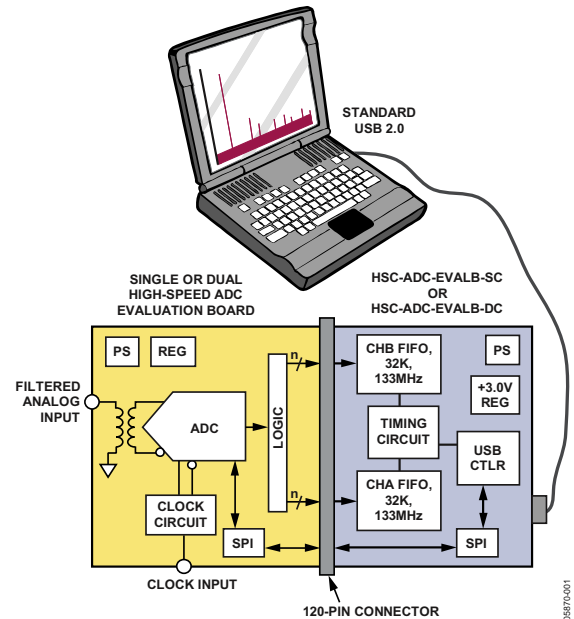


Figure 1.

### PRODUCT HIGHLIGHTS

1. **Easy to Set Up.** Connect the included power supply and signal sources to the two evaluation boards. Then connect to the PC and evaluate the performance instantly.
2. **ADIsimADC™.** ADC Analyzer supports virtual ADC evaluation using ADI proprietary behavioral modeling technology. This allows rapid comparison between multiple ADCs, with or without hardware evaluation boards. For more information, see AN-737 at [www.analog.com/ADIsimADC](http://www.analog.com/ADIsimADC).
3. **USB Port Connection to PC.** PC interface is a USB 2.0 connection (1.1-compatible) to the PC. A USB cable is provided in the kit.
4. **32 kB FIFO.** The FIFO stores data from the ADC for processing. A pin-compatible FIFO family is used for easy upgrading.
5. **Up to 133 MSPS Encode Rate on Each Channel.** Single-channel ADCs with encode rates up to 133 MSPS can be used with the FIFO board. Multichannel and demultiplexed output ADCs can also be used with the FIFO board with clock rates up to 266 MSPS.
6. **Supports ADC with Serial Port Interface or SPI.** Some ADCs include a feature set that can be changed via the SPI. The FIFO supports these SPI-driven features through the existing USB connection to the computer without additional cabling needed.

## TABLE OF CONTENTS

Features .....	1	Clocking with Interleaved Data.....	10
Equipment Needed.....	1	Connecting to the HSC-ADC-FPGA-4/-8 .....	10
Product Description.....	1	Connecting to the DEMUX BRD .....	10
Functional Block Diagram .....	1	Upgrading FIFO Memory .....	10
Product Highlights .....	1	Jumpers .....	11
Revision History .....	2	Default Settings.....	11
FIFO Evaluation Board Easy Start.....	3	Evaluation Board .....	13
Requirements .....	3	Power Supplies.....	13
Easy Start Steps .....	3	Connection and Setup .....	13
Virtual Evaluation Board Easy Start With ADIsimADC .....	4	FIFO Schematics and PCB Layout.....	14
Requirements .....	4	Schematics.....	14
Easy Start Steps .....	4	PCB Layout .....	21
FIFO 4.1 Data Capture Board Features .....	5	Bill of Materials.....	23
FIFO 4.1 Supported ADC Evaluation Boards .....	6	Ordering Information.....	25
Theory of Operation .....	9	Ordering Guide .....	25
Clocking Description.....	9	ESD Caution.....	25
SPI Description.....	9		

## REVISION HISTORY

2/06—Revision 0: Initial Version

## FIFO EVALUATION BOARD EASY START

### REQUIREMENTS

- FIFO evaluation board, ADC Analyzer, and USB cable
- High speed ADC evaluation board and ADC data sheet
- Power supply for ADC evaluation board
- Analog signal source and appropriate filtering
- Low jitter clock source applicable for specific ADC evaluation, typically <1 ps rms
- PC running Windows 98 (2nd ed.), Windows 2000, Windows Me, or Windows XP
- PC with a USB 2.0 port recommended (USB 1.1-compatible)

### EASY START STEPS

Note: You need administrative rights for the Windows operating systems during the entire easy start procedure. It is recommended to complete every step before reverting to a normal user mode.

1. Install ADC Analyzer from the CD provided in the FIFO evaluation kit or download the latest version on the Web. For the latest updates to the software, check the Analog Devices website at [www.analog.com/hsc-FIFO](http://www.analog.com/hsc-FIFO).
2. Connect the FIFO evaluation board to the ADC evaluation board. If an adapter is required, insert the adapter between the ADC evaluation board and the FIFO board. If using the HSC-ADC-EVALB-SC model, connect the evaluation board to the bottom two rows of the 120-pin connector, closest to the installed IDT FIFO chip. If using an ADC with a SPI interface, remove the two 4-pin corner keys so that the third row can be connected.
3. Connect the provided USB cable to the FIFO evaluation board and to an available USB port on the computer.
4. Refer to Table 5 for any jumper changes. Most evaluation boards can be used with the default settings.
5. After verification, connect the appropriate power supplies to the ADC evaluation boards. The FIFO evaluation board is supplied with a wall mount switching power supply that provides a 6 V, 2 A maximum output. Connect the supply end to the rated 100 ac to 240 ac wall outlet at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at J301. Refer to the instructions included in the [ADC data sheet](#) for more information about the ADC evaluation board's power supply and other requirements.
6. Once the cable is connected to both the computer and the FIFO board, and power is supplied, the USB drivers start to install. To complete the total installation of the FIFO drivers, you need to complete the new hardware sequence two times. The first **Found New Hardware Wizard** opens with the text message **This wizard helps you install software for...Pre-FIFO 4.1**. Click the recommended install, and go to the next screen. A hardware installation warning window should then be displayed. Click **Continue Anyway**. The next window that opens should finish the Pre-FIFO 4.1 installation. Click **Finish**. Your computer should go through a second **Found New Hardware Wizard**, and the text message, **This wizard helps you install software for...Analog Devices FIFO 4.1**, should be displayed. Continue as you did in the previous installation and click **Continue Anyway**. Then click **Finish** on the next two windows. This completes the installation.
7. (Optional) Verify in the device manager that **Analog Devices, FIFO4.1** is listed under the USB hardware.
8. Apply power to the evaluation board and check the voltage levels at the board level.
9. Connect the appropriate analog input (which should be filtered with a band-pass filter) and low jitter clock signal. Make sure the evaluation boards are powered on before connecting the analog input and clock.
10. Start ADC Analyzer.
11. Choose an existing configuration file for the ADC evaluation board or create one.
12. Click **Time Data** in ADC Analyzer (left-most button under the menus). A reconstruction of the analog input is displayed. If the expected signal does not appear, or if there is only a flat red line, refer to the ADC Analyzer data sheet at [www.analog.com/hsc-FIFO](http://www.analog.com/hsc-FIFO) for more information.

## VIRTUAL EVALUATION BOARD EASY START WITH ADIsimADC

### REQUIREMENTS

Requirements include

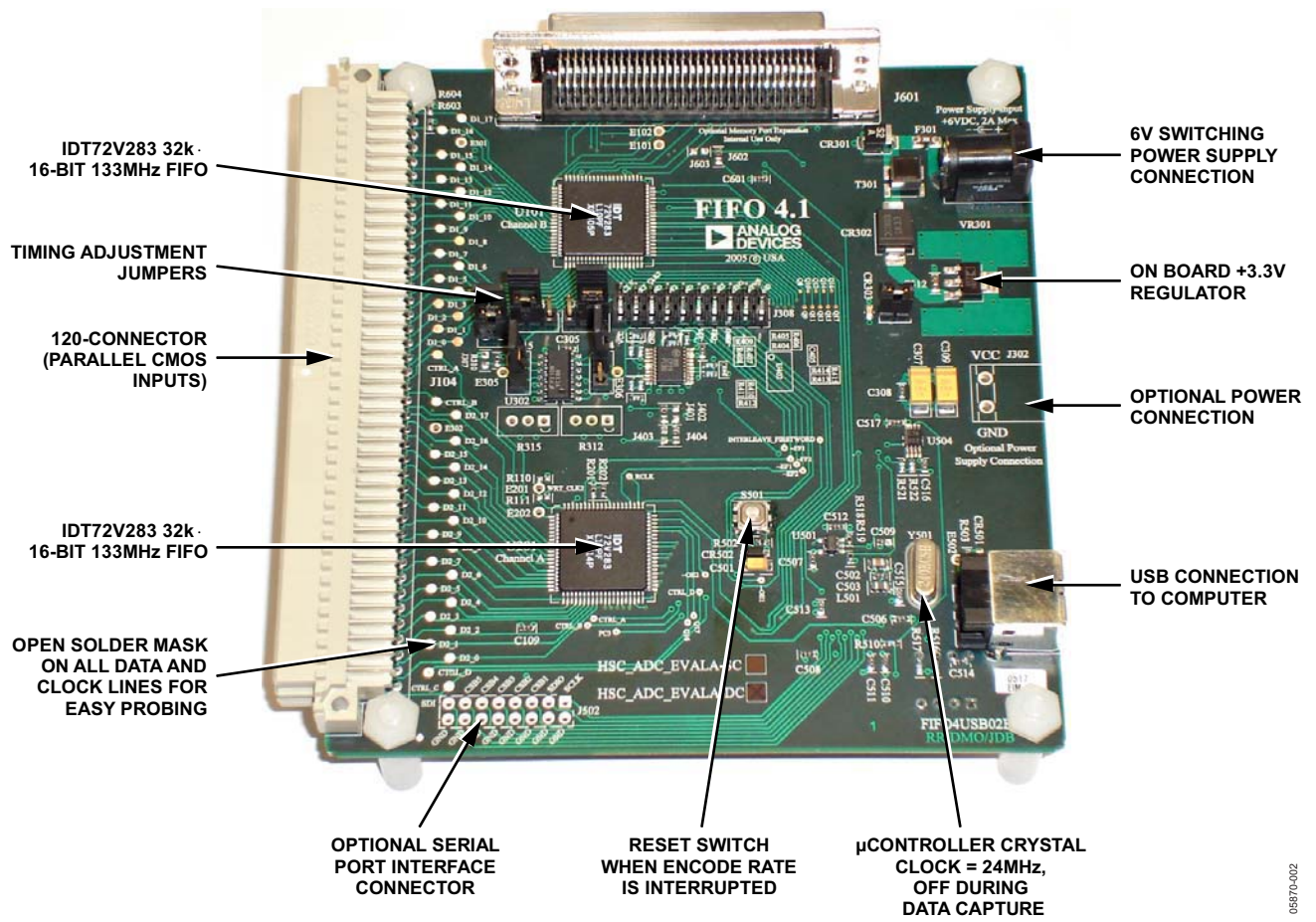
- Completed installation of ADC Analyzer, Version 4.5.17 or later.
- ADIsimADC product model files for the desired converter. Models are not installed with the software, but they can be downloaded from the [ADIsimADC Virtual Evaluation Board website](#) at no charge.

No hardware is required. However, if you wish to compare results of a real evaluation board and the model, you can switch easily between the two, as outlined in the following Easy Start Steps section.

### EASY START STEPS

1. To get ADC model files, go to [www.analog.com/ADIsimADC](http://www.analog.com/ADIsimADC) for the product of interest. Download the product of interest to a local drive. The default location is c:\program files\adc\_analyzer\models.
2. Start ADC Analyzer (see the [ADC Analyzer User Manual](#)).
3. From the menu, click **Config > Buffer > Model** as the buffer memory. In effect, the model functions in place of the ADC and data capture hardware.
4. After selecting the model, click the **Model** button (located next to the **Stop** button) to select and configure which converter is to be modeled. A dialog box appears in the workspace, where you can select and configure the behavior of the model.
5. In the **ADC Modeling** dialog box, click the **Device** tab and then click the **... (Browse)** button, adjacent to the dialog box. This opens a file browser and displays all of the models found in the default directory: c:\program files\adc\_analyzer\models. If no model files are found, follow the on-screen directions or see Step 1 to install available models. If you have saved the models somewhere other than the default location, use the browser to navigate to that location and select the file of interest.
6. From the menu, click **Config > FFT**. In the **FFT Configuration** dialog box, ensure that the **Encode Frequency** is set for a valid rate for the simulated device under test. If set too low or too high, the model does not run.
7. Once a model has been selected, information about the model displays on the **Device** tab of the **ADC Modeling** dialog box. After ensuring that you have selected the right model, click the **Input** tab. This lets you configure the input to the model. Click either **Sine Wave** or **Two Tone** for the input signal.
8. Click **Time Data** (left-most button under the pull-down menus). A reconstruction of the analog input is displayed. The model can now be used just as a standard evaluation board would be.
9. The model supports additional features not found when testing a standard evaluation board. When using the modeling capabilities, it is possible to sweep either the analog amplitude or the analog frequency. For more information consult the [ADC Analyzer User Manual](#) at [www.analog.com/hsc-FIFO](http://www.analog.com/hsc-FIFO).

## FIFO 4.1 DATA CAPTURE BOARD FEATURES





# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

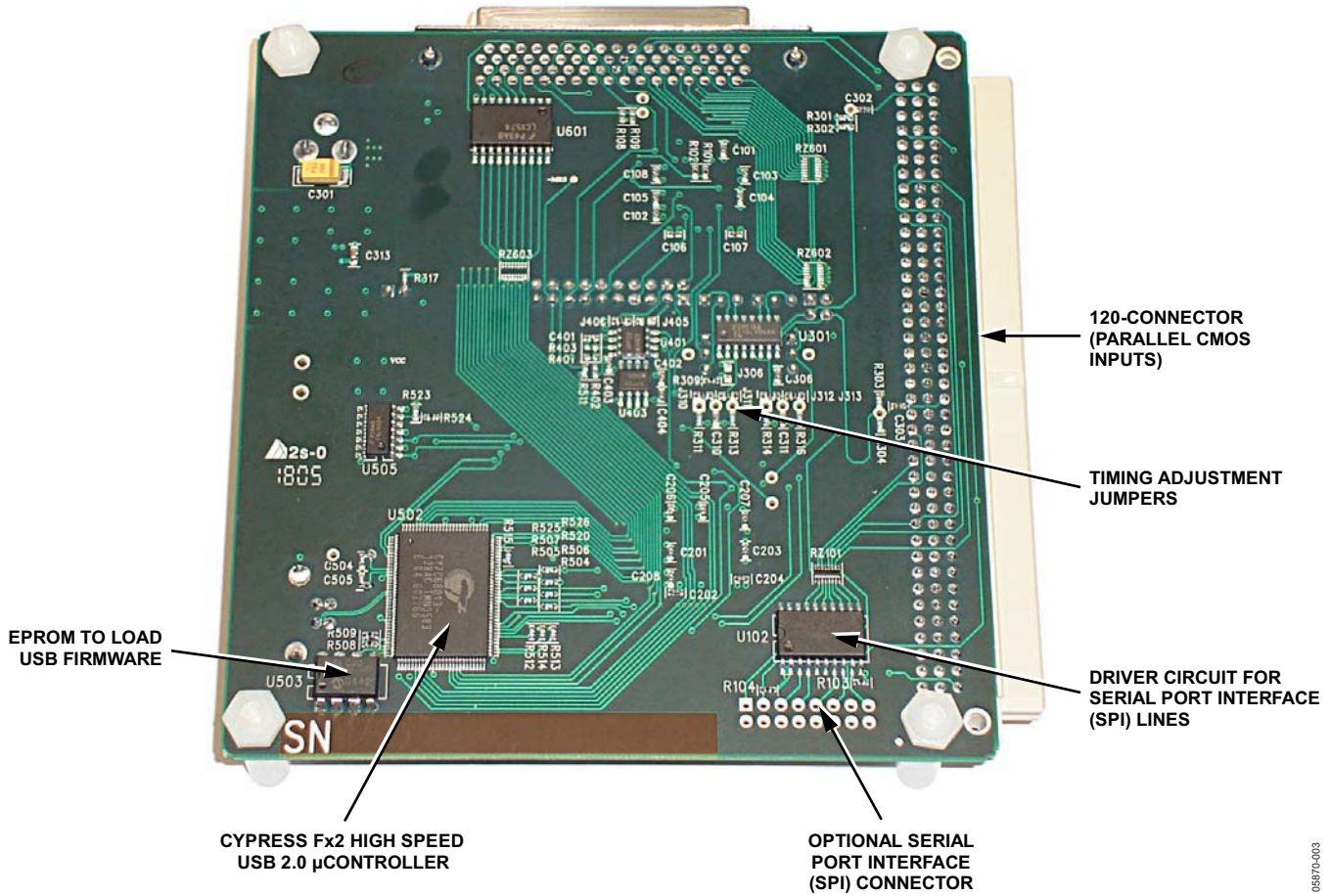


Figure 3. FIFO Components (Bottom View)

## FIFO 4.1 SUPPORTED ADC EVALUATION BOARDS

The evaluation boards in Table 1 can be used with the high speed ADC FIFO evaluation kit. Some evaluation boards require an adapter between the ADC evaluation board connector and the FIFO connector. If an adapter is needed, send an email to [highspeed.converters@analog.com](mailto:highspeed.converters@analog.com) with the part number of the adapter and a mailing address.

Table 1. HSC-ADC-EVALB-DC- and HSC-ADC-EVALB-SC-Compatible Evaluation Boards<sup>1</sup>

Evaluation Board Model	Description of ADC	FIFO Board Version	Comments
AD6644ST/PCB	14-bit, 65 MSPS ADC	SC	
AD6645-80/PCB	14-bit, 80 MSPS ADC	SC	
AD6645-105/PCB	14-bit, 105 MSPS ADC	SC	
AD9051/PCB	10-bit, 60 MSPS ADC	SC	Requires AD9051FFA
AD9200SSOP-EVAL	10-bit, 20 MSPS ADC	SC	Requires AD922xFFA
AD9200TQFP-EVAL	10-bit, 20 MSPS ADC	SC	Requires AD922xFFA
AD9201-EVAL	Dual 10-bit, 20 MSPS ADC <sup>1</sup>	SC	Requires AD922xFFA
AD9203-EB	10-bit, 40 MSPS ADC	SC	Requires AD922xFFA
AD9212-65EB <sup>1</sup>	Octal 10-bit, 65 MSPS ADC	DC	Requires HSC-ADC-FPGA-8
AD9215BCP-65EB	10-bit, 65 MSPS ADC	SC	
AD9215BCP-80EB	10-bit, 80 MSPS ADC	SC	
AD9215BCP-105EB	10-bit, 105 MSPS ADC	SC	
AD9215BRU-65EB	10-bit, 65 MSPS ADC	SC	
AD9215BRU-80EB	10-bit, 80 MSPS ADC	SC	
AD9215BRU-105EB	10-bit, 105 MSPS ADC	SC	
AD9216-80PCB	Dual 10-bit, 80 MSPS ADC	DC	
AD9216-105PCB	Dual 10-bit, 105 MSPS ADC	DC	

# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

Evaluation Board Model	Description of ADC	FIFO Board Version	Comments
AD9218-105PCB	10-bit, 105 MSPS ADC	DC	
AD9218-65PCB	10-bit, 65 MSPS ADC	DC	
AD9219-65EB <sup>1</sup>	Quad 10-bit, 65 MSPS ADC	DC	Requires HSC-ADC-FPGA-4/-8
AD9220-EB	12-bit, 10 MSPS ADC	SC	Requires AD922xFFA
AD9222-65EB <sup>1</sup>	Octal 12-bit, 65 MSPS ADC	DC	Requires HSC-ADC-FPGA-8
AD9226-EB	12-bit, 65 MSPS ADC	SC	Requires AD922xFFA
AD9226QFP-EB	12-bit, 65 MSPS ADC	SC	Requires AD922xFFA
AD9228-65EB <sup>1</sup>	Quad 12-bit, 65 MSPS ADC	DC	Requires HSC-ADC-FPGA-4/-8
AD9229-65EB <sup>1</sup>	Quad 12-bit, 65 MSPS ADC	DC	Requires HSC-ADC-FPGA-4/-8
AD9233-80EB	12-bit, 80MSPS ADC	SC	
AD9233-105EB	12-bit, 105MSPS ADC	SC	
AD9233-125EB	12-bit, 125MSPS ADC	SC	
AD9234-EB	12-bit, 150MSPS ADC	SC	
AD9235BCP-20EB	12-bit, 20 MSPS ADC	SC	
AD9235BCP-40EB	12-bit, 40 MSPS ADC	SC	
AD9235BCP-65EB	12-bit, 65 MSPS ADC	SC	
AD9235-20PCB	12-bit, 20 MSPS ADC	SC	
AD9235-40PCB	12-bit, 40 MSPS ADC	SC	
AD9235-65PCB	12-bit, 65 MSPS ADC	SC	
AD9236BRU-80EB	12-bit, 80 MSPS ADC	SC	
AD9236BCP-80EB	12-bit, 80 MSPS ADC	SC	
AD9237BCP-20EB	12-bit, 20 MSPS ADC	SC	
AD9237BCP-40EB	12-bit, 40 MSPS ADC	SC	
AD9237BCP-65EB	12-bit, 65 MSPS ADC	SC	
AD9238BST-20PCB	Dual 12-bit, 20 MSPS ADC	DC	
AD9238BST-40PCB	Dual 12-bit, 40 MSPS ADC	DC	
AD9238BST-65PCB	Dual 12-bit, 65 MSPS ADC	DC	
AD9238BCP-20EB	Dual 12-bit, 20 MSPS ADC	DC	
AD9238BCP-40EB	Dual 12-bit, 40 MSPS ADC	DC	
AD9238BCP-65EB	Dual 12-bit, 65 MSPS ADC	DC	
AD9240-EB	14-bit, 40 MSPS ADC	SC	Requires AD922xFFA
AD9241-EB	14-bit, 1.25 MSPS ADC	SC	Requires AD922xFFA
AD9243-EB	14-bit, 3 MSPS ADC	SC	Requires AD922xFFA
AD9244-40PCB	14-bit, 40 MSPS ADC	SC	
AD9244-65PCB	14-bit, 65 MSPS ADC	SC	
AD9245BCP-20EB	14-bit, 20 MSPS ADC	SC	
AD9245BCP-40EB	14-bit, 40 MSPS ADC	SC	
AD9245BCP-65EB	14-bit, 65 MSPS ADC	SC	
AD9245BCP-80EB	14-bit, 80 MSPS ADC	SC	
AD9246-80EB	14-bit, 80 MSPS ADC	SC	
AD9246-105EB	14-bit, 105 MSPS ADC	SC	
AD9246-125EB	14-bit, 125 MSPS ADC	SC	
AD9248BST-65EB	Dual 14-bit, 65 MSPS ADC	DC	
AD9248BCP-20EB	Dual 14-bit, 20 MSPS ADC	DC	
AD9248BCP-40EB	Dual 14-bit, 40 MSPS ADC	DC	
AD9248BCP-65EB	Dual 14-bit, 65 MSPS ADC	DC	
AD9259-50EB <sup>1</sup>	Quad 14-bit, 50 MSPS ADC	DC	Requires HSC-ADC-FPGA-4/-8
AD9260-EB	16-bit, 2.5 MSPS ADC	SC	Requires AD922xFFA
AD9280-EB	8-bit, 32 MSPS ADC	SC	Requires AD922xFFA
AD9281-EB	Dual 8-bit, 28 MSPS ADC	SC	Requires AD922xFFA
AD9283/PCB	8-bit, 100 MSPS ADC	SC	Requires AD9283FFA
AD9287-100EB <sup>1</sup>	Quad 8-bit, 100 MSPS ADC	DC	Requires HSC-ADC-FPGA-4/-8
AD9289-65EB <sup>1</sup>	Quad 8-bit, 65 MSPS ADC	DC	Requires HSC-ADC-FPGA-9289
AD9411/PCB	10-bit, 200 MSPS ADC	DC	Requires DEMUX BRD

# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

Evaluation Board Model	Description of ADC	FIFO Board Version	Comments
AD9430-CMOS/PCB	12-bit, 210 MSPS ADC	DC	
AD9430-LVDS/PCB <sup>2</sup>	12-bit, 210 MSPS ADC	DC	Requires DEMUX BRD
AD9432/PCB	12-bit, 105 MSPS ADC	SC	
AD9433/PCB	12-bit, 125 MSPS ADC	SC	
AD9444-CMOS/PCB	14 bit, 80 MSPS ADC	SC	
AD9444-LVDS/PCB	14 bit, 80 MSPS ADC	SC	
AD9445-IF-LVDS/PCB	14-bit, 125 MSPS ADC	SC	
AD9445-BB-LVDS/PCB	14-bit, 125 MSPS ADC	SC	
AD9446-80LVDS/PCB	16-bit, 80 MSPS ADC	SC	
AD9446-100LVDS/PCB	16-bit, 100 MSPS ADC	SC	
AD9460-80EB-IF	16-bit, 80 MSPS ADC	SC	
AD9460-80EB-BB	16-bit, 80 MSPS ADC	SC	
AD9460-105EB-IF	16-bit, 105 MSPS ADC	SC	
AD9460-105EB-BB	16-bit, 105 MSPS ADC	SC	
AD9461-130EB-IF	16-bit, 130 MSPS ADC	SC	
AD9461-130EB-BB	16-bit, 130 MSPS ADC	SC	
AD9480-LVDS/PCB <sup>2</sup>	8-bit, 250 MSPS ADC	DC	Requires DEMUX BRD
AD9481-PCB	8-bit, 250 MSPS ADC	DC	
AD10200/PCB	Dual 12-bit, 105 MSPS ADC	DC	Requires GS09066
AD10201/PCB	Dual 12-bit, 105 MSPS ADC	DC	Requires GS09066
AD10226/PCB	Dual 12-bit, 125 MSPS ADC	DC	Requires GS09066
AD10265/PCB	Dual 12-bit, 65 MSPS ADC	DC	Requires GS09066
AD10465/PCB	Dual 14-bit, 65 MSPS ADC	DC	Requires GS09066
AD10677/PCB	16-bit, 65 MSPS ADC	SC	Requires GS09066
AD10678/PCB	16-bit, 80 MSPS ADC	SC	Requires GS09066
AD15252/PCB	12-bit, Dual 65 MSPS ADC	DC	
AD15452/PCB	12-bit, Quad 65 MSPS ADC	DC	Requires HSC-ADC-FPGA-4/-8

<sup>1</sup> The high speed ADC FIFO evaluation kit can be used to evaluate two channels at a time.

<sup>2</sup> If a DEMUX BRD is needed, send an email to [highspeed.converters@analog.com](mailto:highspeed.converters@analog.com).



## THEORY OF OPERATION

The FIFO evaluation board can be divided into several circuits, each of which plays an important part in acquiring digital data from the ADC and allows the PC to upload and process that data. The evaluation kit is based around the IDT72V283 FIFO chip from Integrated Device Technology, Inc (IDT). The system can acquire digital data at speeds up to 133 MSPS and data record lengths up to 32 kB using the HSC-ADC-EVALB-SC FIFO evaluation kit. The HSC-ADC-EVALB-DC, which has two FIFO chips, is available to evaluate multichannel ADCs or demultiplexed data from ADCs sampling faster than 133 MSPS. A USB 2.0 microcontroller communicating with ADC Analyzer allows for easy interfacing to newer computers using the USB 2.0 (USB 1.1-compatible) interface.

The process of filling the FIFO chip or chips and reading the data back requires several steps. First, ADC Analyzer initiates the FIFO chip fill process. The FIFO chips are reset, using a master reset signal (MRS). The USB microcontroller is then suspended, which turns off the USB oscillator and ensures that it does not add noise to the ADC input. After the FIFO chips completely fill, the full flags from the FIFO chips send a signal to the USB microcontroller to wake up the microcontroller from suspend. ADC Analyzer waits for approximately 30 ms and then begins the readback process.

During the readback process, the acquisition of data from FIFO 1 (U201) or FIFO 2 (U101) is controlled via Signal OEA and Signal OEB. Because the data outputs of both FIFO chips drive the same 16-bit data bus, the USB microcontroller controls the OEA and OEB signals to read data from the correct FIFO chip. From an application standpoint, ADC Analyzer sends commands to the USB microcontroller to initiate a read from the correct FIFO chip, or from both FIFO chips in dual or demultiplexed mode.

### CLOCKING DESCRIPTION

Each channel of the buffer memory requires a clock signal to capture data. These clock signals are normally provided by the ADC evaluation board and are passed along with the data through Connector J104 (Pin 37 for both Channel A and Channel B). If only a single clock is passed for both channels, they can be connected together by Jumper J303.

Jumpers J304 and J305 at the output of the LVDS receiver allow the output clock to be inverted by the LVDS receiver. By default, the clock outputs are inverted by the LVDS receiver.

The single-ended clock signal from each data channel is buffered and converted to a differential CMOS signal by two gates of a low voltage differential signal (LVDS) receiver, U301. This allows the clock source for each channel to be CMOS, TTL, or ECL.

The clock signals are ac-coupled by 0.1  $\mu$ F capacitors. Potentiometer R312 and Potentiometer R315 allow for fine tuning the threshold of the LVDS gates. In applications where fine-tuning the threshold is critical, these potentiometers can be replaced with a higher resistance value to increase the adjustment range. Resistors R301, R302, R303, R304, R311, R313, R314, and R316 set the static input to each of the differential gates to a dc voltage of approximately 1.5 V.

At assembly, Solder Jumper J310 to Solder Jumper J313 are set to bypass the potentiometer. For fine adjustment using the pot, the solder jumpers must be removed, and R312 and R315 must be populated.

U302, an XOR gate array, is included in the design to let users add gate delays to the FIFO memory chip clock paths. They are not required under normal conditions and are bypassed at assembly by Jumper J314 and Jumper J315. Jumper J306 and Jumper J307 allow the clock signals to be inverted through an XOR gate. In the default setting, the clocks are not inverted by the XOR gate.

The clock paths described above determine the WRT\_CLK1 and WRT\_CLK2 signals at each FIFO memory chip (U101 and U201). The timing options above should let you choose a clock signal that meets the setup and hold time requirements to capture valid data.

A clock generator can be applied directly to S1 and/or S3. This clock generator should be the same unit that provides the clock for the ADC. These clock paths are ac-coupled, so that a sine wave generator can be used. DC bias can be adjusted by R301/R302 and R303/R304.

The DS90LV048A differential line receiver is used to square the clock signal levels applied externally to the FIFO evaluation board. The output of this clock receiver can either directly drive the write clock of the IDT72V283 FIFO(s), or first pass through the XOR gate timing circuitry described above.

### SPI DESCRIPTION

The Cypress IC (U502) supports the HSC SPI standard to allow programming of ADCs that have SPI-accessible register maps. U102 is a buffer that drives the 4-wire SPI (SCLK, SDI, SDO, CSB<sup>1</sup>) through the 120-pin connector (J104) on the third or top row. J502 is an auxiliary SPI connector to monitor the SPI signals connected directly to the Cypress IC. For more information on this and other functions, consult the user manual titled *Interfacing to High Speed ADCs via SPI* at [www.analog.com/hsc-FIFO](http://www.analog.com/hsc-FIFO).

<sup>1</sup> Note that CSB1 is the default CSB line used.

# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

The SPI interface designed on the Cypress IC can communicate with up to five different SPI-enabled devices. The CLK and data lines are common to all SPI devices. The correct device is chosen to communicate by using one of the five active low chip select pins. This functionality is controlled by selecting a SPI channel in the software.

## CLOCKING WITH INTERLEAVED DATA

ADCs with very high data rates can exceed the capability of a single buffer memory channel (~133 MSPS). These converters often demultiplex the data into two channels to reduce the rate required to capture the data. In these applications, ADC Analyzer must interleave the data from both channels to process it as a single channel. The user can configure the software to process the first sample from Channel A, the second from Channel B, and so on, or vice versa. The synchronization circuit included in the buffer memory forces a small delay between the write enable signals (WENA and WENB) to the FIFO memory chips (Pin 1, U101, and U201), ensuring that the data is captured in one FIFO before the other. Jumper J401 and Jumper J402 determine which FIFO receives WENA and which FIFO receives WENB.

## CONNECTING TO THE HSC-ADC-FPGA-4/-8

ADCs that have serial LVDS outputs require another board that is connected between the ADC evaluation board and the FIFO data capture card. This board converts the serial data into parallel CMOS so that the FIFO data capture card can accept the data. For more detailed information on this board, refer to the HSC-ADC-FPGA datasheet at [www.analog.com/hsc-FIFO](http://www.analog.com/hsc-FIFO).

## CONNECTING TO THE DEMUX BRD

ADCs that have parallel LVDS outputs require another board that is connected between the ADC evaluation board and the FIFO data capture card. This board converts parallel LVDS to parallel CMOS, using both channels of the FIFO data capture card. For more detailed information on this board, send an email to [highspeed.converters@analog.com](mailto:highspeed.converters@analog.com)

## UPGRADING FIFO MEMORY

The FIFO evaluation board includes one or two 32 kB FIFOs that are capable of 133 MHz clock signals, depending on the model number. Pin-compatible FIFO upgrades are available from IDT. See Table 2 for the IDT part number matrix.

**Table 2. IDT Part Number Matrix**

Part Number	FIFO Depth	FIFO Speed
IDT72V283-L7-5PF (Default)	32 kB	133 MHz
IDT72V293-L7-5PF	64 kB	133 MHz
IDT72V2103-L7-5PF	132 kB	133 MHz
IDT72V2113-L7-5PF	256 kB	133 MHz
IDT72V283-L6PF	32 kB	166 MHz
IDT72V293-L6PF	64 kB	166 MHz
IDT72V2103-L6PF	132 kB	166 MHz
IDT72V2113-L6PF	256 kB	166 MHz

For more information, visit [www.idt.com](http://www.idt.com).

## JUMPERS

Use the legends in Table 3 and Table 4 to configure the jumpers. On the FIFO evaluation board, Channel A is associated with the bottom IDT FIFO chip, and Channel B is associated with the top IDT FIFO chip (closest to the Analog Devices logo).

**Table 3. Jumper Legend**

Position	Description
In	Jumper in place (2-pin header).
Out	Jumper removed (2-pin header).
Position 1 or Position 3	Denotes the position of a 3-pin header. Position 1 is marked on the board.

**Table 4. Solder Jumper Legend**

Position	Description
In	Solder pads should be connected with 0 Ω resistor.
Out	Solder pads should not be connected with 0 Ω resistor.

## DEFAULT SETTINGS

Table 5 lists the default settings for each model of the FIFO evaluation kit. The single channel (SC) model is configured to work with a single channel ADC using the bottom FIFO, U201. The dual channel (DC) model is configured to work with demultiplexed ADCs (such as the AD9430). Dual channel ADC settings are shown in a separate column, as are settings for the opposite (top) FIFO, U101 for a single channel ADC. To align the timing properly, some evaluation boards require modifications to these settings. Refer to the Clocking Description section in the Theory of Operation section for more information.

Another useful way to configure the jumper settings easily for various configurations is to consult ADC Analyzer under **Help > About HSC\_ADC\_EVALB**, and click **Set Up Default Jumper Wizard**. Then click the configuration setting that applies to the application of interest. A picture of the FIFO board is displayed for that application with a visual of the correct jumper settings already in place.

**Table 5. Jumper Configurations**

Jumper #	Single Channel Settings, Default (Bottom)	Demultiplexed Settings	Dual-Channel Settings	Single-Channel Settings (Top) <sup>1</sup>	Description
J303	In	Out	Out	In	Position 2 to Position 4, ties write clocks together
J304	In	In	In	In	Position 1 to Position 2, POS3: invert clock out of DS90 (U301)
J305	In	In	In	In	Position 2 to Position 3, POS3: invert clock out of DS90 (U301)
J306	Out	Out	Out	Out	No invert to encode clock from XOR (U302), 0 Ω resistor
J307	Out	Out	Out	Out	No invert to encode clock from XOR (U302), 0 Ω resistor
J310 to J313	In	In	In	In	All solder jumpers are shorted with 0 Ω resistors (bypass level shifting to input of DS90)
J314	In	In	In	In	Position 1 to Position 2, one XOR gate timing delay for top FIFO (U101)
J315	In	In	In	In	Position 1 to Position 2, one XOR gate timing delay for bottom FIFO (U201)
J316	In	In	In	In	Power connected using switching power supply
J401	In	In	In	In	Controls if top FIFO (U101) gets write enable before or after bottom FIFO, 0 Ω resistor
J402	Out	Out	Out	Out	Controls if top FIFO (U101) gets write enable before or after bottom FIFO, 0 Ω resistor
J403	Out	Out	Out	Out	Controls if bottom FIFO (U201) gets a write enable before or after the top FIFO, 0 Ω resistor
J404	In	In	In	In	Controls if bottom FIFO (U201) gets a write enable before or after the top FIFO, 0 Ω resistor
J405	Out	In	Out	Out	When in, WRT_CLK1 is used to create write enable signal for FIFOs, 0 Ω resistor (significant only for interleave mode)

# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

Jumper #	Single Channel Settings, Default (Bottom)	Demultiplexed Settings	Dual-Channel Settings	Single-Channel Settings (Top) <sup>1</sup>	Description
J406	In	In	In	In	WRT_CLK2 is used to create write enable signal for FIFOs, 0 $\Omega$ resistor (significant only for interleave mode)
J503	In	In	In	In	Connect enable empty flag of top FIFO (U101) to USB MCU, 0 $\Omega$ resistor
J504	Out	Out	Out	Out	N/A
J505	In	In	In	In	Connect enable full flag of top FIFO (U101) to USB MCU, 0 $\Omega$ resistor
J506	Out	Out	Out	Out	N/A
J602	Out	Out	Out	Out	N/A
J603	In	In	In	In	N/A

<sup>1</sup> Some jumpers can be a 0  $\Omega$  resistor instead of a physical jumper. This is shown in Table 5 in the jumper description column.

## EVALUATION BOARD

The FIFO provides all of the support circuitry required to accept two channels of an ADC's digital parallel CMOS outputs. Each of the various functions and configurations can be selected by proper connection of various jumpers (see Table 5). When using this in conjunction with an ADC evaluation board, it is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the ultimate performance of the converter. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 5 to Figure 15 for complete schematics and layout plots.

## POWER SUPPLIES

The FIFO board is supplied with a wall mount switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to the rated 100 ac to 240 ac wall outlet at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at J301. On the PC board, the 6 V supply is then fused and conditioned before connecting to the low dropout 3.3 V linear regulator that supplies the proper bias to the entire board.

When operating the evaluation board in a non-default condition, J316 can be removed to disconnect the switching power supply. This enables the user to bias the board independently. Use P302 to connect an independent supply to the board. A 3.3 V supply is needed with at least a 1 A current capability.

## CONNECTION AND SETUP

The FIFO board has a 120-pin (40-pin, triple row) connector that accepts two 16-bit channels of parallel CMOS inputs (see Figure 6). For those ADC evaluation boards that have only an 80-pin (40-pin, double row) connector, it is pertinent for the lower two rows of the FIFO's triple row connector to be connected in order for the data to pass to either FIFO channel correctly. The top or third row is used to pass SPI signals across to the adjacent ADC evaluation board that supports this feature.

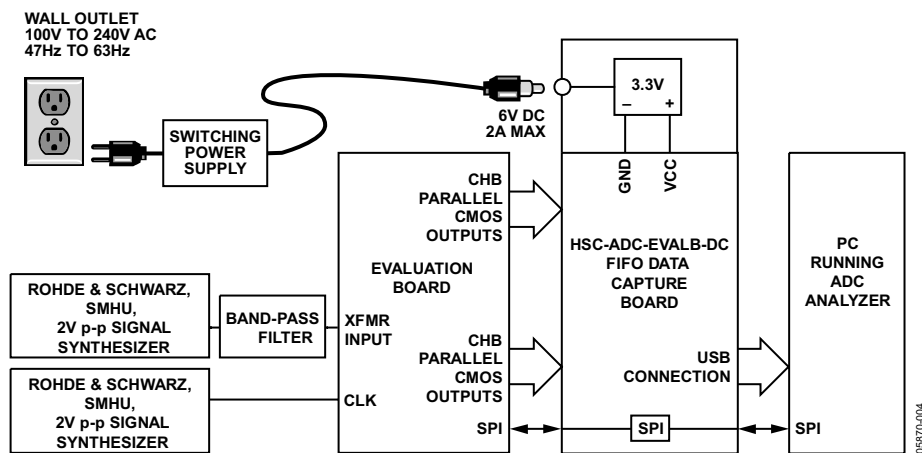


Figure 4. Example Setup Using Quad ADC Evaluation Board and FIFO Data Capture Board



# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

## FIFO SCHEMATICS AND PCB LAYOUT

### SCHEMATICS

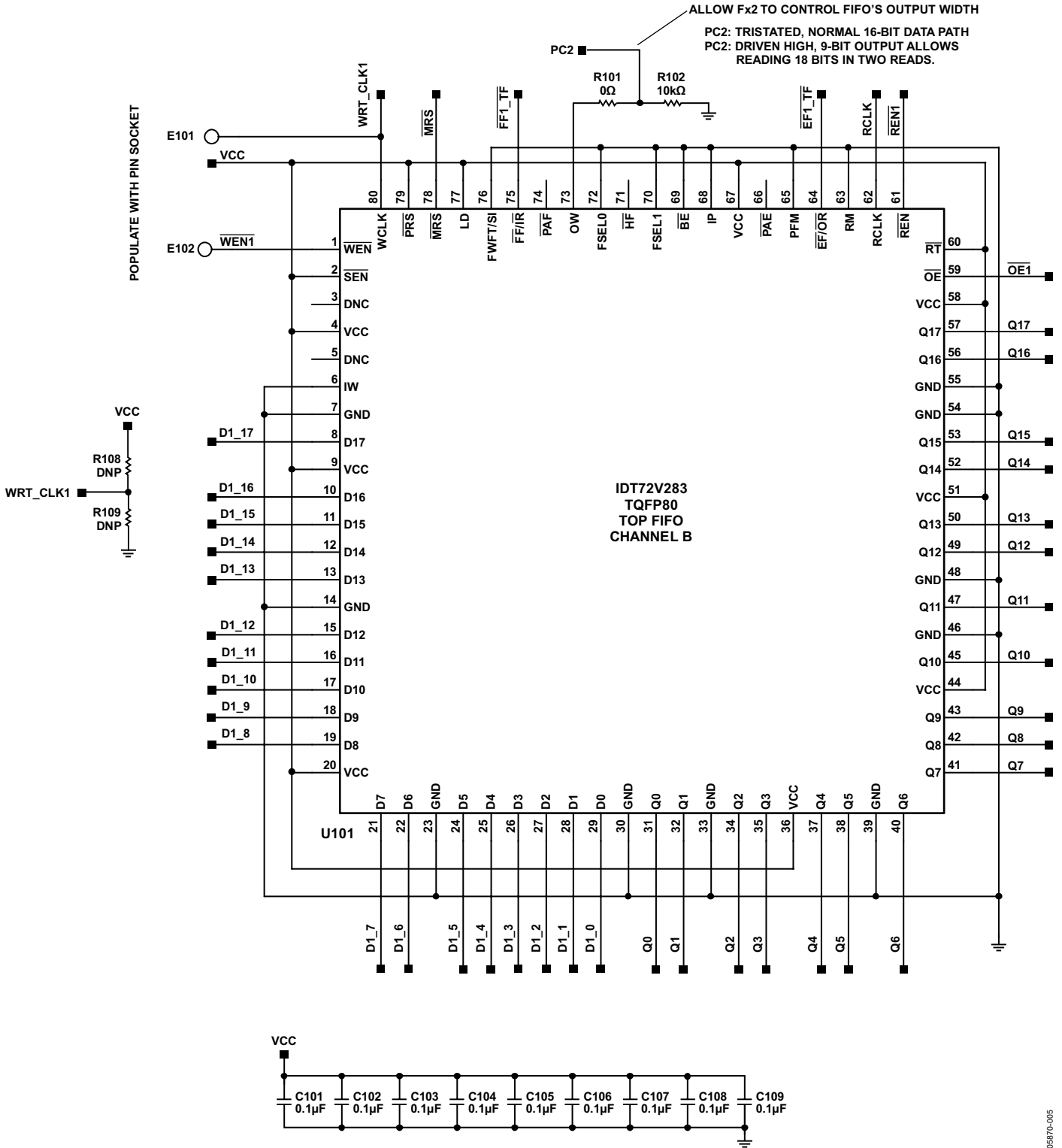


Figure 5. PCB Schematic

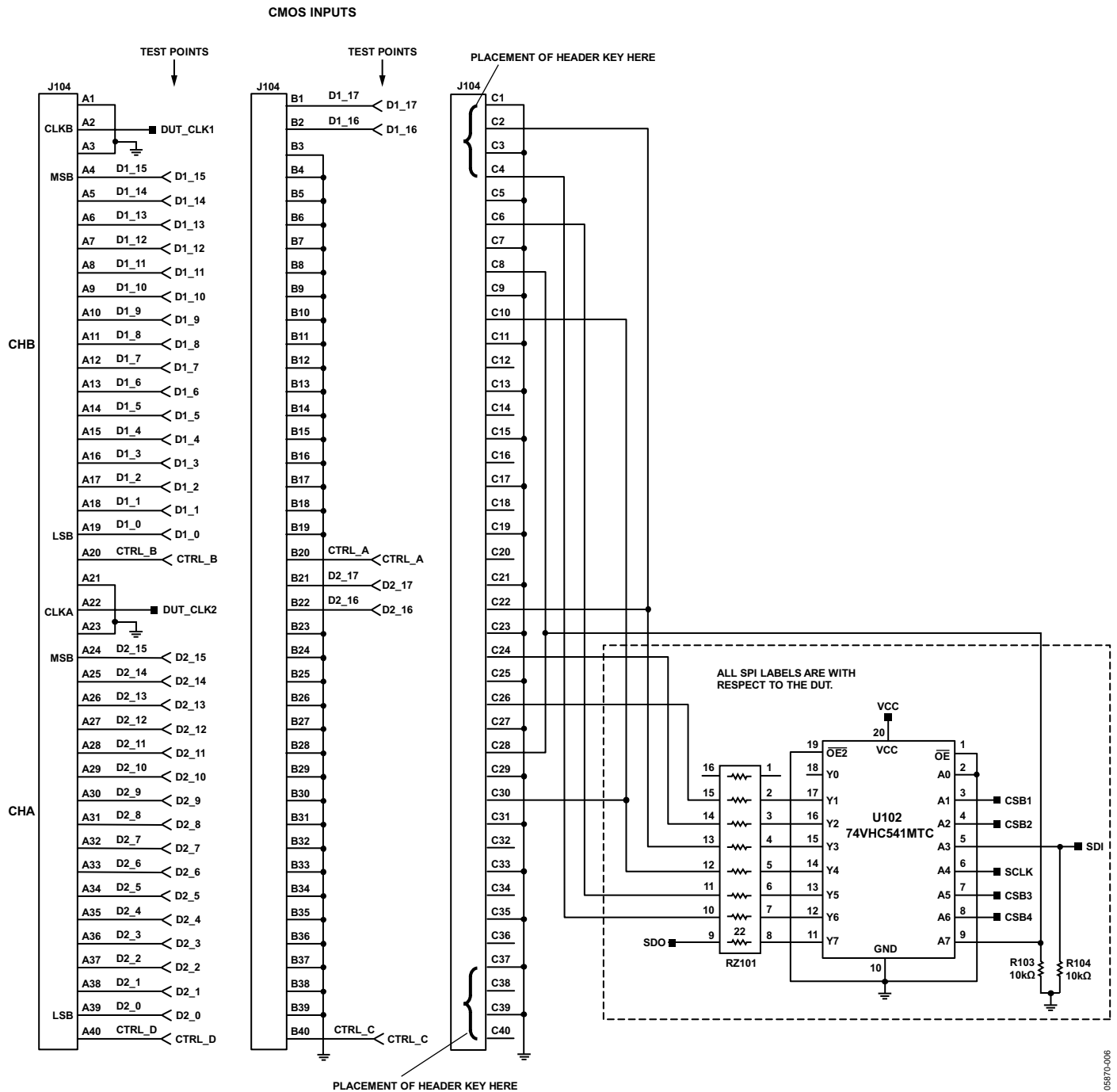


Figure 6. Schematic (Continued)

# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

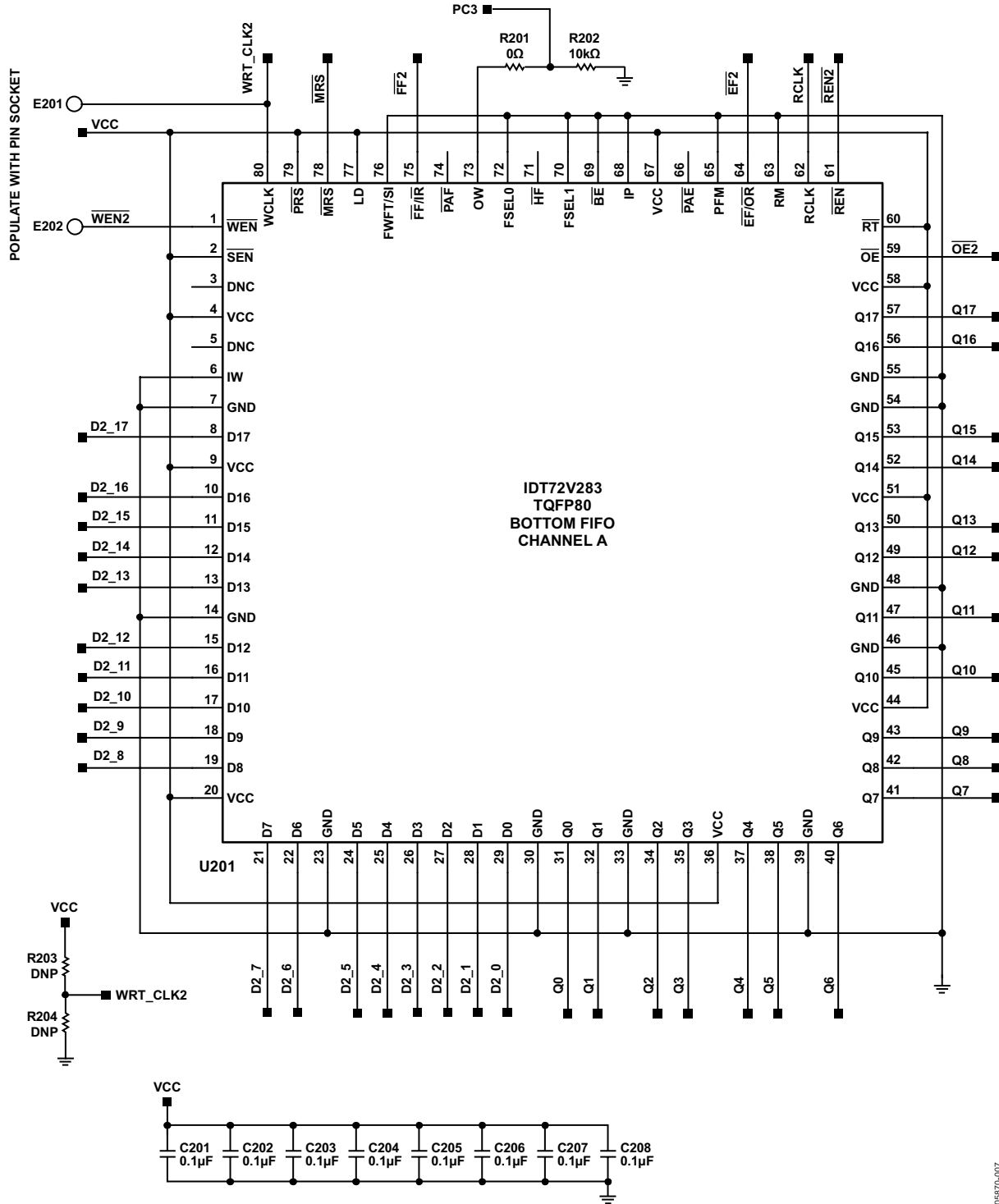


Figure 7. Schematic (Continued)

05870-007

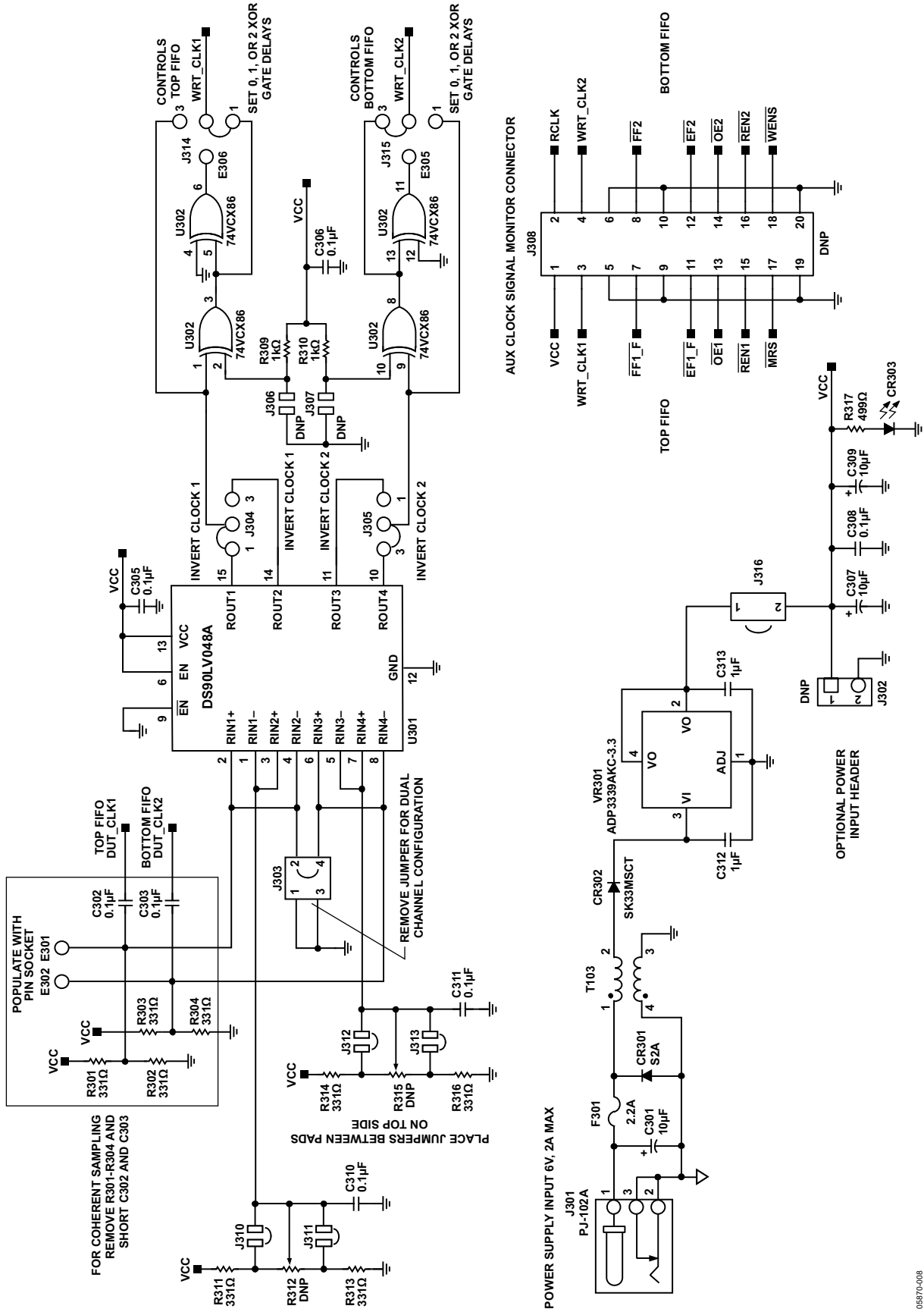


Figure 8. Schematic (Continued)

# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

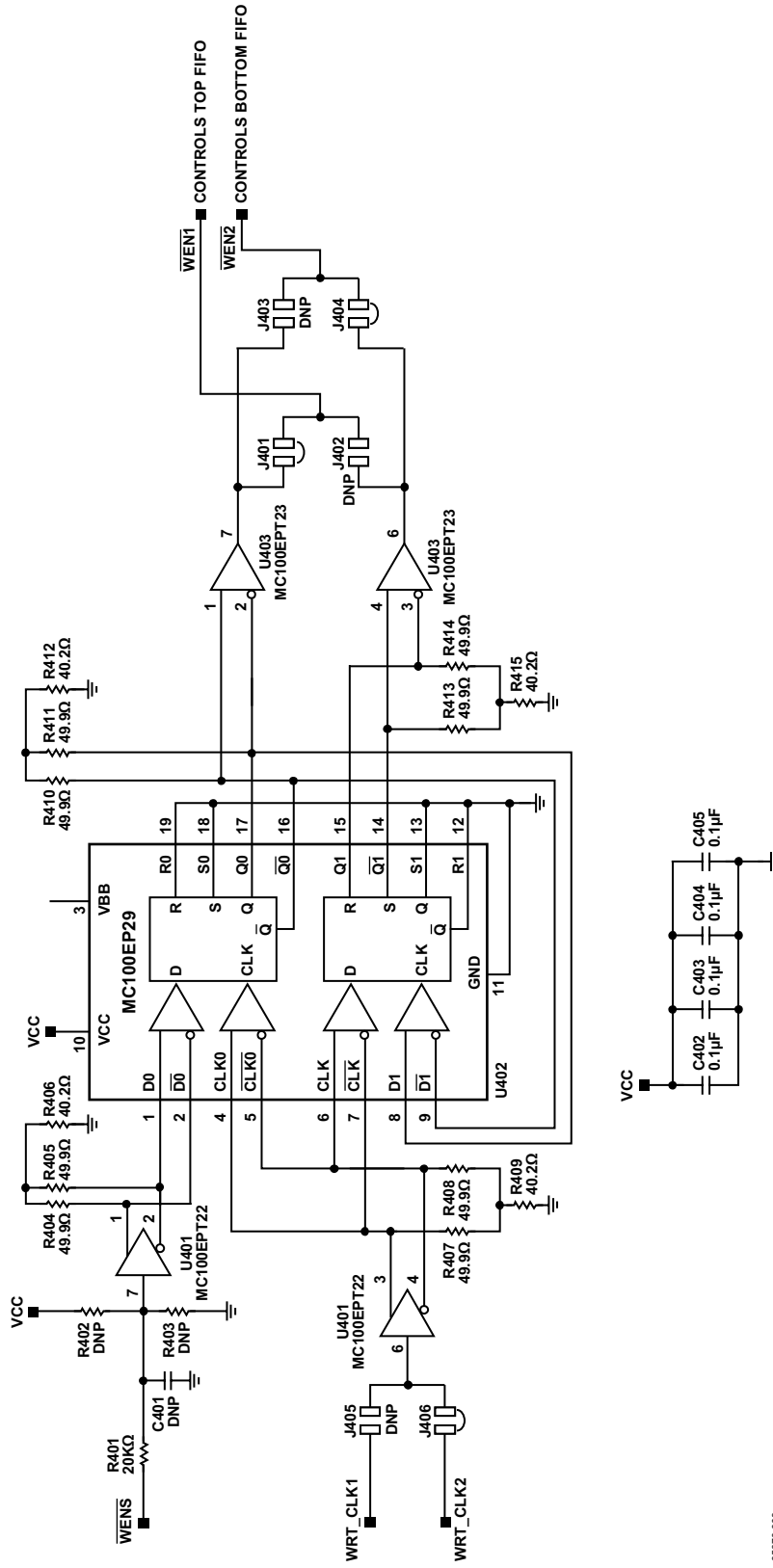


Figure 9. Schematic (Continued)

05670-009



# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

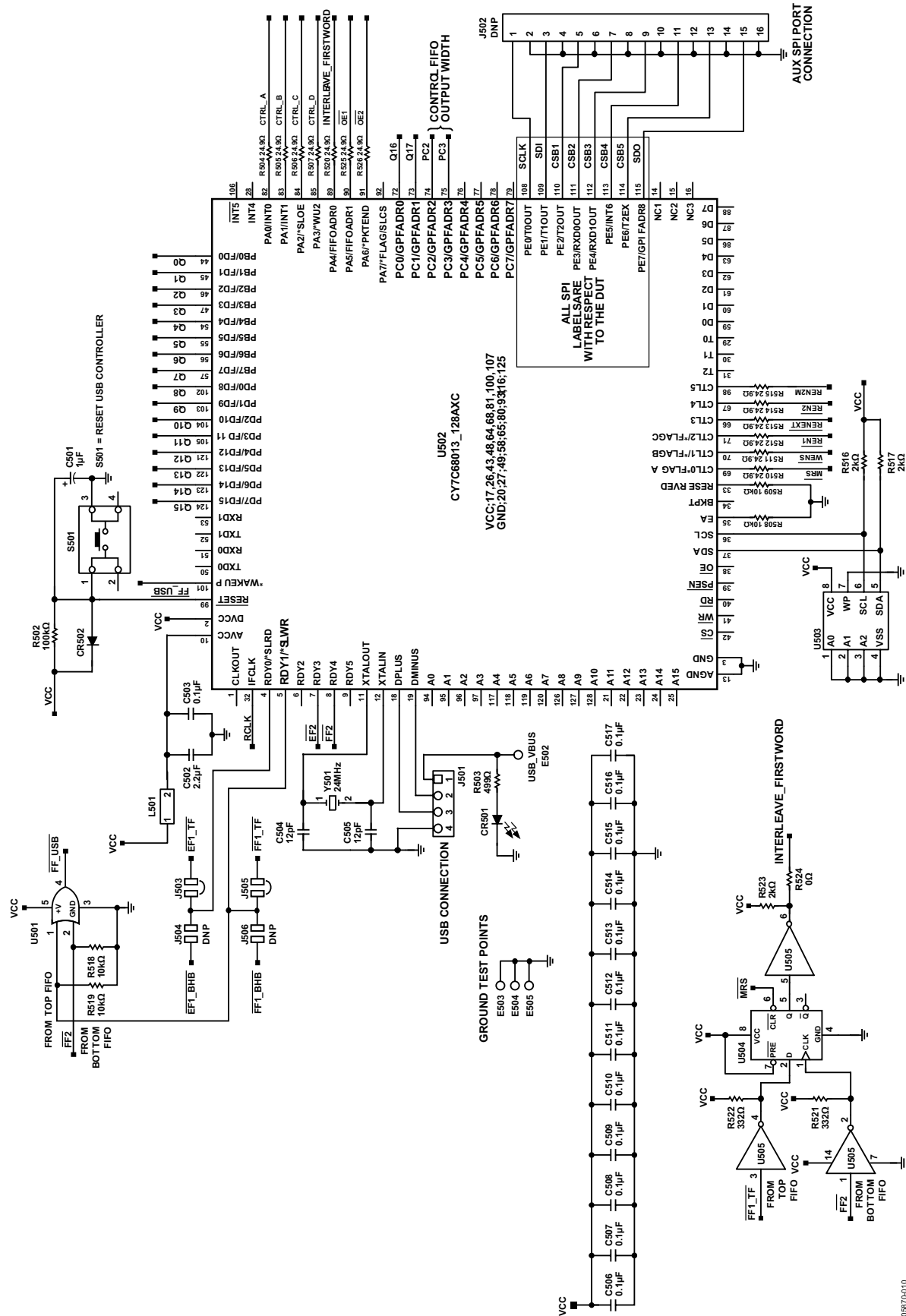
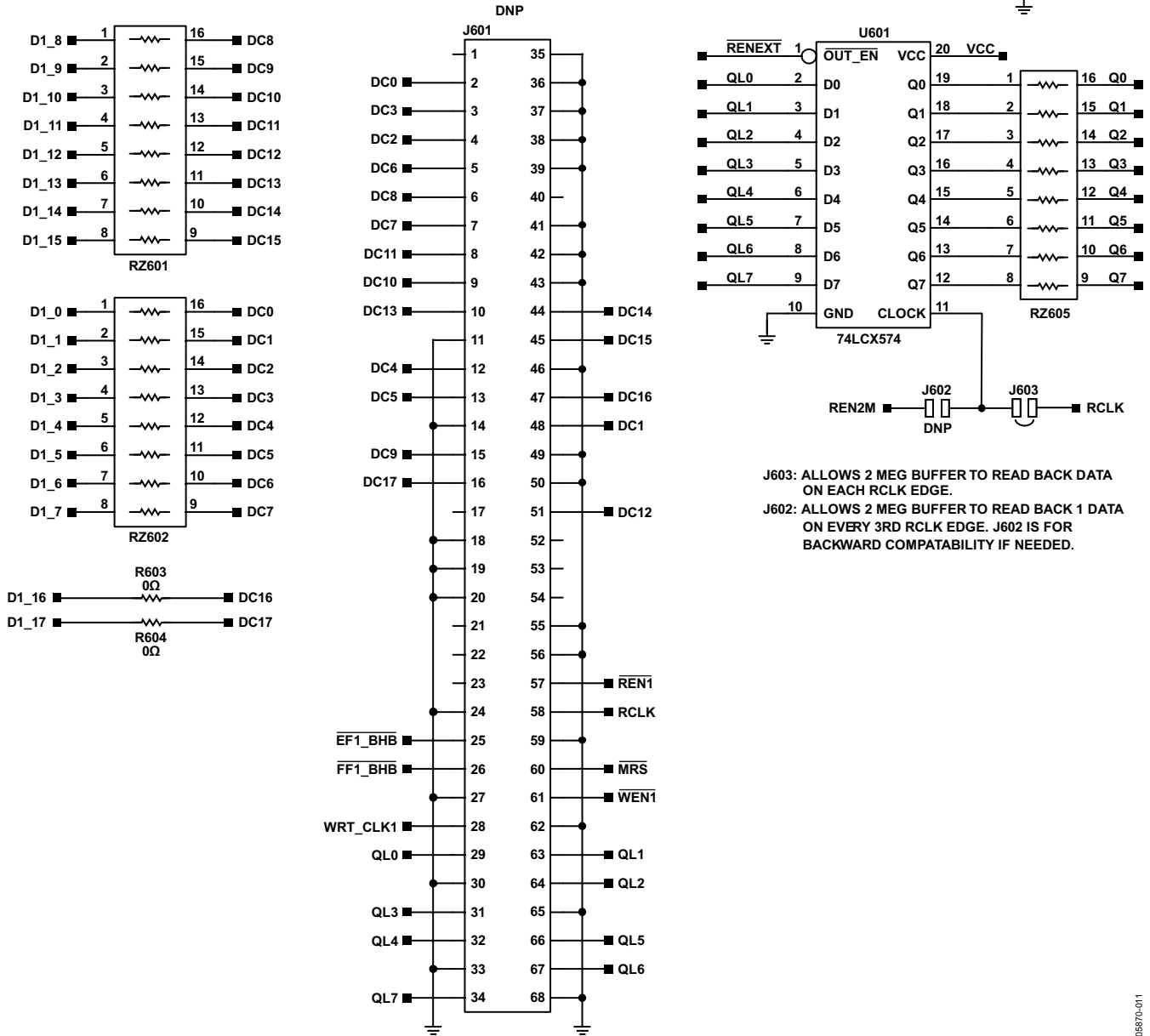
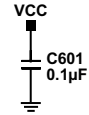


Figure 10. Schematic (Continued)

# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

CONNECTIONS FOR 2M WORD EXTERNAL MEMORY  
EXTERNAL MEMORY OVERRIDES ON BOARD MEMORIES WHEN PLUGGED IN. ONLY A SIDE DATA.



J603: ALLOWS 2 MEG BUFFER TO READ BACK DATA ON EACH RCLK EDGE.  
J602: ALLOWS 2 MEG BUFFER TO READ BACK 1 DATA ON EVERY 3RD RCLK EDGE. J602 IS FOR BACKWARD COMPATABILITY IF NEEDED.

Figure 11. Schematic (Continued)

05870-011



# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

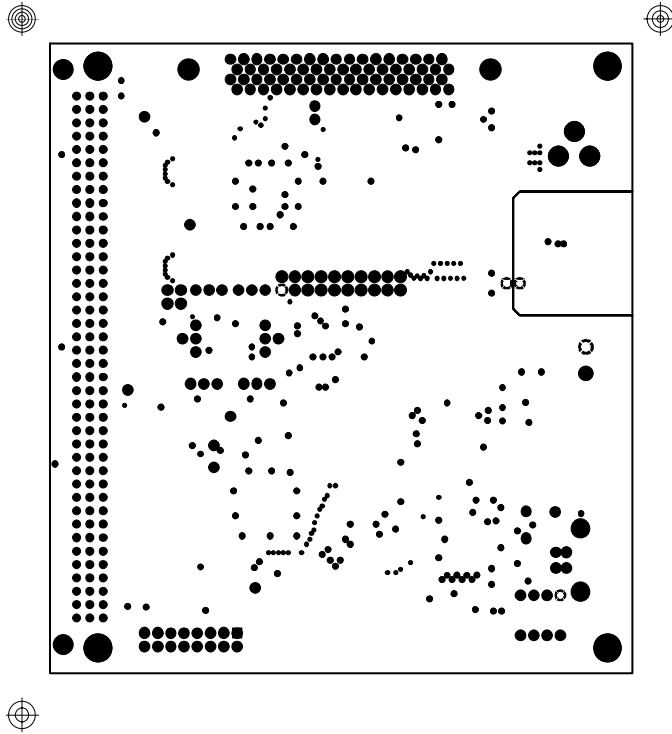


Figure 14. Layer 3—Power Plane

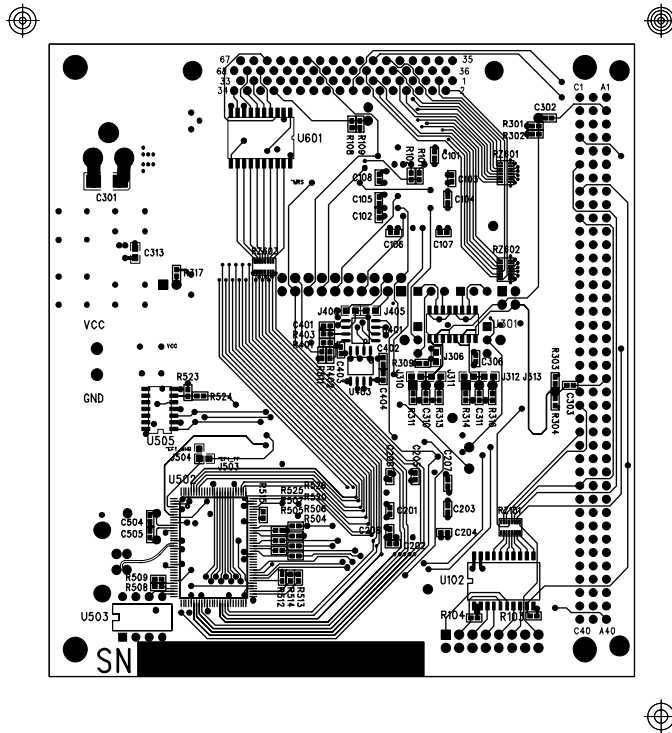


Figure 15. Layer 4—Secondary Side

# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

## BILL OF MATERIALS

Table 6. HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC Bill of Materials

Item	Qty	Reference Designation	Device	Package	Description	Manufacturer	Mfg Part Number
1	42	C101 to C109, C201 to C208, C302, C303, C305, C306, C308, C310, C311, C402 to C405, C503, C506 to C517, C601	Capacitor	402	Ceramic, 0.1 $\mu$ F, 16 V, X5R, 10%	Panasonic	ECJ-0EB1C014K
2	3	C301, C307, C309	Capacitor	6032-28	Tantalum, 10 $\mu$ F, 16 V, 10%	Kemet	T491C106K016AS
3	2	C312, C313	Capacitor	603	Ceramic, 1 $\mu$ F, 10 V, X5R, 10%	Panasonic	ECJ-1VB1A105K
4	1	C501	Capacitor	3216-18	Tantalum, 1 $\mu$ F, 16 V, 20%	Panasonic	ECS-T1CY105R
5	1	C502	Capacitor	805	Ceramic, 2.2 $\mu$ F, 25 V, X5R 10%	Panasonic	ECJ-2FB1E225K
6	2	C504, C505	Capacitor	402	Ceramic, 12 pF, NPO, 50 V, 5%	Panasonic	ECJ-0EC1H120J
7	1	CR301	Diode	DO-214AA	Schottky diode, 50 V, 2 A, SMC	Micro Commercial Group	S2A
8	1	CR302	Diode	DO-214AB	Schottky diode, 30 V, 3 A, SMC	Micro Commercial Group	SK33MSCT
9	2	CR303, CR501	LED	603	Green, 4 V 5 m, candela	Panasonic	LNJ314G8TRA
10	1	CR502	Diode	SOD-123	Switching, 75 V, 150 mA	Diodes, Inc.	1N4148W-7
11	1	F301	Fuse	1210	6.0 V, 2.2 A trip current resettable fuse	Tyco, Raychem	NANOSMDC110F-2
12	1	J104	Connector		120-pin, female, PC mount, right angle	AMP	650874
13	1	J301	Connector	0.08", PCMT	RAPC722, power supply connector	Switchcraft	SC1153
14	1	J303	Connector	4-pin	Male, straight, 100 mil	SAMTEC	TSW-1-10-08-GD
15	4	J304, J305, J314, J315	Connector	3-pin	Male, straight, 100 mil	SAMTEC	TWS-103-08-G-S
16	8	J310 to J313, J401, J404, J406, J603	Connector	603	2-pin solder jumper, 0 $\Omega$ , 1/10 W, 5%	Panasonic	ERJ-3GEY0R00V
17	1	J316	Connector	2-pin	Male, straight, 100 mil	SAMTEC	TSW-1002-08-G-S
18	1	J501	Connector	4-pin	USB, PC mount, right angle, Type B, female	AMP	787780-1
19	1	L501	Ferrite Bead	805	500 mA, 600 $\Omega$ @ 100 MHz	Steward	HZ0805E601R-00
20	5	R101, R201, R524, R603, R604	Resistor	402	0 $\Omega$ , 1/16 W, 5%	Panasonic	ERJ-2GE0R00X
21	8	R102 to R04, R202, R508, R509, R518, R4519	Resistor	402	10 k $\Omega$ , 1/16 W, 1%	Panasonic	ERJ-2RKF1002X
22	10	R301 to R304, R311, R313, R314, R316, R521, R522	Resistor	402	332 $\Omega$ , 1/16 W, 1%	Panasonic	ERJ-2RKF3320X
23	2	R309, R310	Resistor	402	1 k $\Omega$ , 1/16 W, 1%	Panasonic	ERJ-2RKF1002X
24	2	R317, R503	Resistor	402	499 $\Omega$ , 1/16 W, 1%	Panasonic	ERJ-2RKF1001X
25	1	R401	Resistor	402	20 k $\Omega$ , 1/16 W, 1%	Panasonic	ERJ-2RKF4990X
26	8	R404, R405, R407, R408, R410, R411, R413, R414	Resistor	402	49.9 $\Omega$ , 1/16 W, 1%	Panasonic	ERJ-2RKF2002X
27	4	R406, R409, R412, R415	Resistor	402	40.2 $\Omega$ , 1/16 W, 1%	Panasonic	ERJ-2RKF40R2X
28	1	R502	Resistor	402	100 k $\Omega$ , 1/16 W, 1%	Panasonic	ERJ-2RKF1003X
29	13	R504, R506, R507, R510 to R515, R520, R525, R526	Resistor	402	24.9 $\Omega$ , 1/16 W, 1%	Panasonic	ERJ-2RKF24R9X
30	3	R516, R517, R523	Resistor	402	2 k $\Omega$ , 1/16 W, 1%	Panasonic	ERJ-2RKF2001X
31	1	RZ101	Resistor		Resistor array, 22 $\Omega$ , 1/4 W, 5%	Panasonic	EXB-2HV220JX
32	1	S501	Switch		Momentary (normally open), 100 GE, 5 mm, SPST	Panasonic	EVQ-PLDA15



# HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC

Item	Qty	Reference Designation	Device	Package	Description	Manufacturer	Mfg Part Number
33	1	T301	Choke	2020	10 $\mu$ H, 5 A, 50 V, 190 $\Omega$ @ 100 MHz	Murata	DLW5BSN191SQ2L
34 <sup>1</sup>	2	U101, U201	IC	TQFP80	3.3 V, IDT72V283L7-5PF	IDT	IDT72V283L7-5PF
35	1	U102	IC	SOIC20	74VHC541, octal buffer/line driver, three-state	Fairchild	74VHC541M
36	1	U301	IC	SOIC16	DS90LV048A	National Semiconductor	DS90LV048A
37	1	U302	IC	SOIC14	74VCX86	Fairchild	74VCX86
38	1	U401	IC	SO8M1	MC100EPT22D	Motorola	MC100EPT22D
39	1	U402	IC	TSSOP20	MC100EP29DT	ON Semiconductor	MC100EP29DT
40	1	U403	IC	SO8M1	MC100EPT23D	Motorola	MC100EPT23D
41	1	U501	IC	SOT23L5	NC7SZ32M5, NC7SZ32, tiny log UHS 2-input or gate	Fairchild	NC7SZ32M5
42	1	U502	IC	TQFP128	CY7C68013	Cypress	CY7C68013-128AXC or CY7C68014A-128AXC
43	1	U503	IC	DIP8	24LC00P	Microchip	24LC00P
44	1	U504	IC	DCT_8PIN_06, 5 mm	SN74LVC2G74DCTR, D-type flip-flop, DCT_8PIN_0.65MM	Texas Instruments	SN74LVC2G74DCTR
45	1	U505	IC	SOIC 14	74LVQ04SC, low voltage hex inverter	Fairchild	74LVQ04SC
46	1	U601	IC	DIP20/SOL	74LCX574WM-ND, 74LCX574 octal D-type flip-flop	Fairchild	74LCX574WM-ND
47	1	VR301	IC	SOT-223HS	High accuracy, ADP3339AKC-3.3, 3.3 V	Analog Devices	ADP3339AKC-3.3
48	1	Y501	Crystal	Crystal	Oscillator, 24 MHz	Ecliptek	EC-12-24.000M
49	6	See schematic for placement	Connector	100 mil jumper	0.1" jumpers	Samtec	SNT-100-BK-G-H
50	4	Insert from bottom side of board	Standoff	Plastic mount standoffs	7/8" height, standoffs	Richco	CBSB-14-01A-RT
51	2	See schematic for placement	Connector	Third-row header key	These header inserts for J104, Pin 81, and Pin 120 are located on the edges of the top row	Samtec	TSW-104-07-T-S

<sup>1</sup> Only U201 is populated for the single-channel version (HSC-ADC-EVALB-SC).

## ORDERING INFORMATION

### ORDERING GUIDE

Model	Description
HSC-ADC-EVALB-SC	Single FIFO Version of USB Evaluation Kit
HSC-ADC-EVALB-DC	Dual FIFO Version of USB Evaluation Kit
HSC-ADC-FPGA-4/-8	Quad/Octal Serial LVDS to Dual Parallel CMOS Interface; supports all Quad/Octal ADCs in this family except the AD9289 (not Included in Evaluation Kit)
HSC-ADC-FPGA-9289	Quad Serial LVDS to Dual Parallel CMOS Interface for the AD9289 Only (Not Included in Evaluation Kit)
AD922XFFA <sup>1</sup>	Adapter for AD922x Family (Not Included in Evaluation Kit)
AD9283FFA <sup>1</sup>	Adapter for the AD9283 and AD9057 (Not Included in Evaluation Kit)
AD9059FFA <sup>1</sup>	Adapter for the AD9059 (Not Included in Evaluation Kit)
AD9051FFA <sup>1</sup>	Adapter for the AD9051 (Not Included in Evaluation Kit)
LG-0204A <sup>1</sup>	Adapter for the AD10xxx and AD13xxx Families (Not Included in Evaluation Kit)

<sup>1</sup> If an adapter is needed, send an email to [highspeed.converters@analog.com](mailto:highspeed.converters@analog.com).

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



**NOTES**

**NOTES**

**NOTES**