MCRF355

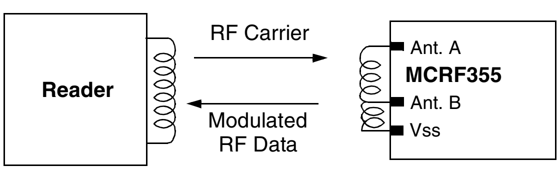
13.56 MHz Passive RFID Device with Anti-Collision Feature

Features

- Carrier frequency: 13.56 MHz
- Data modulation frequency: 70 kHz
- Manchester coding protocol
- 154 bits of user memory
- On-board 100 ms SLEEP timer
- Built-in anti-collision algorithm for reading up to multiple tags in the same RF field
- "Cloaking" feature to minimize the detuning effects of adjacent tags
- Read only device in RF field
- Long read range
- Rewritable with contact programmer
- Factory-programmed options
- Very low-power CMOS design
- Die, wafer, wafer-on-frame, PDIP or SOIC package options

Applications

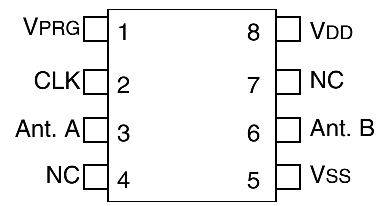
- Book store and library book ID
- Airline baggage tracking
- Toys and games
- Access control/asset tracking
- Applications for reading multiple tags and long read range



Read range: ~ up to 1.5 meters depending on tag size and system design.

Package Type

PDIP/SOIC



Note: Pins 1, 2, 5 and 8 are for device testing and contact programming.

Pins 3, 5 and 6 are for external antenna connection.

NC = Not connected

MCRF355 may be ordered blank or factory-programmed with a unique serial number, header and checksum. Microchip's format is further defined in TB031.

Description

The MCRF355 is Microchip's uniquely designed read-only passive Radio Frequency Identification (RFID) device with an advanced anti-collision feature. It is programmable with a contact programmer or factory programming only. The device is powered remotely by rectifying RF magnetic fields that are transmitted from the reader.

The device has a total of six pads (see Figure 1-1). Three (ant. A, ant. B, V_{SS}) are used to connect the external resonant circuit elements. The additional three pads (V_{PRG}, CLK, V_{DD}) are used for programming and testing of the device.

The device needs an external resonant circuit between antenna A, B, and V_{SS} pads. The resonant frequency of the circuit is determined by the circuit elements between the antenna A and V_{SS} pads. The resonant circuit must be tuned to the carrier frequency of the reader for maximum performance. The circuit element between the antenna B and V_{SS} pads is used for data modulation. See Application Note AN707 for further operational details. Examples of the resonant circuit configuration for the MCRF355 are shown in Section 3.0.

When a tag (device with the external LC resonant circuit) is brought to the reader's RF field, it induces an RF voltage across the LC resonant circuit. The device rectifies the RF voltage and develops a DC voltage. The device becomes functional as soon as V_{DD} reaches the operating voltage level.

The device includes a modulation transistor that is located between antenna B and V_{SS} pads. The transistor has high turn-off (a few MΩ) and low turn-on (3 Ω) resistance. The turn-on resistance is called modulation resistance (R_M). When the transistor turns off, the resonant circuit is tuned to the carrier frequency of the reader. This condition is called uncloaking. When the modulation transistor turns on, its low turn-on resistance shorts the external circuit element between antenna B and V_{SS}. As a result, the resonant circuit no longer resonates at the carrier frequency. This is called cloaking.

The induced voltage amplitude (on the resonant circuit) changes with the modulation data: higher amplitude during uncloaking (tuned), and lower amplitude during cloaking (detuned). This is called "amplitude modulation" signal. The receiver channel in the reader detects this amplitude modulation signal and reconstructs the modulation data.

The occurrence of the cloaking and uncloaking of the device is controlled by the modulation signal that turns the modulation transistor on and off, resulting in communication from the device to the reader.

The data stream consists of 154 bits of Manchester-encoded data at a 70 kHz rate. The Manchester code waveform is shown in Figure 2-2. After completion of the data transmission, the device goes into SLEEP mode for about 100 ms. The device repeats the transmitting and SLEEP cycles as long as it is energized. During the SLEEP time, the device remains in an uncloaked state.

SLEEP time is determined by a built-in, low-current timer. There is a wide variation of the SLEEP time between each device. This wide variation of SLEEP time results in a randomness of the time slot. Each device wakes up and transmits its data in a different time slot with respect to each other. Based on this scenario, the reader is able to read many tags that are in the same RF field.

The device has a total of 154 bits of reprogrammable memory. All bits are reprogrammable by a contact programmer. A contact programmer (part number PG103003) is available from Microchip Technology Inc. Factory programming prior to shipment, known as Serialized Quick Turn Programming[SM] (SQTP[SM]), is also available. The device is available in die, wafer, wafer-on-frame, PDIP and SOIC packages.

Note:	Information provided herein is subject to change without notice.

1.0 ELECTRICAL CHARACTERISTICS

TABLE 1-1: ABSOLUTE RATINGS

Parameters	Symbol	Min	Max	Units	Conditions
Coil Current	I_{PP_AC}	—	40	mA	Peak-to-Peak coil current
Assembly temperature	T_{ASM}	—	265	°C	< 10 sec
Storage temperature	T_{STORE}	-65	150	°C	—

TABLE 1-2: DC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	**Commercial (C): T_{AMB} = -20°C to 70°C**					
Parameters	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Reading voltage	V_{DDR}	2.4	—	—	V	V_{DD} voltage for reading
Hysteresis voltage	V_{HYST}	—	TBD	—	TBD	—
Operating current	I_{DDR}	—	7	10	µA	V_{DD} = 2.4V during reading at 25°C
Testing voltage	V_{DDT}	—	4	—	V	—
Programming voltage: High level input voltage Low level input voltage High voltage	 V_{IH} V_{IL} V_{HH}	 0.7 * V_{DDT} — —	 — — 20	 — 0.3 * V_{DDT} —	 V V V	External DC voltage for programming and testing
Current leakage during SLEEP time	I_{DD_OFF}	—	10	—	nA	**(Note 1)**
Modulation resistance	R_M	—	3	4	Ω	DC resistance between Drain and Source gates of the modulation transistor (when it is turned on)
Pull-Down resistor	R_{PDW}	5	8	—	kΩ	CLK and V_{PRG} internal pull-down resistor

Note 1: This parameter is not tested in production.

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	Commercial (C): T_{AMB} = -20°C to 70°C					
Parameters	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Carrier frequency	F_C		13.56		MHz	Reader's transmitting frequency
Modulation frequency	F_M	58	70	82	kHz	Manchester coding, at V_{DD} = 2.6 V_{DC} - 5 V_{DC}
Coil voltage during reading	V_{PP_AC}	4	—	—	V_{PP}	Peak-to-Peak AC voltage across the coil during reading
Coil clamp voltage	V_{CLMP_AC}	—	32	—	V_{PP}	Peak-to-Peak coil clamp voltage
Test mode clock frequency	F_{CLK}		115	500	kHz	25°C
SLEEP time	T_{OFF}	50	100	200	ms	Off time for anti-collision feature, at 25°C and V_{DD} = 2.5 V_{DC}
Write/Erase pulse width	T_{WC}	—	2	10	ms	Time to program bit, at 25°C
Clock high time	T_{HIGH}	—	4.4	—	µs	25°C for testing and programming
Clock low time	T_{LOW}	—	4.4	—	µs	25°C for testing and programming
STOP condition pulse width	$T_{PW:STO}$	—	1000	—	ns	25°C for testing and programming
STOP condition setup time	$T_{SU:STO}$	—	200	—	ns	25°C for testing and programming
Setup time for high voltage	$T_{SU:HH}$	—	800	—	ns	25°C for testing and programming
High voltage delay time	$T_{DL:HH}$	—	800	—	ns	Delay time before the next clock, at 25°C for testing and programming
Data input setup time	$T_{SU:DAT}$	—	450	—	ns	25°C for testing and programming
Data input hold time	$T_{HD:DAT}$	—	1.2	—	µs	25°C for testing and programming
Output valid from clock	T_{AA}	—	200	—	ns	25°C for testing and programming
Data retention	—	200		—	Years	For T < 120°C

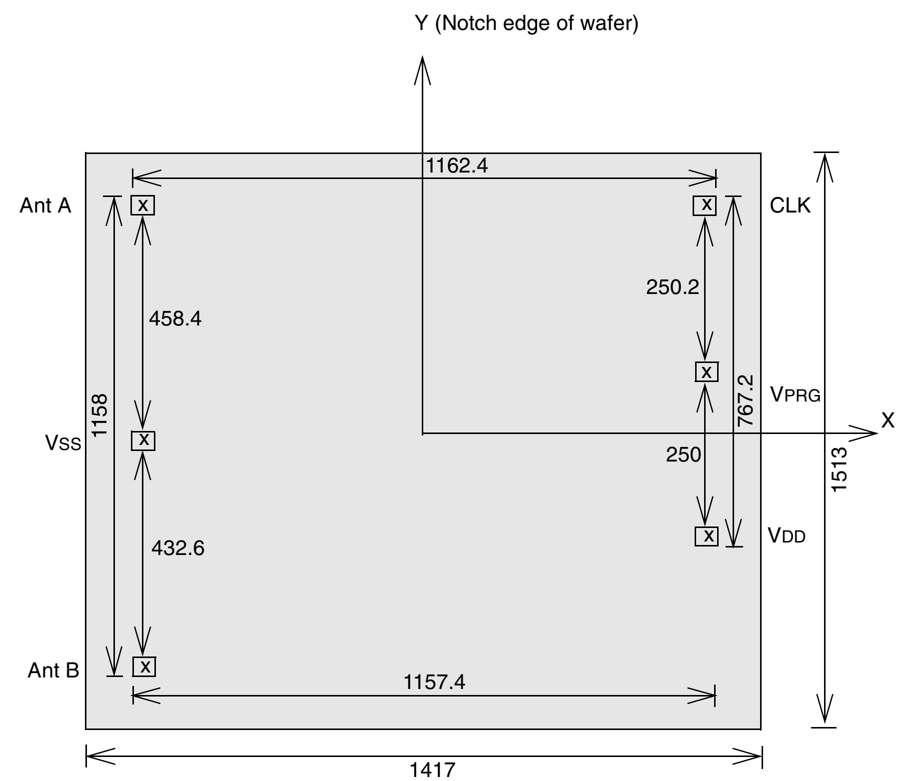
TABLE 1-4: PAD COORDINATES (MICRONS)

Pad Name	Lower Left X	Lower Left Y	Upper Right X	Upper Right Y	Passivation Openings		Pad Center X	Pad Center Y
					Pad Width	Pad Height		
Ant. A	-610.0	489.2	-521.0	578.2	89	89	-565.5	533.7
Ant. B	-605.0	-579.8	-516.0	-490.8	89	89	-560.5	-535.3
VSS	-605.0	-58.2	-516.0	30.8	89	89	-560.5	-13.7
VDD	463.4	-181.4	552.4	-92.4	89	89	507.9	-136.9
CLK	463.4	496.8	552.4	585.8	89	89	507.9	541.3
VPRG	463.4	157.6	552.4	246.6	89	89	507.9	202.1

Note 1: All coordinates are referenced from the center of the die. The minimum distance between pads (edge to edge) is 10 mil.

2: Die Size = 1.417 mm x 1.513 mm = 1417 µm x 1513 µm = 55.79 mil x 59.57 mil

FIGURE 1-1: DIE LAYOUT



Die size before saw:
1417 µm x 1513 µm
55.79 mil x 59.57 mil

Die size after saw:
1353.8 µm x 1450.34 µm
53.3 mil x 57.1 mil

Bond pad size:
89 µm x 89 µm
3.5 mil x 3.5 mil

TABLE 1-5: PAD FUNCTION TABLE

Name	Function
Ant. A	Connected to external resonant circuit, **(Note 1)**
Ant. B	Connected to external resonant circuit, **(Note 1)**
VSS	Connected to external resonant circuit, **(Note 1)** Device ground during Test mode
VDD	DC voltage supply for programming and Test mode
CLK	Main clock pulse for programming and Test mode
VPRG	Input/Output for programming and Test mode

Note 1: See Figure 3-1 for the connection with external resonant circuit.

TABLE 1-6: DIE MECHANICAL DIMENSIONS

Specifications	Min.	Typ.	Max.	Unit	Comments
Wafer Diameter	—	8	—	inch	
Die separation line width	—	80	—	µm	
Dice per wafer	—	12,000	—	die	
Batch size	—	24	—	wafer	
Bond pad opening	— —	3.5 x 3.5 89 x 89	— —	mil µm	**(Note 1, Note 2)**
Die back grind thickness	7.5 190.5	8 203.2	8.5 215.9	mil µm	Sawed 8” wafer on frame (option = WF) **(Note 3)**
	10 254	11 279.4	12 304.8	mil µm	• Bumped, sawed 8” wafer on frame (option = WFB) • Unsawed wafer (option = W) • Unsawed 8” bumped wafer (option = WB), **(Note 3)**
Die passivation thickness (multilayer)	—	1.3	—	µm	**(Note 4)**
Die Size: Die size X*Y before saw (step size) Die size X*Y after saw	 — —	 55.79 x 59.57 53.3 x 57.1	 — —	 mil mil	 — —

Note 1: The bond pad size is that of the passivation opening. The metal overlaps the bond pad passivation by at least 0.1 mil.
2: Metal pad composition is 98.5% aluminum with 1% Si and 0.5% Cu.
3: As the die thickness decreases, susceptibility to cracking increases. It is recommended that the die be as thick as the application will allow.
4: The die passivation thickness (1.3 µm) can vary by device depending on the mask set used.
- Layer 1: Oxide (undoped oxide)
- Layer 2: PSG (doped oxide)
- Layer 3: Oxynitride (top layer)

Note: Extreme care is urged in the handling and assembly of die products since they are susceptible to mechanical and electrostatic damage.

2.0 FUNCTIONAL DESCRIPTION

The device contains three major sections: (1) analog front-end, (2) controller logic and (3) memory. Figure 2-1 shows the block diagram of the device.

2.1 Analog Front-End Section

This section includes power supply, Power-on Reset, and data modulation circuits.

2.1.1 POWER SUPPLY

The power supply circuit generates DC voltage (V_{DD}) by rectifying induced RF coil voltage. The power supply circuit includes high-voltage clamping diodes to prevent excessive voltage development across the antenna coil.

2.1.2 POWER-ON-RESET (POR)

This circuit generates a Power-on Reset when the tag first enters the reader field. The RESET releases when sufficient power has developed on the V_{DD} regulator to allow for correct operation.

2.1.3 DATA MODULATION

The data modulation circuit consists of a modulation transistor and an external LC resonant circuit. The external circuit must be tuned to the carrier frequency of the reader (i.e., 13.56 MHz) for maximum performance.

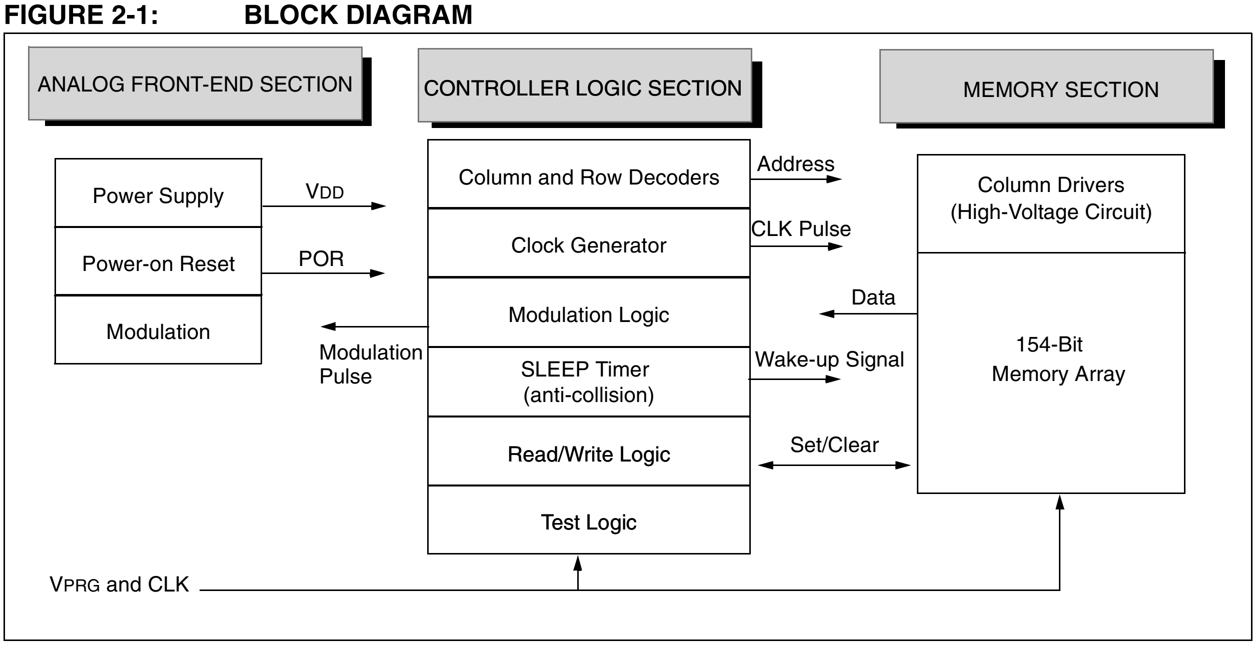
The modulation transistor is placed between antenna B and Vss pads and has small turn-on resistance (R_M). This small turn-on resistance shorts the external circuit between the antenna B and Vss pads as it turns on.

The transistor turns on during the “Hi” period of the modulation data and turns off during the “Lo” period.

When the transistor is turned off, the resonant circuit resonates at the carrier frequency. Therefore, the external circuit develops maximum voltage across it. This condition is called uncloaking (tuned). When the transistor is turned on, its low turn-on resistance shorts the external circuit, and therefore the circuit no longer resonates at the carrier frequency. The voltage across the external circuit is minimized. This condition is called cloaking (detuned).

The device transmits data by cloaking and uncloaking based on the on/off condition of the modulation transistor. Therefore, with the 70 kHz - Manchester format, the data bit “0” will be sent by cloaking (detuned) and uncloaking (tuned) the device for 7 µs each. Similarly, the data bit “1” will be sent by uncloaking (tuned) and cloaking (detuned) the device for 7 µs each. See Figure 2-2 for the Manchester waveform.

FIGURE 2-1: BLOCK DIAGRAM



2.2 Controller Logic Section

2.2.1 CLOCK PULSE GENERATOR

This circuit generates a clock pulse (CLK). The clock pulse is generated by an on-board time base oscillator. The clock pulse is used for baud rate timing, data modulation rate, etc.

2.2.2 MODULATION LOGIC

This logic acts upon the serial data (154 bits) being read from the memory array. The data is then encoded into Manchester format. The encoded data is then fed to the modulation transistor in the analog front-end section. The Manchester code waveform is shown in Figure 2-2.

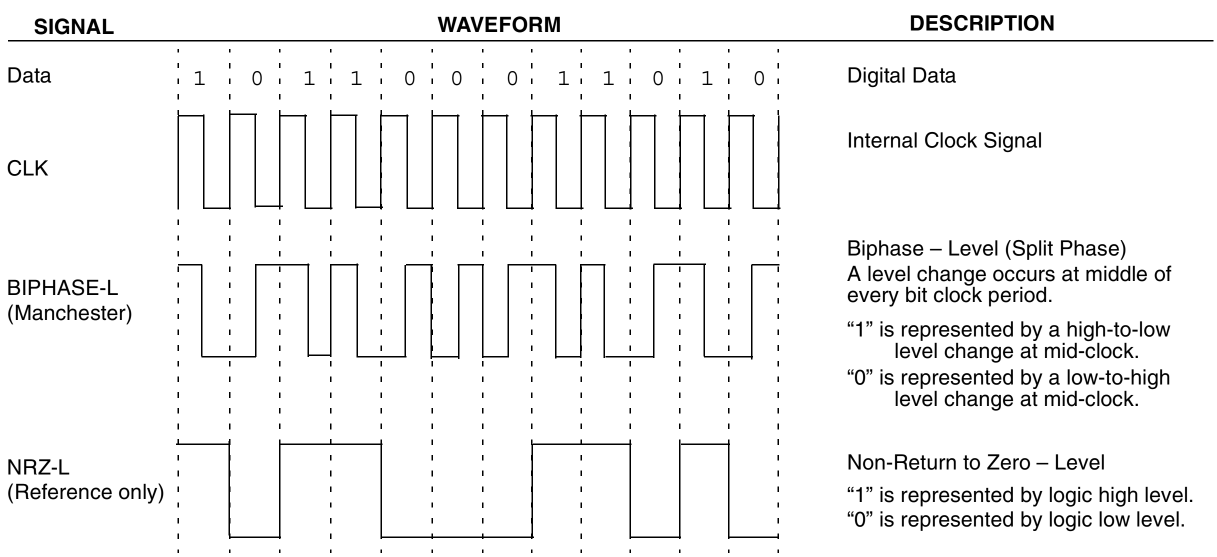
2.2.3 SLEEP TIMER

This circuit generates a SLEEP time (100 ms ± 50%) for the anti-collision feature. During this SLEEP time (T_{OFF}), the modulation transistor remains in a turned-on condition (cloaked) which detunes the LC resonant circuit.

2.2.4 READ/WRITE LOGIC

This logic controls the reading and programming of the memory array.

FIGURE 2-2: CODE WAVEFORMS



Note: The CLK and NRZ-L signals are shown for reference only. BIPHASE-L (Manchester) is the device output.

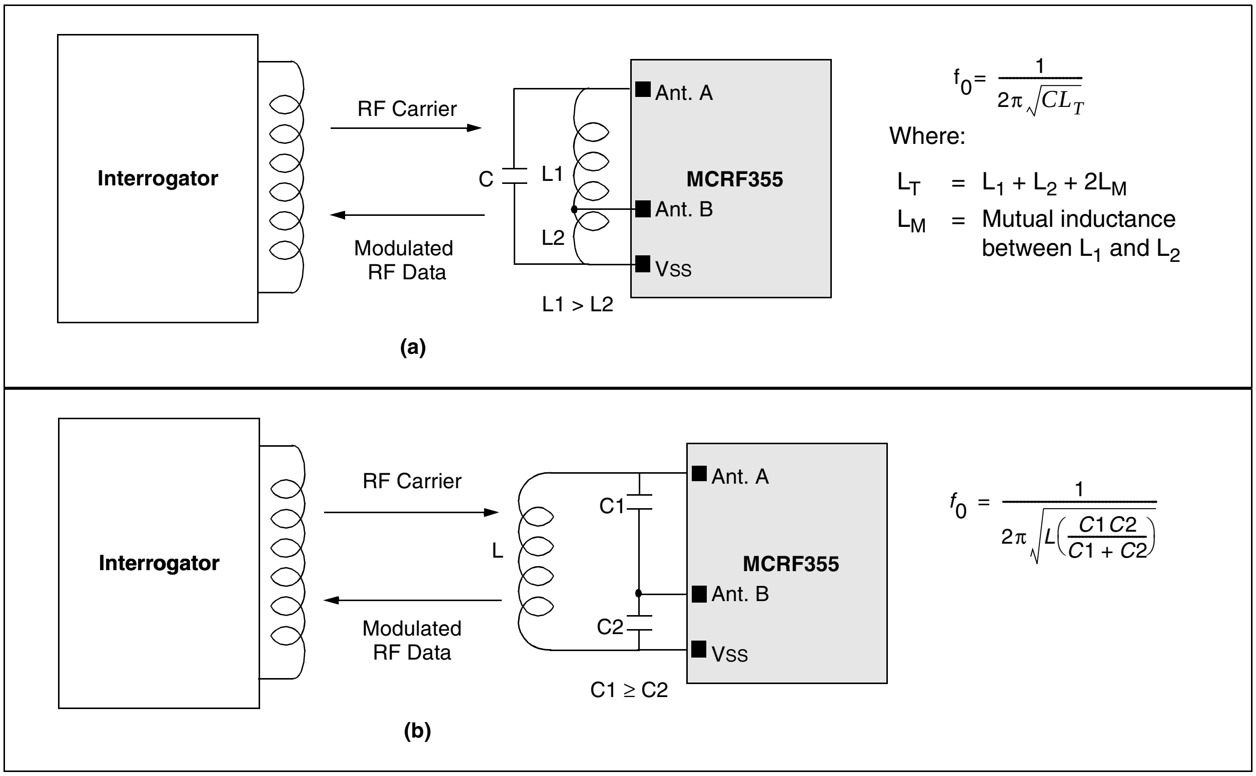
3.0 RESONANT CIRCUIT

The MCRF355 requires external coils and a capacitor in order to resonate at the carrier frequency of the reader. About one-fourth to one-half of the turns of the coil should be connected between antenna B and VSS; remaining turns should be connected between antenna A and B pads.

Figures 3-1 (a) and (b) show possible configurations of the external circuits for the MCRF355. In Figure 3-1 (a), two external antenna coils (L1 and L2) in series and a capacitor that is connected across the two inductors form a parallel resonant circuit to pick up incoming RF signals and also to send modulated signals to the reader. The first coil (L1) is connected between antenna A and B pads. The second coil (L2) is connected between antenna B and VSS pads. The capacitor is connected between antenna A and VSS pads.

Figure 3-1(b) shows the resonant circuit formed by two capacitors (C1 and C2) and one inductor.

FIGURE 3-1: CONFIGURATION OF EXTERNAL RESONANT CIRCUITS



4.0 DEVICE PROGRAMMING

MCRF355 is a reprogrammable device in Contact mode. The device has 154 bits of reprogrammable memory. It can be programmed in the following procedure. (A programmer, part number PG103003, is available from Microchip). Developer kits, DV103003 and DV103006, also include contact programmers.

4.1 Programming Logic

Programming logic is enabled by applying power to the device and clocking the device via the CLK pad while loading the mode code via the V_{PRG} pad (See Examples 4-1 through 4-4 for test definitions). Both the CLK and the V_{PRG} pads have internal pull-down resistors.

4.2 Pin Configuration

Connect antenna A, antenna B and V_{SS} pads to ground.

4.3 Pin Timing

1. Apply V_{DDT} voltage to V_{DD}. Leave V_{SS}, CLK and V_{PRG} at ground.
2. Load mode code into the V_{PRG} pad. The V_{PRG} is sampled at CLK low-to-high edge.
3. The above mode function (3.2.2) will be executed when the last bit of code is entered.
4. Power the device off (V_{DD} = V_{SS}) to exit Programming mode.
5. An alternative method to exit the Programming mode is to bring CLK logic "High" before V_{PRG} to V_{HH} (high voltage).
6. Any Programming mode can be entered after exiting the current function.

4.4 Programming Mode

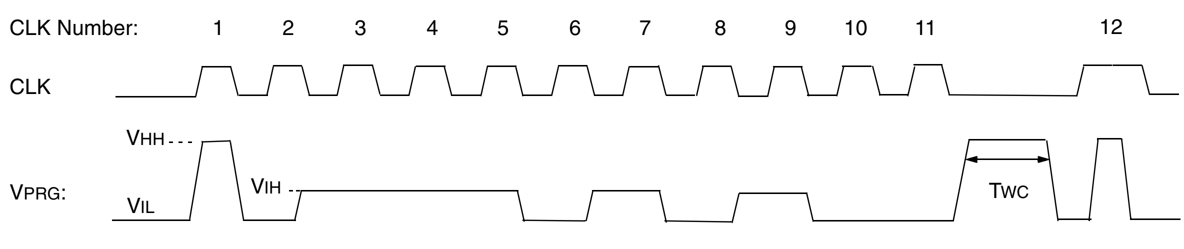
1. Erase EE Code: `0111010100`
2. Program EE Code: `0111010010`
3. Read EE Code: `0111010110`

Note: '0' means logic "Low" (V_{IL}) and '1' means logic "High" (V_{IH}).

4.5 Signal Timing

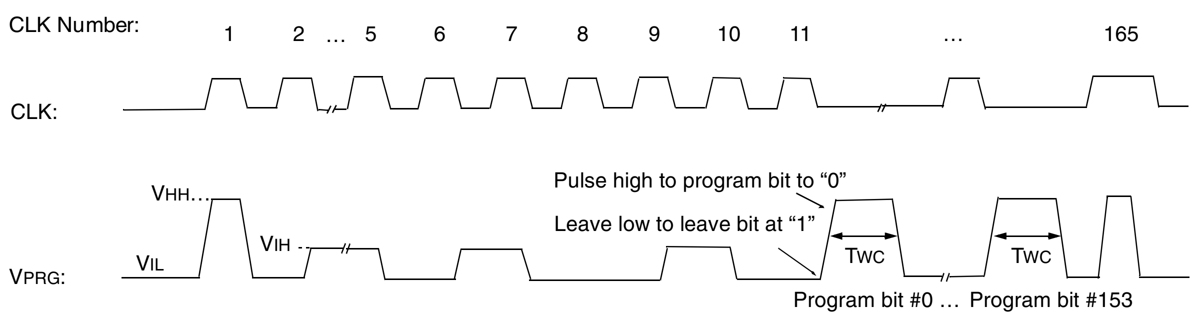
Examples 4-1 through 4-4 show the timing sequence for programming and reading of the device.

EXAMPLE 4-1: PROGRAMMING MODE 1: ERASE EE



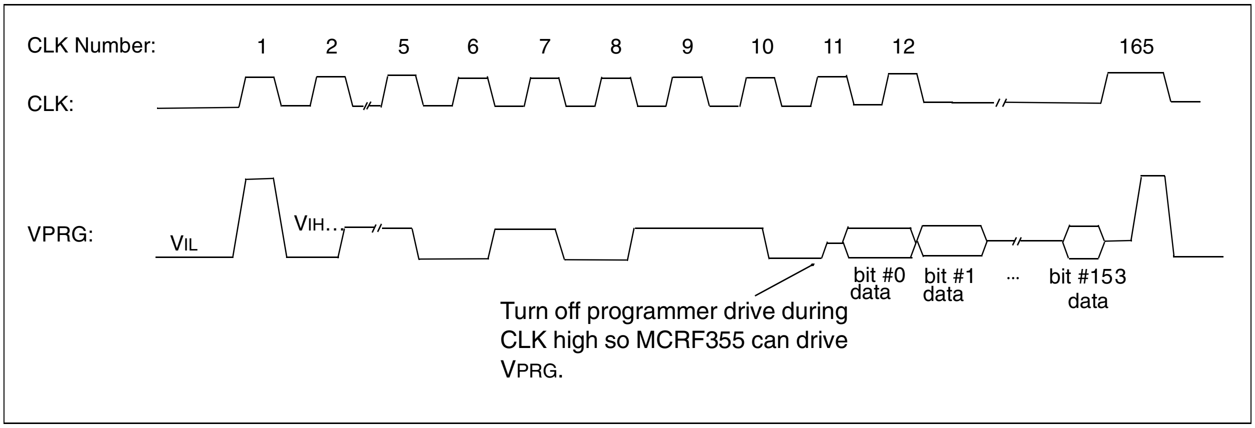
Note: Erases entire array to a '1' state between CLK 11 and 12.

EXAMPLE 4-2: PROGRAMMING MODE 2: PROGRAM EE

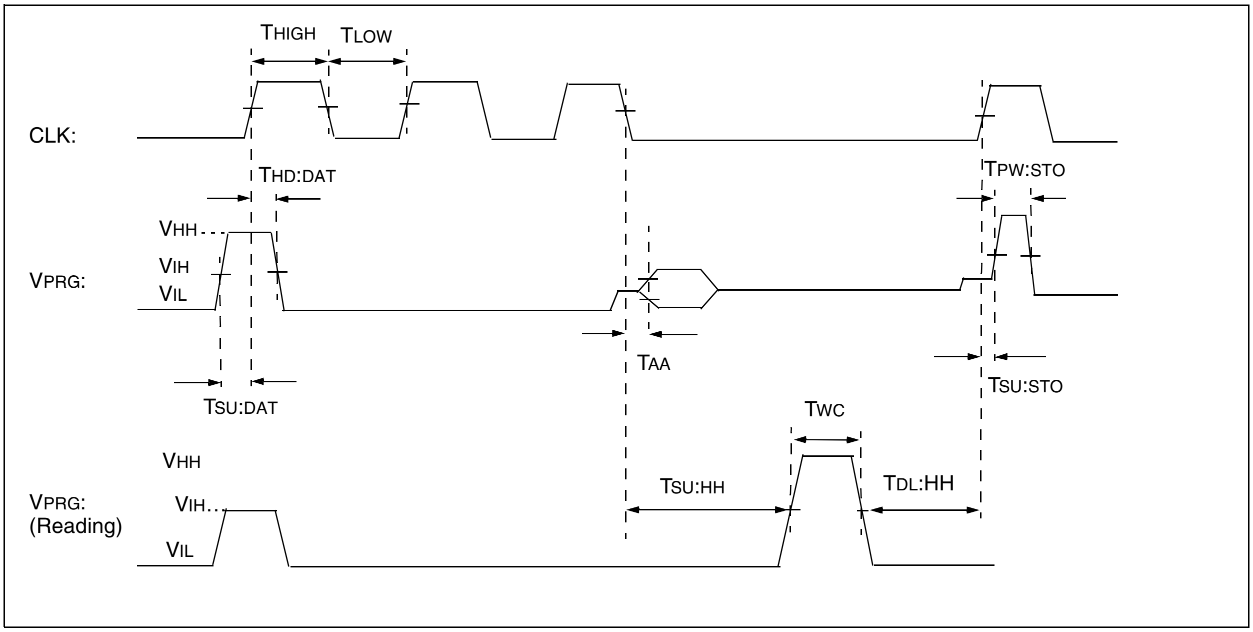


Note: Pulsing V_{PRG} to V_{HH} for the bit programming time while holding the CLK low programs the bit to a '0'.

EXAMPLE 4-3: PROGRAMMING MODE 3: READ EE



EXAMPLE 4-4: TIMING DATA



5.0 FAILED DIE IDENTIFICATION

Every die on the wafer is electrically tested according to the data sheet specifications and visually inspected to detect any mechanical damage, such as mechanical cracks and scratches.

Any failed die in the test or visual inspection is identified by black colored ink. Therefore, any die covered with black ink should not be used.

The ink dot specification:

- Ink dot size: 254 µm in circular diameter
- Position: central third of die
- Color: black
- Wafer map files are also available upon request

6.0 WAFER DELIVERY DOCUMENTATION

The wafer is shipped with the following information:

- Microchip Technology Inc. MP Code
- Lot Number
- Total number of wafers in the container
- Total number of good dice in the container
- Average die per wafer (DPW)
- Scribe number of wafers with number of good dice
- Wafer map files are also available upon request

7.0 NOTICE ON DIE AND WAFER HANDLING

The device is very susceptible to Electro-Static Discharge (ESD), which can cause critical damage to the device. Special attention is needed during the handling process.

Any ultraviolet (UV) light can erase the memory cell contents of an unpackaged device. Fluorescent lights and sunlight can also erase the memory cell, although it takes more time than UV lamps. Therefore, keep any unpackaged device out of UV light and also avoid direct exposure of strong fluorescent lights and shining sunlight.

Certain IC manufacturing, COB and tag assembly operations may use UV light. Operations such as backgrind de-tape, certain cleaning procedures, epoxy or glue cure should be done without exposing the die surface to UV light.

Using X-ray for die inspection will not harm the die, nor erase memory cell contents.

8.0 REFERENCES

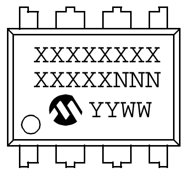
It is recommended that the reader reference the following documents.

1. “Antenna Circuit Design for RFID Applications”, AN710, DS00710.
2. “RFID Tag and COB Development Guide with Microchip’s RFID Devices”, AN830, DS00830.
3. “MCRF355/360 Application Note: Mode of Operation and External Resonance Circuit”, AN707, DS00707.
4. “Microchip Development Kit Sample Format for the MCRF355/360 Devices”, TB031, DS91031.
5. “MCRF355/360 Reader Reference Design”, DS21311.

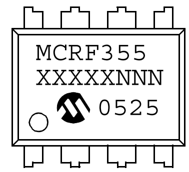
PACKAGING INFORMATION

8.1 Package Marking Information

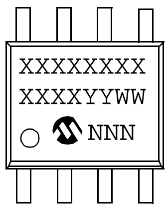
8-Lead PDIP (300 mil)



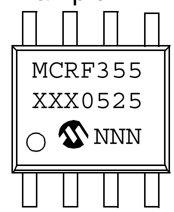
Example:



8-Lead SOIC (150 mil)



Example:

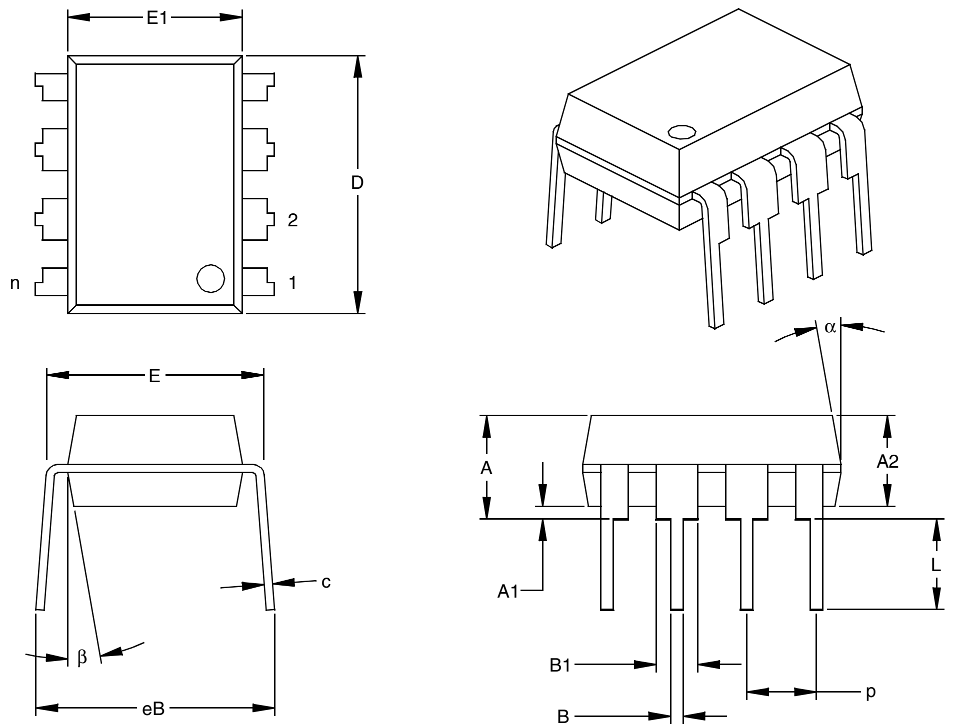


Legend:	XX...X	Customer specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard device marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

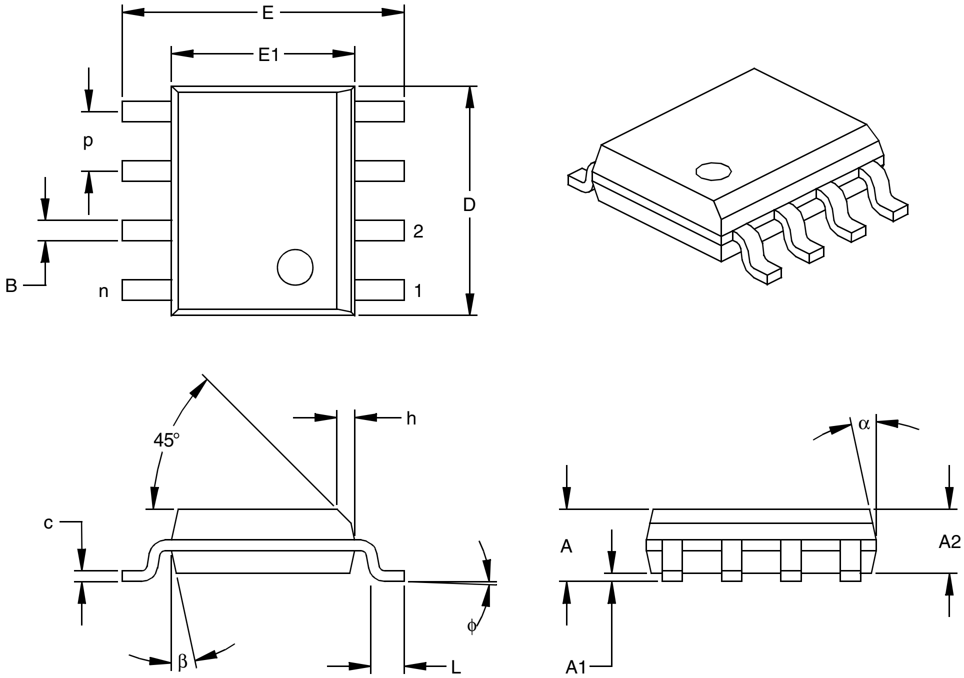


UNITS		INCHES*			MILLIMETERS		
DIMENSION LIMITS		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



UNITS		INCHES*			MILLIMETERS		
DIMENSION LIMITS		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	.10	.18	.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	.25	.38	.51
Foot Length	L	.019	.025	.030	.48	.62	.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	.20	.23	.25
Lead Width	B	.013	.017	.020	.33	.42	.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

NOTES:

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- Development Systems Information Line

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Technical support is available through the web site at: http://support.microchip.com

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

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Device: MCRF355   Literature Number: DS21287G

Questions:

1. What are the best features of this document?

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XXX	XXX
Device	Temperature Range	Package	Programming

Device:	MCRF355	=	13.56 MHz Anti-Collision device.
Temperature Range:		=	-20°C to +70°C
Package:	W	=	Wafer (11 mil backgrind)
	WF	=	Sawed wafer on frame (8 mil backgrind)
	P	=	Plastic PDIP (300 mil Body) 8-lead
	S	=	Dice in waffle pack (8 mil)
	SN	=	Plastic SOIC (150 mil Body) 8-lead
Programming:	blank	=	blank memory
	Q11	=	Factory programmed in Microchip format (see TB031)

Examples:

a) MCRF355/W: = 11-mil wafer, blank

b) MCRF355/WF: = 8-mil wafer on frame, blank

c) MCRF355/P: = PDIP package, blank

d) MCRF355/SNQ11 = SOIC package, factory-programmed

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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