November 2007

KP12x Kit

Evalkit for Pressure Sensors

User's Manual

Rev. 1.1

Sense & Control

Never stop thinking

Edition 2007-11-23

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KP12x Kit Evalkit for Pressure Sensors

Revision History: 2007-11-23, Rev. 1.1

Previous Version: 1.0

Page	Subjects (major changes since last revision)
Page 25	Chapter Data Frames reworked.
Page 30	More detailled description of margin mode.
Page 37	Updated communication conditions.

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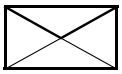

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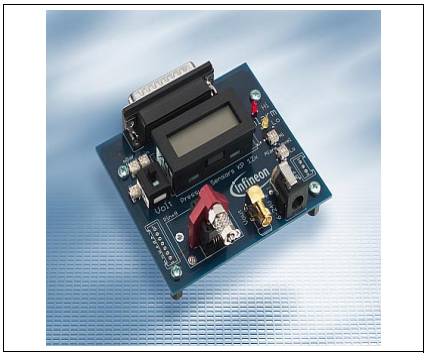
1 Overview



The Pressure Evaluation and Demo Board is intended for following purposes:

Stand-Alone Evalboard for Pressure Sensors KP12x Family

The board can be used as barometer. The sensor is placed in a test socket. It can be optionally soldered directly on the board.

With a standard KP125 pressure sensor, the range goes from 40 kPa (400 mbar) to 115 kPa (1150 mbar).

- Supply
  - 9V Block Battery or 4 x 1.5V batteries in series
  - Power supply 6 ...24V, 50mA
- Display
  - Output voltage in V
  - Barometric pressure in mbar[1)]
  - Limit warning (Upper and lower threshold with LED)
- Power transistors
  - Output of two power transistors BSP75N that drive the LEDs available at external PINs

Evalkit with PC Interface for Pressure Sensors KP12x Family

If a PGSISI interface box is used (see **Figure 10**), the board can be supplied out of the box feeding the voltage regulator with a voltage >6V. Alternatively the V_{DD} may be directly produced from the box. The output voltage can be read back over an analogue input channel. Additionally internal digital values can be read using the SPI interface.

For evaluation purposes in a laboratory environment, the PGSISI box can be used to calibrate the sensor and program the registers in the sensor temporarily. After resetting or disconnecting the sensor, all changes are gone.

With an optional pressure coupling unit, it can be connected with a tube to a pressure source.

1) The displayed pressure value is only an approximation realized with a simple resistor network. The transfer function (offset and gain) is not exactly identical to the sensor behavior. With the potentiometer offset and gain can be adjusted within a certain accuracy range.

Product Name	Product Type	Ordering Code
KP12x Kit	Evalkit for Pressure Sensors	SP000367785
KP12x Board	Evalboard for Pressure Sensors	SP000367783

1.1 Technical Description

1.1.1 Power Supply

The board may be supplied alternatively by battery or a DC voltage power supply.

Note: In case of battery supply it is recommended to switch it on only for short term. Otherwise the lifetime of the battery is not very long (10 to 20 hours for a 9V block battery).

1.1.2 Display

The pressure value or the output voltage can be read on a LCD display. The mode can be selected with a switch.

The default boards are equipped with a 3.5 digits LCD display (see **Figure 1**). Alternatively, the assembly of a precision 4.5 digits display is possible.

Figure 1 3.5 digits LCD Display

1.1.2.1 Display Calibration

The exact output voltage value can only be measured via the connector CON2 (see **Figure 3**) or read out via PC-Interface (**Page 13**). An output voltage value and the equivalent value in mBar of the sensor can be read from the LCD display. This value is not accurate according to the data sheet. Voltage and mBar display values can be adjusted via potentiometers (see **Figure 2**).

Figure 2 Display Configuration via Potentiometers

Output voltage calibration

1. Insert the sensor (see **Figure 4**).
2. Plug in the 9 to 24 V wall power supply to create 5 V through the voltage regulator placed on the KP12xEvalBoard.
3. Measure the output voltage with a volt meter on CON2 (see **Figure 3**).
4. Switch to “Volt”.
5. Adjust the potentiometer until the displayed value matches the measured value.

Calibration of equivalent value in mBar

1. Unplug the PGSISI Box if attached (it has a very small leakage current which would create a voltage of -0.3 V at the Vout sensor pin).
2. Plug in the 9 to 24 V wall power supply to create 5 V through the voltage regulator placed on the KP12xEvalBoard.
3. Take the sensor out of its socket if sensor is inserted.
4. Switch to "Volt", the LCD must now display "0.00".
5. Switch to "mBar".
6. Adjust the "mBar offset" potentiometer until the LCD displays the mBar value for a sensor output voltage of 0.0 V (refer to data sheet).
7. Insert the sensor into the socket (see **Figure 4**).
8. Adjust the 'V' potentiometer until the LCD displays the actual sensor output voltage.
9. Adjust the "mBar gain" potentiometer until the LCD displays the actual ambient pressure in mBar.
10. You may want to repeat steps 3 to 9 to verify your settings.

1.1.3 Pressure Sensor

Following sensors in a PG-DSOF-8-12 package are supported:

- KP120 (no software support via PGSISI Box)
- KP123, KP124, KP125, KP126 and derivatives

The connection is done using a test socket. Additionally, a pressure adapter can be mounted.

Measure points for all sensor pins are available at CON 2 on the lower left corner of the board, see **Figure 3** and **Table 1**.

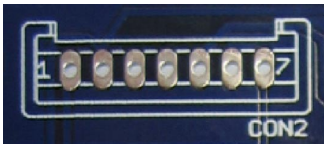


Figure 3 Measure Points for all Sensor Pins

Table 1 Pin Definitions and Functions

Pin No. Sensor	Pin No. CON2 Evalboard	Name	Function
1	1	TEST	Test pin
2	2	CLOCK / V_{PROG}	External Clock for Communication / Programming Voltage
3	3	DATA IN	Serial data input pin
4	4	DATA OUT	Serial data output pin
5	5	V_{DD}	Supply Voltage
6	6	GND	0 Volt circuit ground potential
7	7	V_{OUT}	Analog pressure signal output
8	6	GND	Alternative ground pin

Insertion of the User's Manual Sensor

Make sure to insert the User's Manual sensor with the large GND PIN aligned to the marking in the socket, see **Figure 4**.

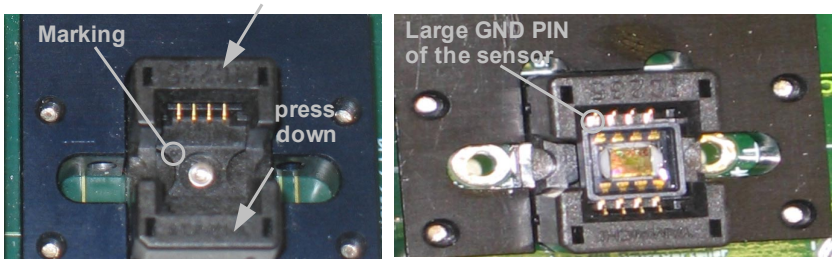


Figure 4 Sensor Insertion

With an optional pressure coupling unit, it can be connected with a tube to a pressure source, see **Figure 5**.

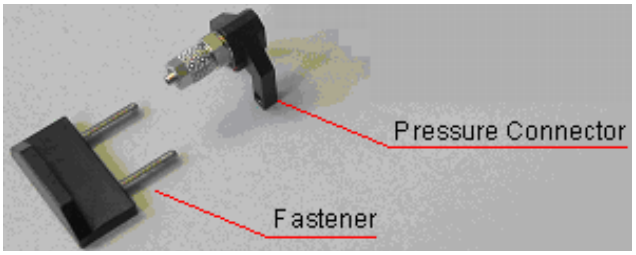


Figure 5 Pressure Connector for the Evalboard

1.1.4 Alarm

The two comparators in IC 31 drive the LEDs 33 and 34. With the trimming potentiometers P33 and P34, two individual thresholds can be set.

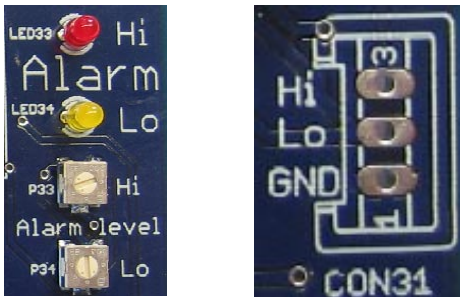


Figure 6 Alarm LEDs for Threshold Violation and Switch Output Signals

- LED33 is active, when the output voltage is over the threshold set in P33.
  It works as a warning for a max value (Hi).
- LED34 is active, when the output voltage is under the threshold set in P34.
  It works as a warning for a min. value (Lo).

The output signals of the comparators are additionally available at CON31 (see **Figure 6**). The signals are buffered with low-side switches BSP75N. They may drive 0.7A with a voltage of 60V.

1.2 Schematic Diagram

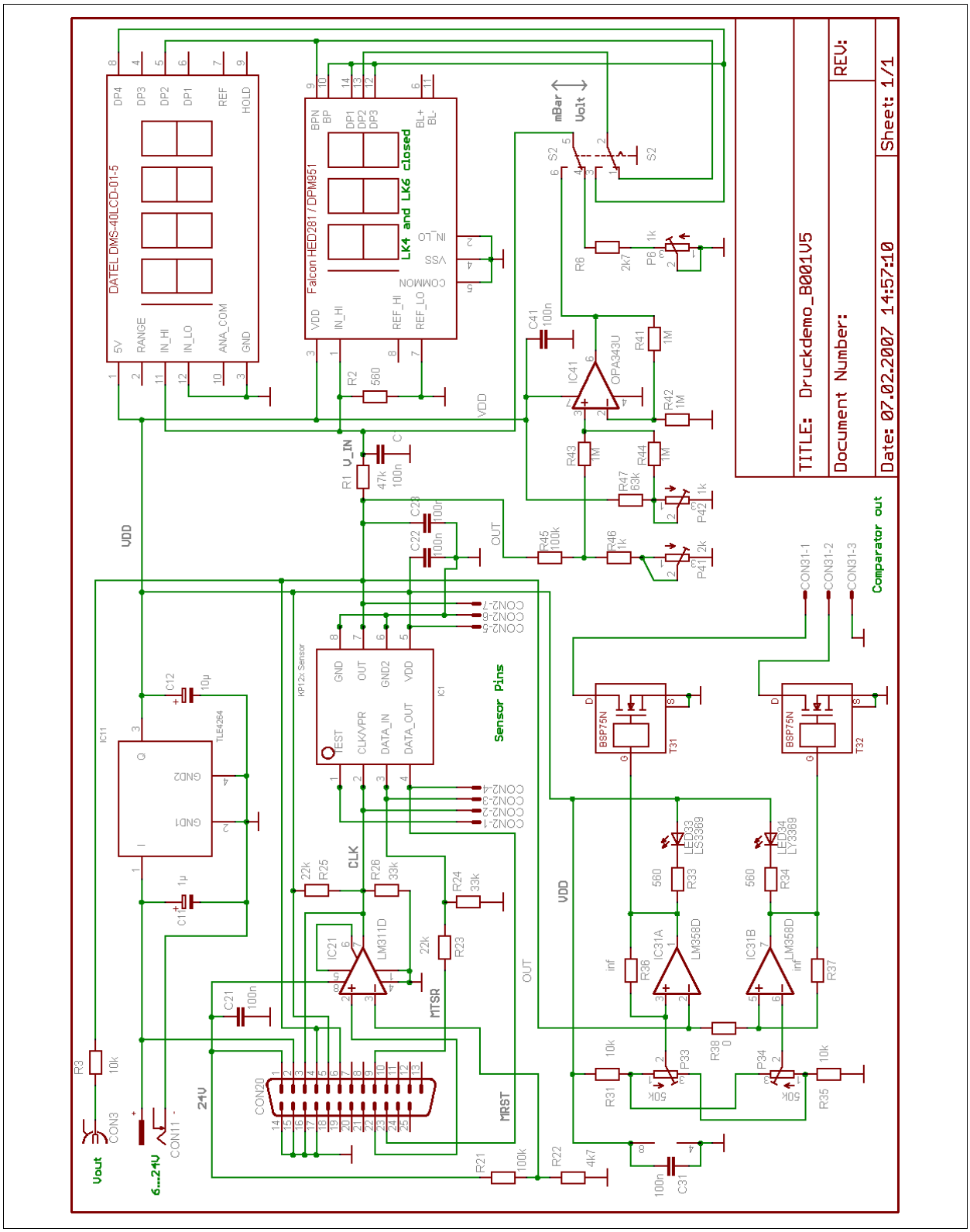


Figure 7 Schematics Diagram

2 Board Layout

Figure 8 shows the components placed on the top layer of the board.

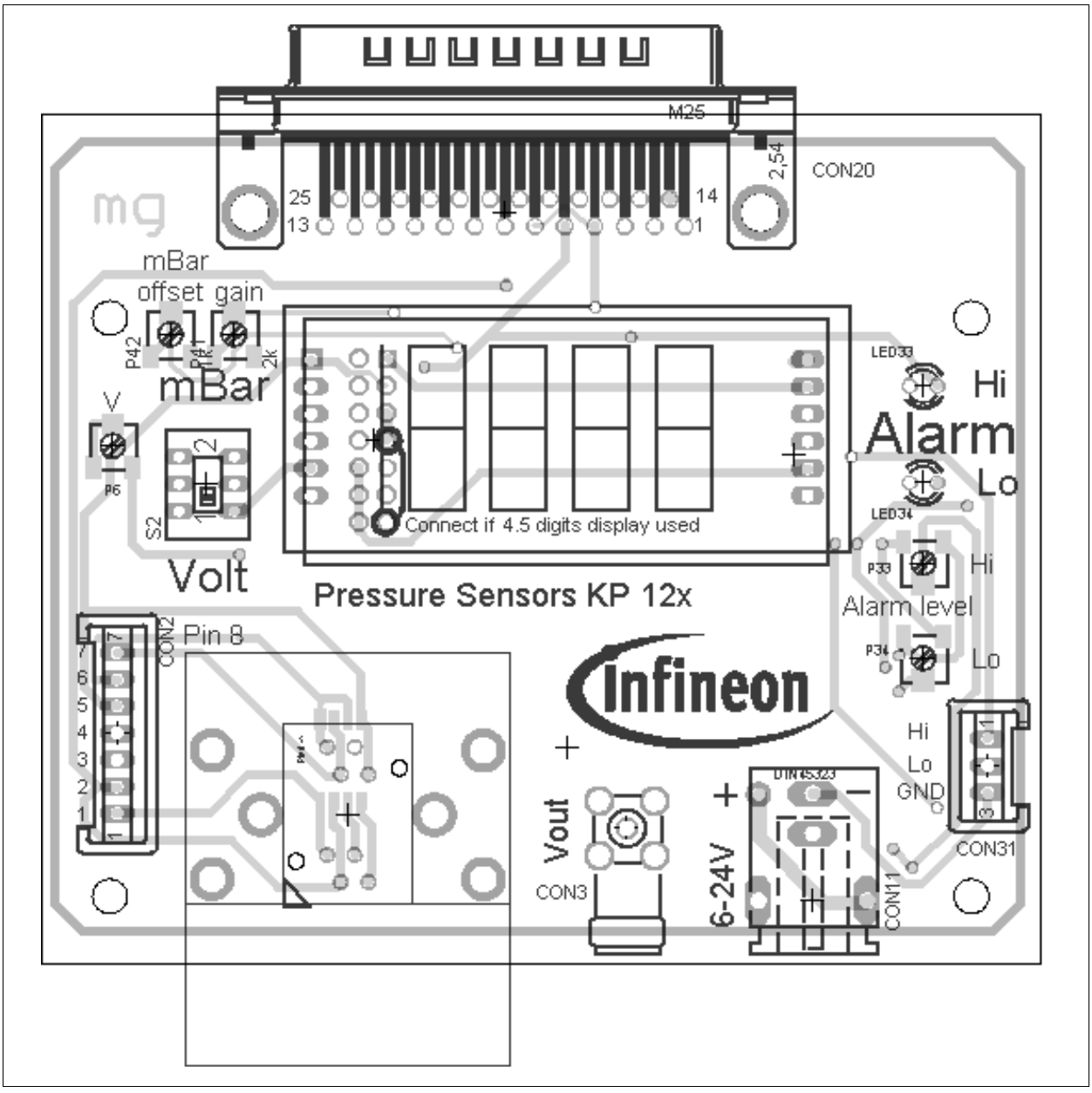


Figure 8 Board Layout Top Layer

Figure 9 shows the components placed on the bottom layer of the board.

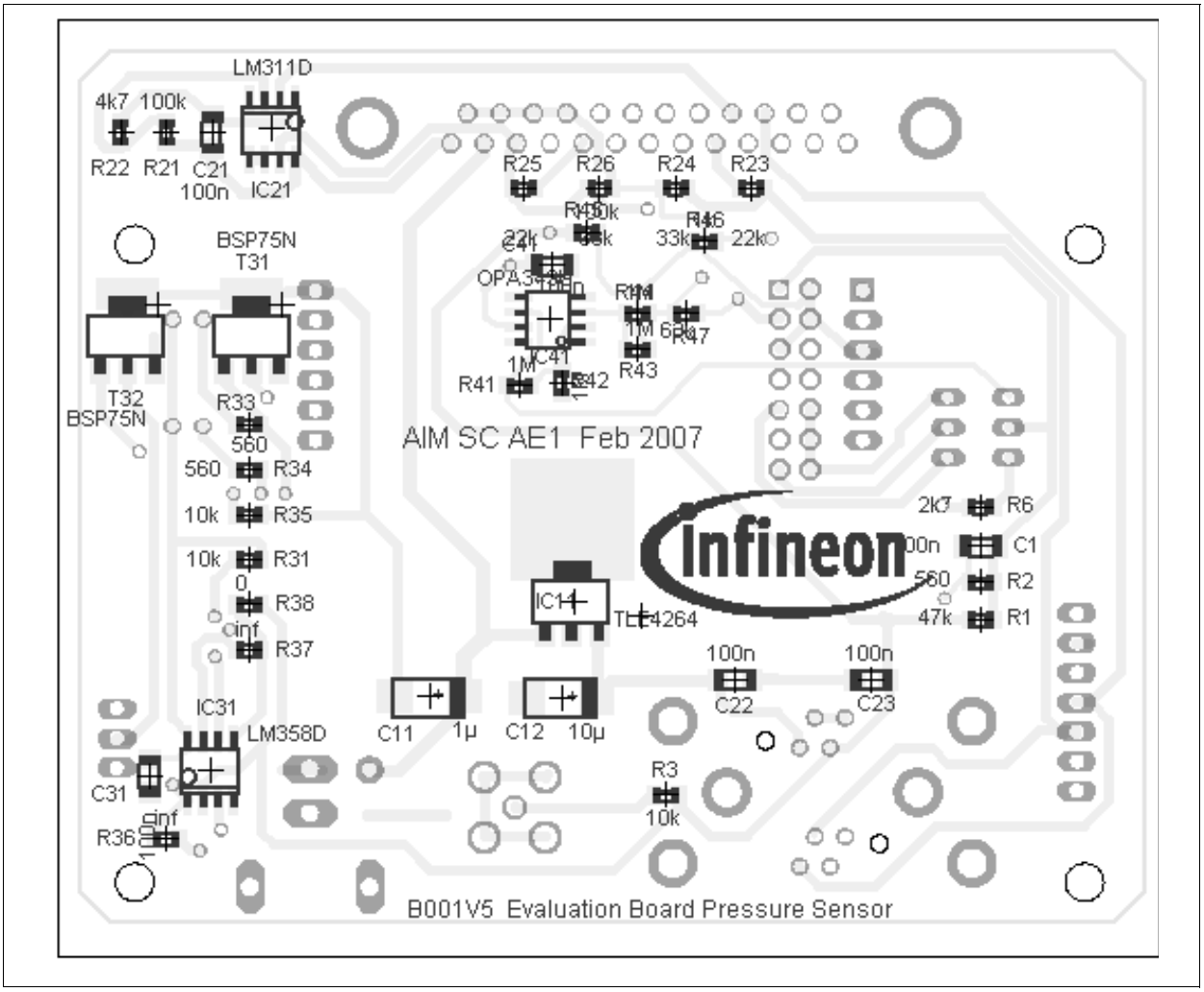


Figure 9 Board Layout Bottom Layer

3 Electrical Parameters

Table 2 Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		min.	typ.	max.		
Supply Voltage	V_{SUP}	6	9	24	V	
Supply Current	I_{SUP}	-	15	20	mA	
Board dimensions		-	80x92	-	mm	only PCB

4 PC Interface

The link to a PC can be made using a PGSISI box (see **Figure 10**).

Figure 10 PGSISI box

The board can be connected directly to the box with the 25 pin connector. Communication with the PC is supported by a USB or alternatively a RS232 interface. Via a graphical user interface sensor internal analog and digital values can be read, see **Figure 11**.

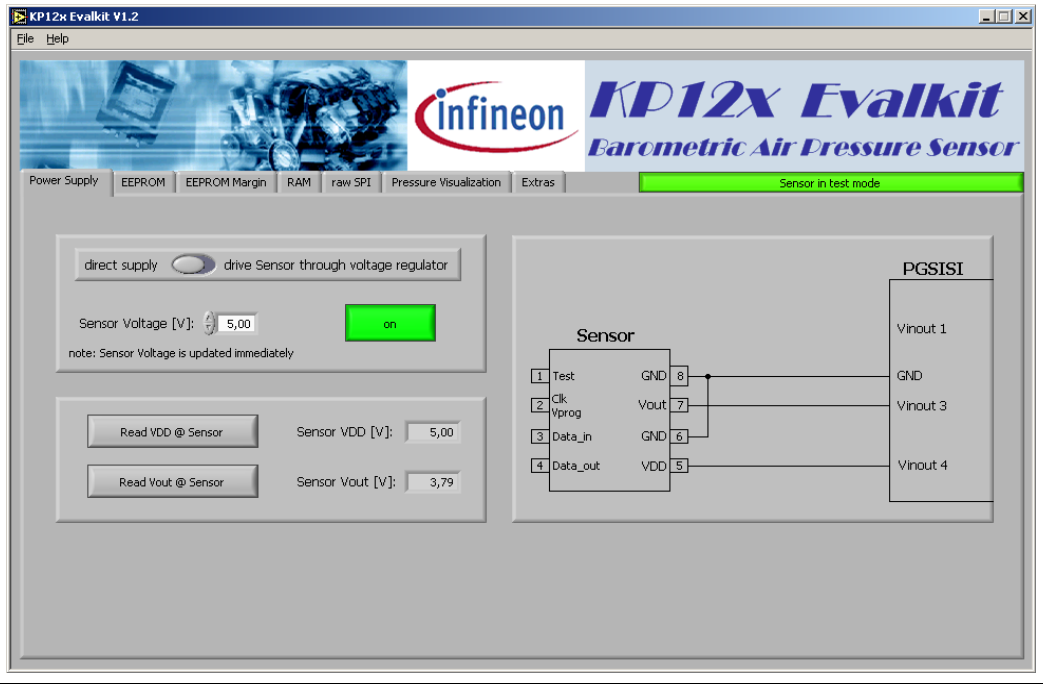


Figure 11 Graphical User Interface

4.1 Hardware

Following equipment is necessary for the PC-Interface:

- PGSISI-Box
- KP12x demoboard
- Power supply unit
- Different power supply adapters
- USB-connector
- Optional: RS232-connector

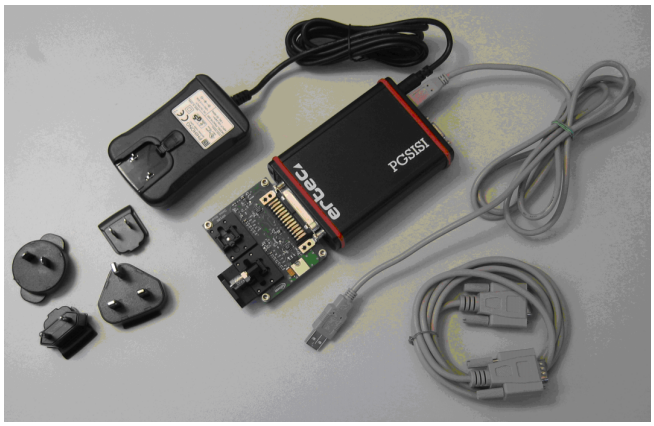


Figure 12 PC-Interface Hardware

4.2 Software

Following software is necessary for the PC-Interface:

- KP12x Evalkit V1.2. Installer
- FTDI Driver (on CD Rom)

4.3 Block Diagram

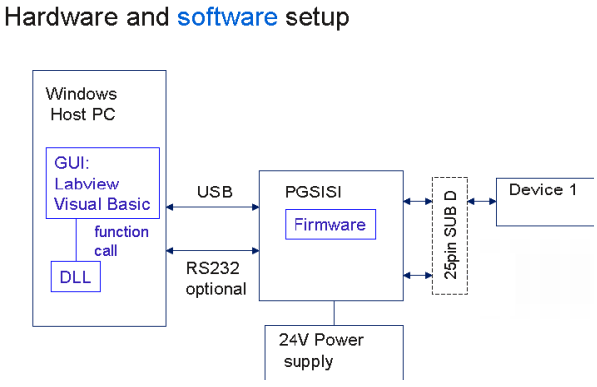


Figure 13 Block Diagram Hardware and Software Setup

The board is connected to the PGSISI box via a 25 Pin connector. The box can be connected to the Computer either via USB or by a serial cable (RS232). User interaction is possible via a Labview environment which is communicating via a DLL with the PGSISI box firmware (**Figure 13**).

5 Installation

5.1 PGSISI Driver Unit

The hardware must be connected as shown in **Figure 12**. The USB connector has to be connected to a free USB port of the PC, alternatively the RS-232 cable can be used.

Note: Be sure not to connect both of them!

After connecting the PGSISI-Box with your PC (Operating System Windows 2000 or WindowsXP) the Installation Wizard will start automatically to install the correct driver. During the installation the *specify alocation* option (see **Figure 14**) should be enabled. The appropriate driver can be found on the CD-ROM in the subfolder volume.

Note: The installation routine operates twice!

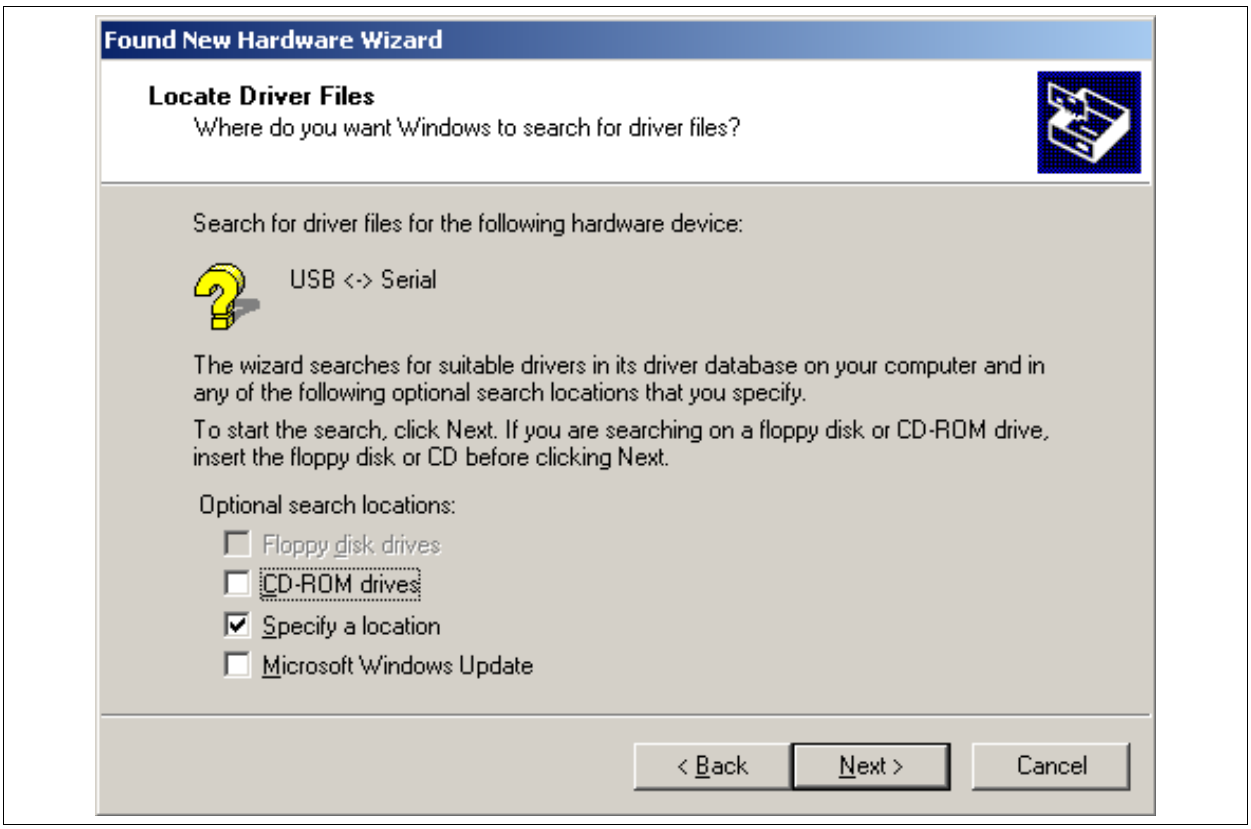


Figure 14 Installer Wizard

5.2 KP12x Evalkit V1.2 Installer

To install the KP12x Evalkit software, insert the provided CD in your CD-ROM drive. Start the *setup.exe* file in the *Volume* folder. The KP12xDemoBoard Installer Wizard will start. Follow the installation instructions. Afterwards you will be able to start the GUI (*Start -> Programs -> KP12x Evalkit -> KP12x Evalkit V1.2*).

6 Graphic User Interface

After installing the KP12xDemoBoard Software and connecting the PGSISI-Box to your PC, the application can be started (*Start -> Programs -> KP12xDemoBoard-> KP12xDemoBoard_v1.2*). The first page is always the power supply page.

6.1 Power Supply Page

The sensor can be powered in two ways: using the voltage output of the PGSISI box (adjustable from 0.0 V to 8.0 V, be sure not to damage the sensor) or the voltage regulator on the demo board (5 V fixed). Additionally the voltages at the sensor pins V_{DD} and V_{out} can be read in.

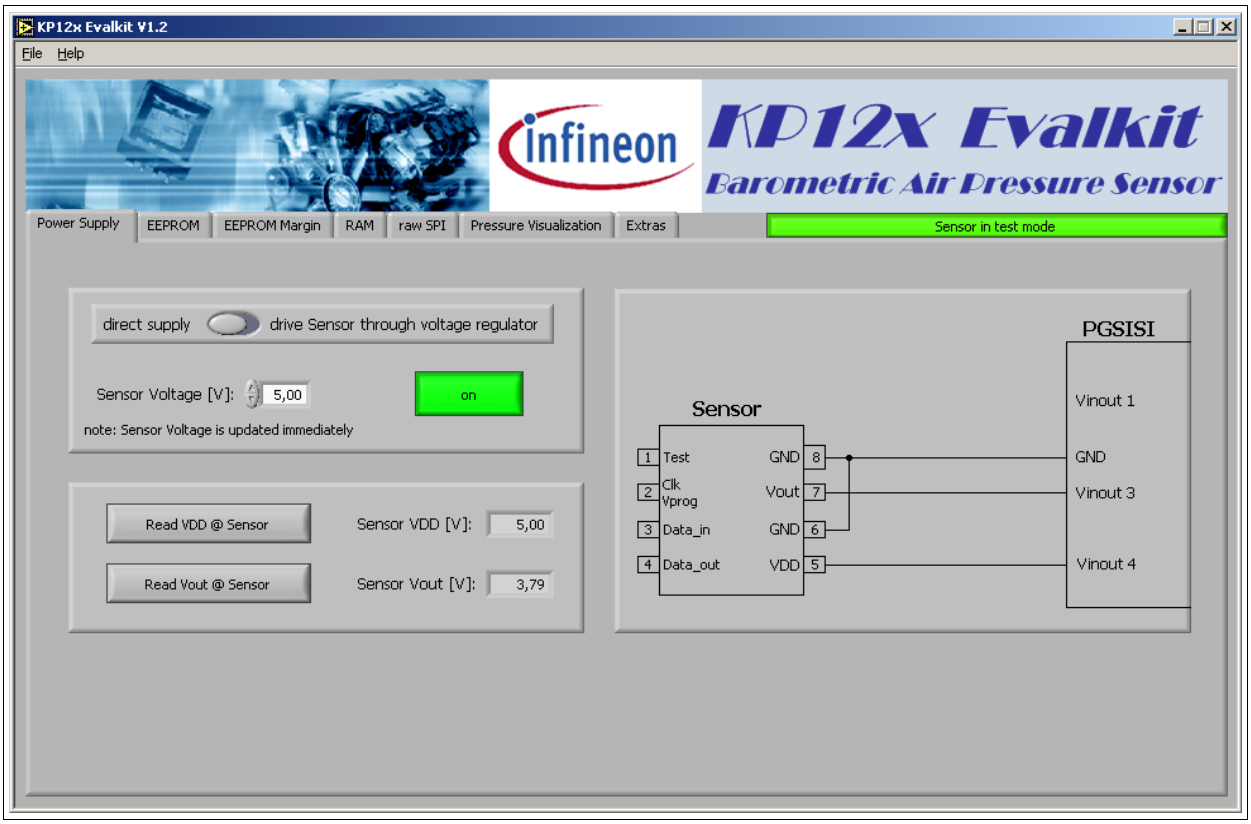


Figure 15 Power Supply Page

6.2 EEPROM Page

The EEPROM page gives the possibility to read out and program (temporary[1)]) the EEPROM shadow register. Therefore, the test mode must be activated. Switching to the EEPROM page (see **Figure 16**), activates the test mode automatically. The *sensor in test mode/sensor in normal operation* button will indicate the status. Pressing this button changes status (this function is available at every page).

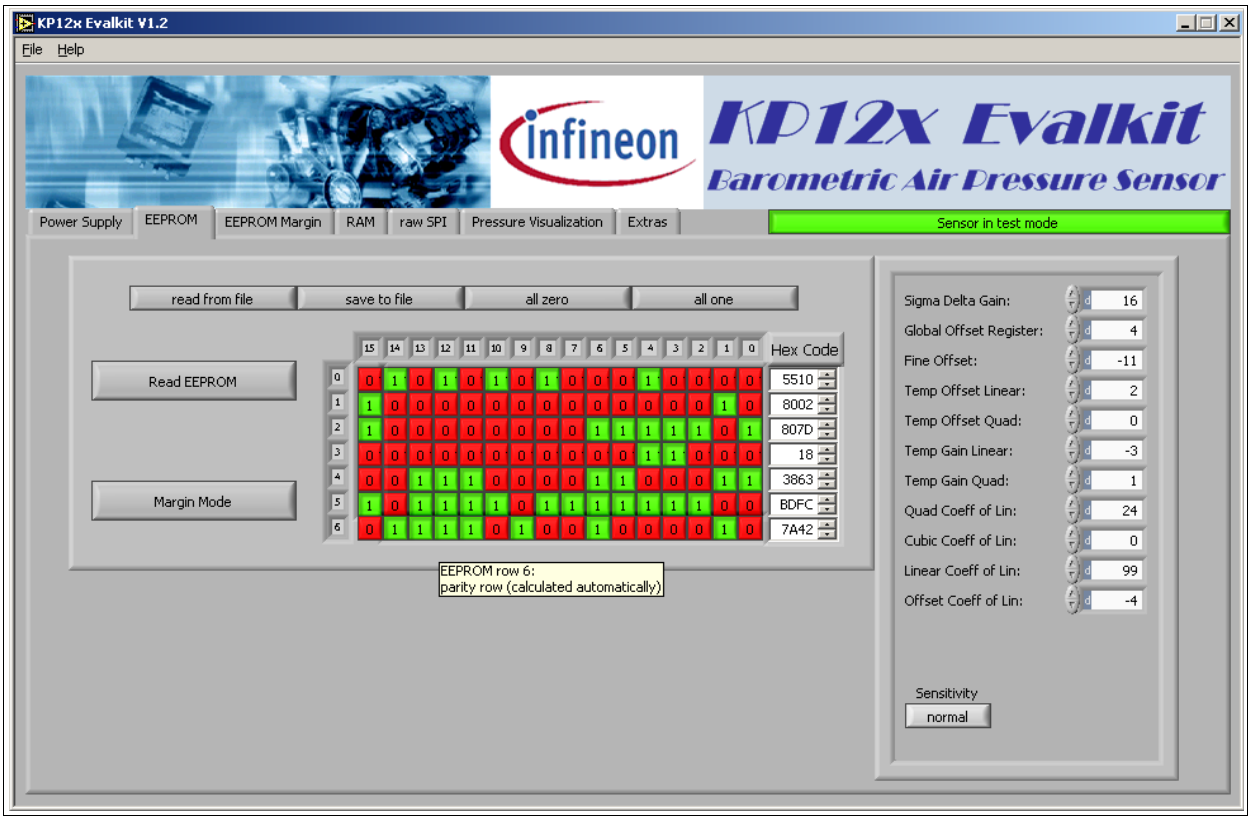


Figure 16 EEPROM Page

1) Disconnecting or power cycling the sensor will discard changes

6.3 EEPROM Margin Page

On this page the voltage of all programmed EEPROM cells can be checked. Switching to the EEPROM margin page automatically activates the test mode.

Figure 17 EEPROM Page

Defining Margin Voltage “1”

For “1” it can be specified in which range (between lower and upper voltage) and with which granularity (voltage per step) the margin voltage is checked. By hitting the check margin voltage “1” button, several readouts with margin voltages from *lower voltage* to *upper voltage* are executed. The voltage level a bit toggles from one to zero is displayed for each bit in the EEPROM table.

Zeros in EEPROM are marked with *“ - “*. If the bit is outside the given range, *“low”* or *“high”* will be displayed.

Defining Margin Voltage “0”:

Here, it is checked wether all “0”s are below a certain level (threshold voltage) with a robust distance to the voltage level of all “1”s. Zeros that are below this level are marked *“ok”*, otherwise *“ERR”*.

6.4 RAM page

The RAM page gives the possibility to read out and write (temporary[1)]) the RAM. Switching to the RAM page automatically activates the test mode.

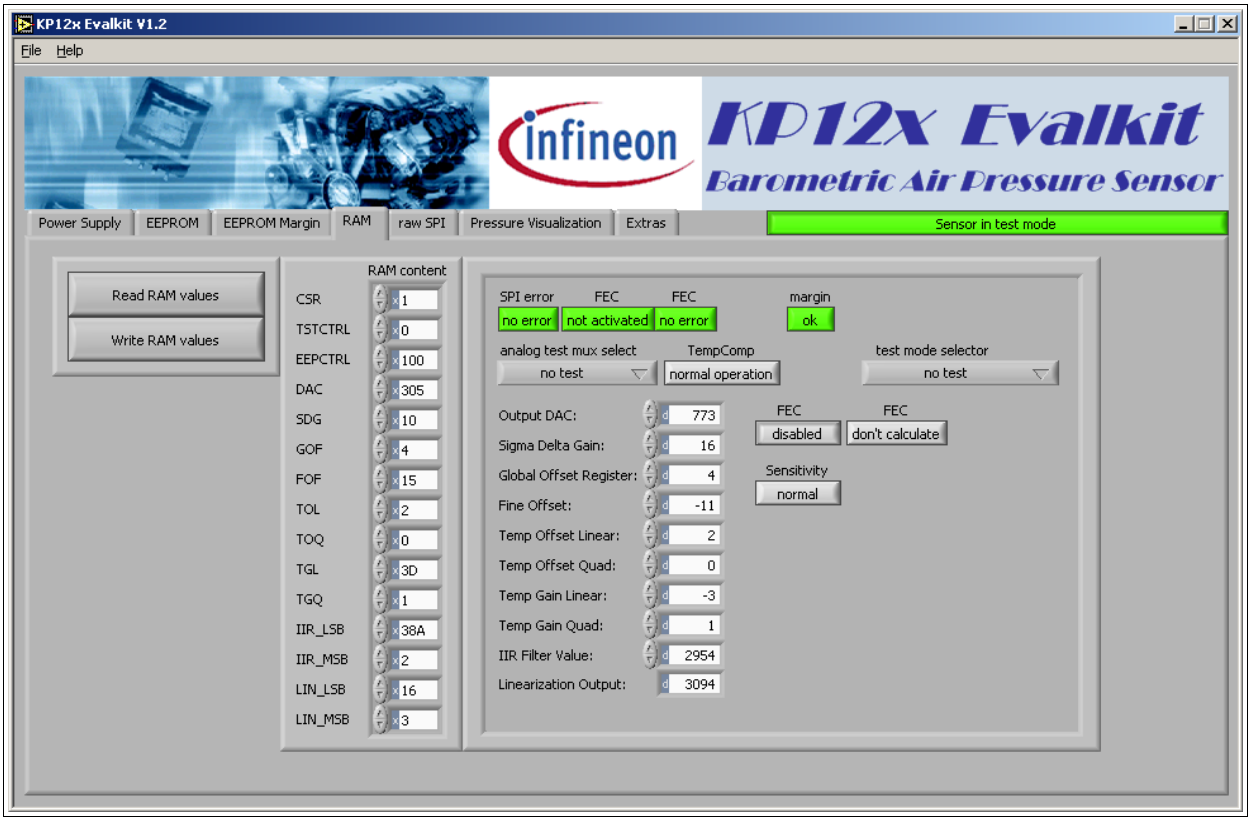


Figure 18 RAM Page

RAM content shows the stored values of the EEPROM registers in hexadecimal format. On the right side the respective human readable meaning of the EEPROM register content is displayed. Changing one representation automatically changes the other one, too.

Besides several status information, some test modes can be activated via drop-down lists. A description of these modes can be found in **Chapter 7.4**.

1) Disconnecting or resetting the sensor will discard changes.

6.5 SPI Page

The SPI page allows sending SPI commands to the sensor. The SPI command could be a read or write command to the given address. The *data in* field gives the possibility to define the data which should be written to the selected register. After executing the SPI command the previous content of the addressed register is shown in the *data out* field.

For details about SPI Communication see **"Digital Interface for EEPROM access" on Page 24**.

Note: A read SPI command is only possible when the sensor is in test mode

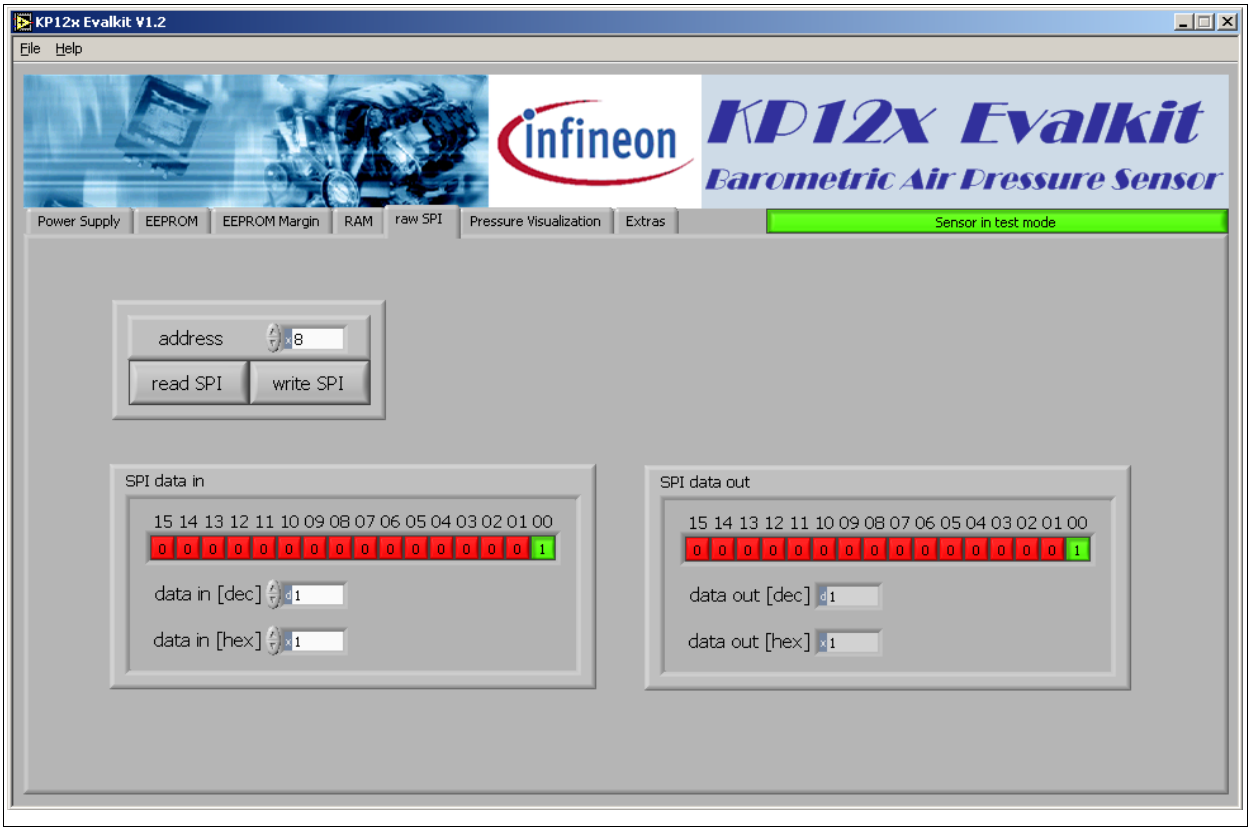


Figure 19 SPI Page

6.6 Pressure Visualization Page

The pressure visualization page continuously shows the output voltage of the sensor (the same value as on page **Power Supply Page**). For activation press *read Vout*. Press the button again to deactivate the measurement.

The coordinate axes are adjustable by changing the values displayed (e.g. mark the maximum voltage “5” with the cursor and type “4.2”).

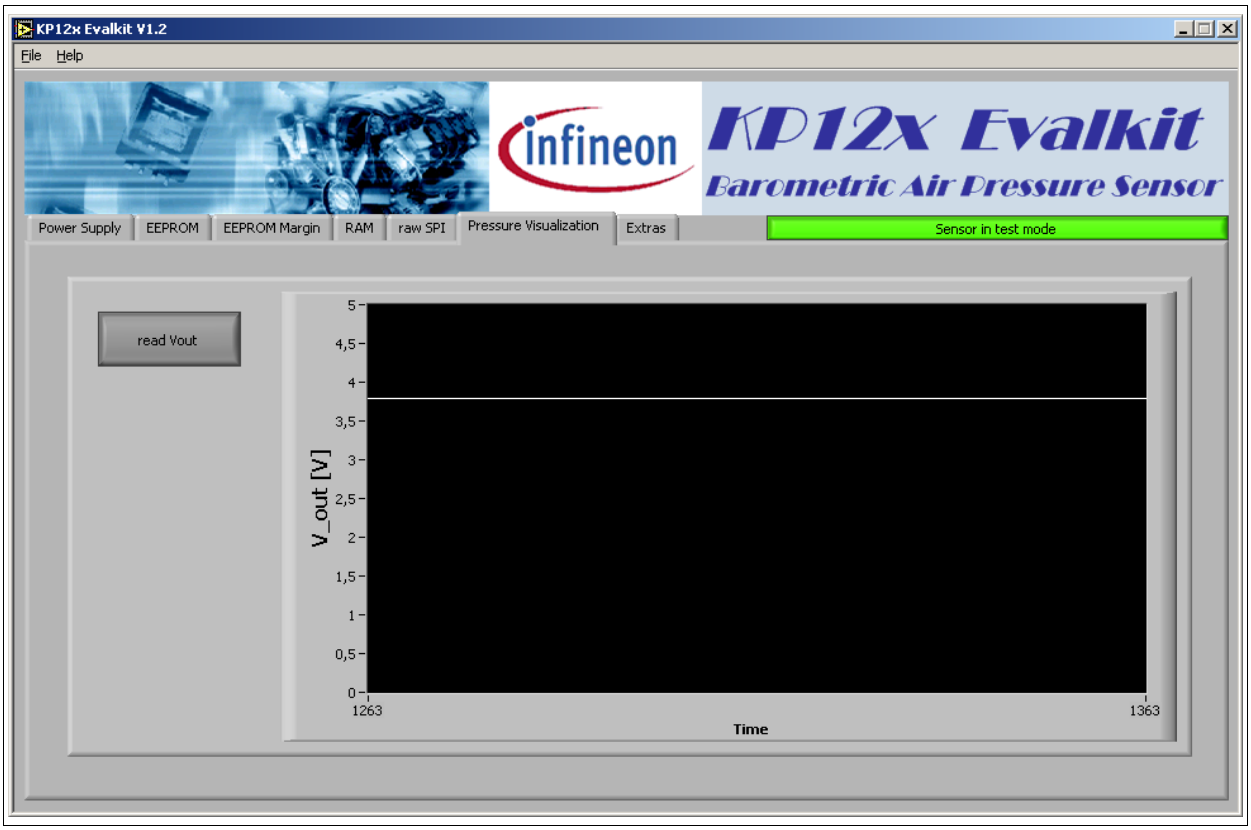


Figure 20 Pressure Visualization Page

6.7 Extras Page

On the Extras page the path settings for reading and saving the EEPROM content can be done.

Figure 21 Extras Page

6.8 Menu bar

Reconnect to PGSISI Box will close the (virtual) COM port, reopen it and start the boot loader again. This can be used when the connection has been lost or the box was powered down.

Open manual shows this document and *About KP12xDemoBoard* presents some version information.

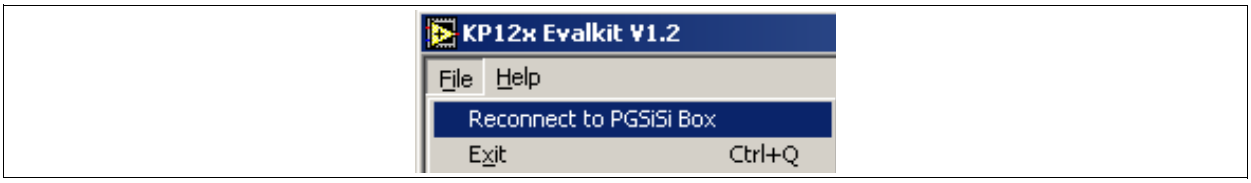


Figure 22 Extras Page - File

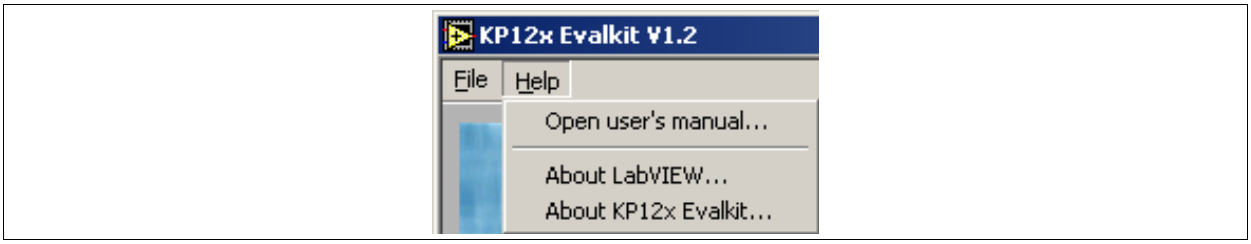


Figure 23 Extras Page - Help

7 Digital Interface for EEPROM access

Communication during calibration process is done via digital programming interface.

The Evalkit for Pressure Sensors digital interface is a three wire interface consisting of DATA IN, DATA OUT and CLOCK / V_{PROG}, see **Figure 24**.

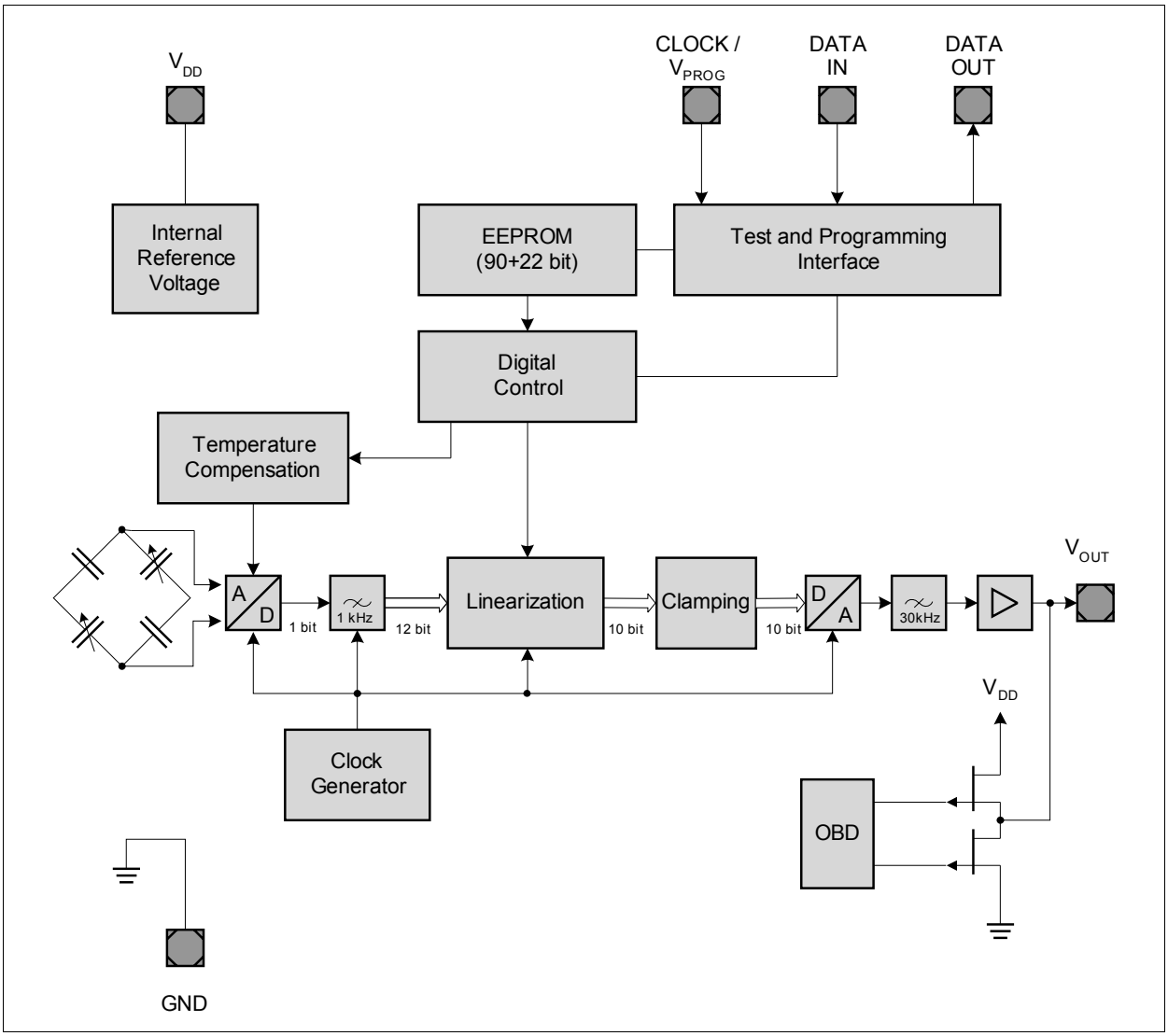


Figure 24 Block Diagram[1)]

1) Clamping only available for KP126 and derivatives

7.1 SPI address space

The address space for SPI communication consists of two main blocks:

- the EEPROM registers (3 bit address)
- the control registers (5 bit address)

addr	register	description
00h	EE0	EEPROM register, analog trim
01h	EE1	EEPROM register, analog trim, memlock
02h	EE2	EEPROM register, analog trim
03h	EE3	EEPROM register, linearization coefficients
04h	EE4	EEPROM register, linearization coefficients / clamping level
05h	EE5	EEPROM register, linearization coefficients / clamping level
06h	EE6	EEPROM register, column parity
07h	reserved	invalid EEPROM register address
08h	CSR	configuration register; test mode activation/deactivation, status flags
09h	TSTCTRL	configuration register, test mode configuration
0Ah	EEPCTRL	configuration register, EEPROM control
0Bh	DAC	data register, read/write output DAC
0Ch	SGD	data register, SD-converter gain setting, MAP/BAP mode select
0Dh	GOF	data register, global offset
0Eh	FOF	data register, fine offset
0Fh	TOL	data register, linear offset of temperature compensation
10h	TOQ	data register, quadratic offset of temperature compensation
11h	TGL	data register, linear gain of temperature compensation
12h	TGQ	data register, quadratic gain of temperature compensation
13h	IIR_LSB	data register, read/write IIR filter value bits 9:0
14h	IIR_MSB	data register, read/write IIR filter value bits 11:10
15h	LIN_LSB	data register, read linearization output bits 9:0
16h	LIN_MSB	data register, read linearization output bits 11:10

EEPROM Registers

Control Registers

Figure 25 SPI Address Space

7.2 Data Frames

- 1 bit write/read (SPI mode: 1 = write/read; 0 = read only)
- 1 bit mode select (Mode select: 1 = E^2PROM register access, 0 = Control register access)
- 3 / 5 bit address (depending on mode)
- 16 / 10 bit data (depending on mode

The configuration of the serial pins (CLOCK/V_{PROG}, DATA_IN, DATA_OUT) is shown in **Figure 1**. The response is readable at the data out pin (DATA_OUT). When sending a serial command (regardless if read or write), the current content of the addressed register can be read out at the DATA_OUT pin after the address has been recognized. During a read operation only the mode selection bit and the address bits are taken into account whereas the data bits are ignored. During a write operation, the current content of the addressed register can be read at DATA_OUT and the content of the data field is written into the register afterwards, provided that the transmission is complete and correct (frame length, address and enable condition).

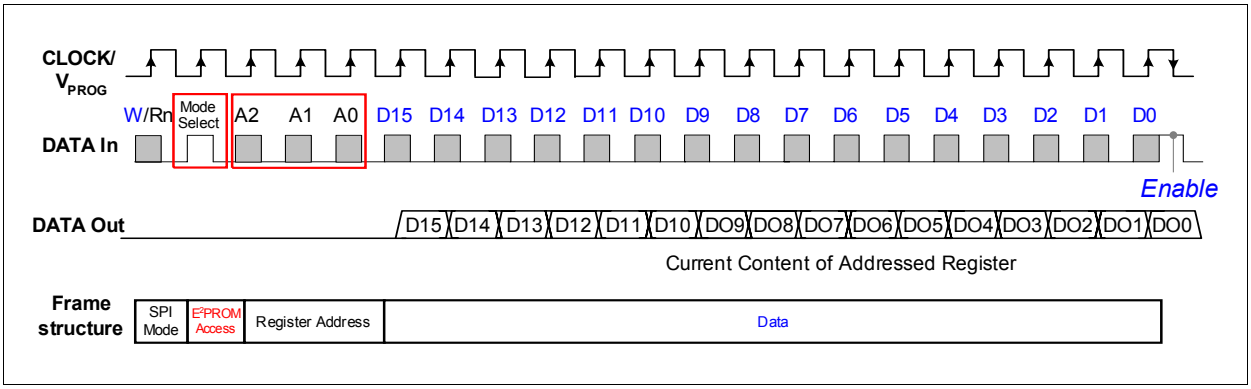


Figure 26 Serial Interface Communication Frame for E²PROM Register Access[1)]

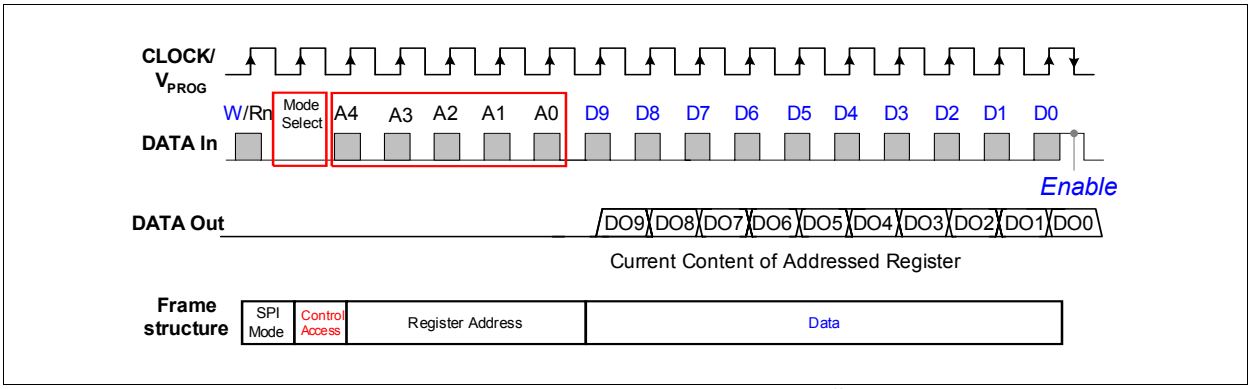


Figure 27 Serial Communication Frame for Control Register Access[2)]

After startup the chip is in normal operation mode and does not react to any read or write command except the test mode activation sequence on the serial interface. Test mode is enabled by writing a defined sequence into the status register. Each data frame has a length of either 17 or 21 clock pulses.

The first bit in the transmission frame is the write/read bit. If it is set to 1 a write of the addressed register is performed.

The second bit is the mode selection bit. This bit determines whether to address EEPROM or command registers, and defines thereby the length of the SPI frame.

During a read operation additionally only the mode selection bit and the address bits have an influence and data bits are ignored. The content of the addressed register is shifted to data_out after the address has been recognized.

During a write operation the addressed register will only be updated after a complete and correct transmission (frame length, address and enable condition). With the N rising edges of the clock the signal on DATA IN is clocked into a shift register. The address and the data words are starting with the MSB, respectively. During the falling edges of the first N-1 clock cycles the DATA IN must be low. The falling edge of the N^{th} clock cycle enables the write frame. At this time DATA IN must be high. This combination comprises the “enable write frame” signal.

The current content of the addressed register is always written to data_out, regardless from read or write mode. If an enable condition occurs prior to the 17th/21st clock pulse a read transmission will be interrupted and a write transmission has no effect; additionally the SPI error flag will be set.

1) Enable condition and Data is ignored for read command.
2) Enable condition and Data is ignored for read command.

When addressing the EEPROM registers, the data frame consists of a 3 bit address and 16 data bits (see **Figure 26**). When addressing the control registers, the data frame consists of a 5 bit address and 10 data bits (see **Figure 27**). Data_in is read after the rising edge of clock and data_out is updated after the rising edge and remains until the next rising edge or in case of the LSB until the end of frame.

In general, data_in has always to be low on the falling clock edge. Only at the last falling clock edge data_in must be high to generate an enable condition and to complete the data frame, otherwise a communication error is detected and no write or read command is performed.

7.3 Register Description

The content of the EEPROM registers should not be changed. In this User's Manual only the content of the *control registers* is described.

After startup the chip is in normal operation mode and does not react to any read or write command except the test mode activation sequence on the serial interface. Test mode is enabled by writing "2CEh" to the CSR register (see **Figure 28**) address. Writing any other sequence disables test mode. Status bits 7/8 (FEC) are updated after EEP refresh or by triggering CALC_FEC in EEP control register and during startup. Deactivation followed by activation of the FEC does not recalculate the FEC-flags. Serial interface does not transmit any status information when test mode is not activated. Status bits cannot be written.

bit	function	value	description	remark
9	SPI_ERR	0	last SPI transaction OK	
		1	last SPI transaction not OK	reset only by a faultless read access
8	FEC_ACT	0	FEC not activated	no parity error in EEP array or FEC disabled
		1	FEC activated	one parity error in EEP array detected and corrected
7	FEC_ERR	0	FEC ok	
		1	FEC error	uncorrectable error detected in EEP array, VOUT will be set to GND level
6	CLAMPED_H	0	no clamping	
		1	upper clamping level exceeded	reset only by a read access
5	CLAMPED_L	0	no clamping	
		1	lower clamping level under-run	reset only by a read access
4	MARG_FAIL	0	margin threshold not reached during last test	
		1	margin threshold reached during last test; at least one EEP register toggled	reset only by a read access
3	reserved			
2:1	reserved	0		
0	TSTMD_ACT	0	test mode inactive	
		1	test mode activated	

Figure 28 Address 0x08: CSR Register[1)]

1) Clamping only available for KP126

bit	function	value	description	remark
9:6	TSTMUX_SEL	0	analog test mux select	see detailed description of analog test modes
5	TEST_TC	0	TempComp normal operation	
		1	TempComp test	set TC virtually to 125°C
4	TCQ_OFF	0	quadratic coefficients of TempComp enabled	
		1	quadratic coefficients of TempComp disabled	
3:0	TSTMD	0	test mode select	see detailed description of test mode selection bits

Figure 29 Address 0x09: TSTCTRL Register[1) 2)]

bit	function	value	description	remark
9	CALC_FEC	0	no effect	write access only (self clearing)
		1	calculate FEC from EEP registers	result is stored in status register (FEC_ACT / ERR)
8	FEC_OFF	0	FEC enabled	
		1	FEC disabled	
7	SET_CKB_ODD	0	no effect	
		1	set EEP registers to odd checkerboard pattern	sets odd bits in even rows and even bits in odd rows to one, all other bits to zero
6	SET_CKB_EVEN	0	no effect	
		1	set EEP registers to even checkerboard pattern	sets even bits in even rows and odd bits in odd rows to one, all other bits to zero
5	SET_ZEROS	0	no effect	
		1	set all EEP registers to zero	
4	SET_ONES	0	no effect	
		1	set all EEP registers to one	
3	reserved			For internal use only
2:0	EEP_MODE	0	EEP mode select (see detailed description of EEP_MODE bits)	write access only (self clearing)

Figure 30 Address 0x0A: EEPCTRL Register[3)]

Bits 2:0 for the EEPROM mode can have the values shown in **Figure 31**.

1) TCQ_OFF is updated from EEP during startup.
2) Refer to **Chapter 7.4** for test mode description.
3) Only one of the four SET bits (7:4) must be enabled at the same time, otherwise no action will be taken. For those bits only write access is allowed (self clearing).

EEP_MODE(2:0)	description
000	standby (default)
001	write
010	erase
011	refresh
100	margin
101	margin_z
110	reserved
111	reserved

Figure 31 EEPROM Modes

Standby mode

Standby mode is the default mode of the EEPROM array. In test mode rows EE0 to EE6 can be accessed via SPI commands.

Refresh mode

In refresh mode the content of the EEP_cells is copied into the corresponding EEP_registers. This also means that in test mode written content in the EEP_registers is obsolete. Signal path - registers will only be updated when test mode is left. If FEC is enabled the row and column parity of the EEPROM array is checked and the result is stored in the status register.

Margin mode

Margin mode is used to check the amount of charge on the floating gates of the EEPROM cells (refer to **"EEPROM Margin Page" on Page 18**).

The margin mode gives a confirmation about the stored charge inside an E²PROM cell and therewith the possibility to check the quality of the E²PROM programming. For the E²PROM cells with a programmed "1" the margin voltage can be verified in detail. The cells with a programmed "0" can only be checked if the value is lower than maximum margin level. However, being inside the defined range guarantees data consistency over lifetime.

Figure 32 shows the two ranges for a programmed "1" and "0".

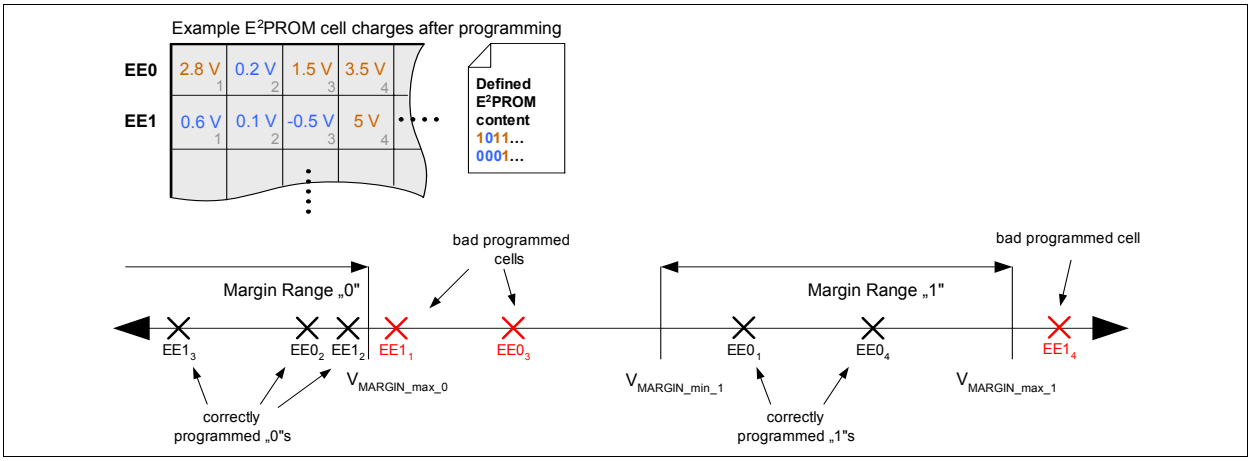


Figure 32 Margin Range

In order to check if programmed "1" cells are within the specified range, the serial command for margin test has to be sent to the E²PROM control register with the $V_{MARGIN\_min\_1}$ voltage level (refer to **Figure 9**). Afterwards, the

entire E²PROM has to be read out. The E²PROM content must be equal to the requested content (refer to **Figure 10**). Then the serial command for margin test must be sent to the E²PROM control register with the $V_{MARGIN\_max\_1}$ voltage level. Now the entire E²PROM content must be "0" (refer to **Figure 10**).

In order to check if programmed "0" cells are within the specified range, the serial command for margin test must be sent to the E²PROM control register with the $V_{MARGIN\_max\_0}$ voltage level. The entire E²PROM has to be read out again. The E²PROM content must be equal to the requested content (refer to **Figure 10**).

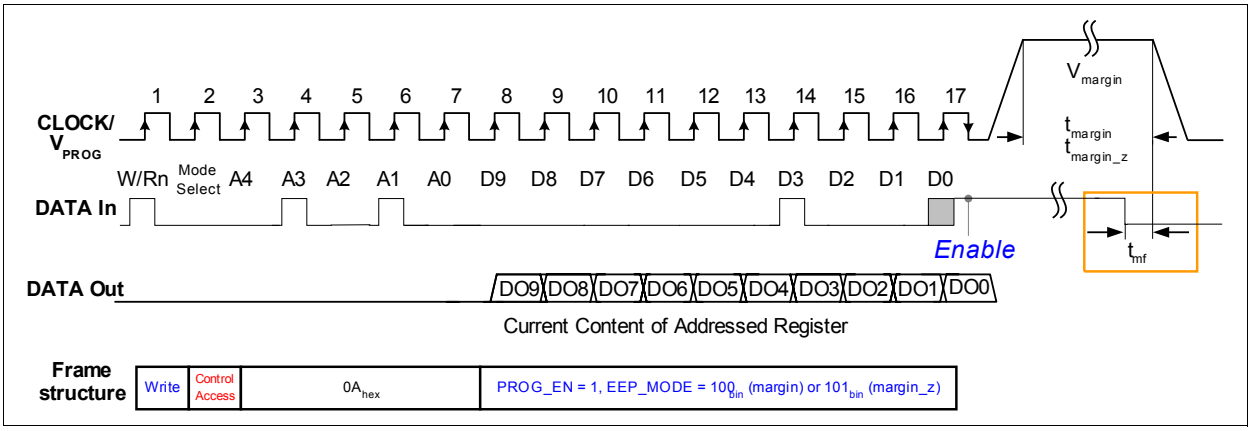


Figure 33 Serial command E²PROM margin mode

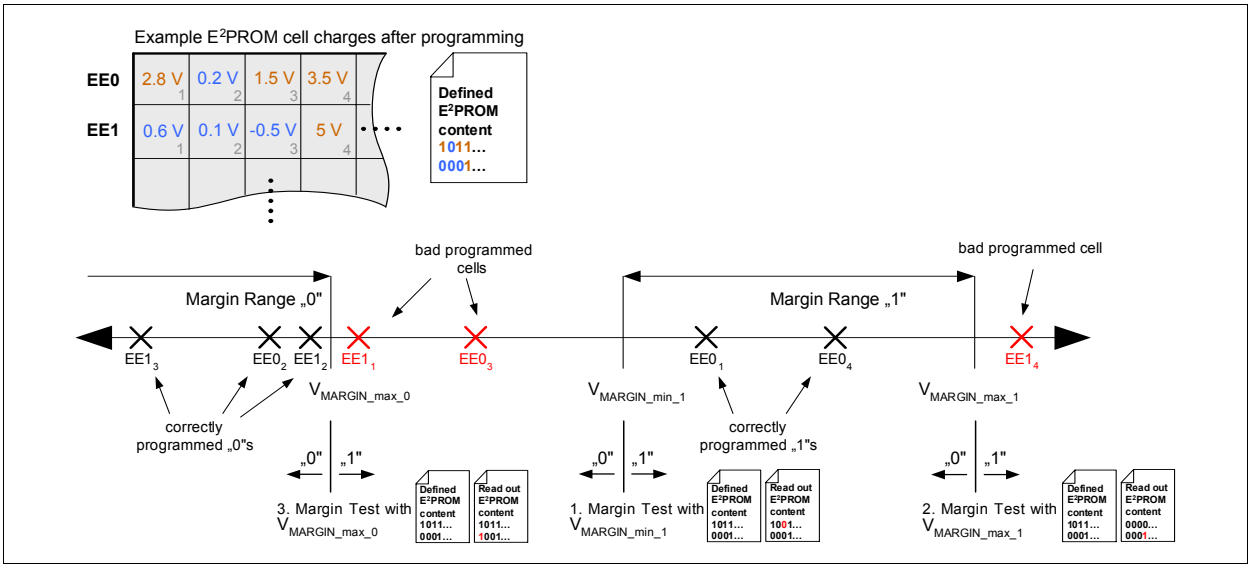


Figure 34 Margin Test

The routine described above ensures that the programmed cells are inside the specified range. To optimize the programming tool it is recommended to do a more detailed margin test for the programmed "1" cells. Therein, the margin test has to be done several times with an increasing margin voltage (Recommendation: 25 mV step size). By comparing the E²PROM readout of the previous mode step with the current step, which drives a flip from “1” to “0”, defines the margin voltage (bit 4 of the register 08_{hex} = “1” indicates that at least one bit toggled). The target where most of the "1" programmed cells are flipped should be directly in the middle between $V_{MARGIN\_min\_1}$ and $V_{MARGIN\_max\_1}$. To optimize the E²PROM programming it is only allowed to modify the programming time t_{PROG_1} and t_{PROG_0} proportionally inside the given range.

bit	function	description	remark
9:0	DAC	read/write value of output DAC	write access only possible when DAC test mode is active

Figure 35 Address 0x0B: DAC Register

bit	function	value	description	range
9:7	reserved	0		
6	Sensitivity	0	Normal	nominal sensitivity range
		1	Increased	increased sensitivity range
5:0	SDG		SD converter gain setting	0 … 63; 0 = max. sensitivity

Figure 36 Address 0x0C: SDG Register[1)]

bit	function	value	description	range
9:4	reserved	0		
3:0	GOF		global offset of SD converter	Fehler! Textmarke nicht definiert. 0 (upper limit)… 15 (lower limit)

Figure 37 Address 0x0D: GOF Register[2)]

bit	function	value	description	range
9:5	reserved	0		
4:0	FOF		fine offset of SD converter	Fehler! Textmarke nicht definiert. -16 … 15

Figure 38 Address 0x0E: FOF Register[1)]

bit	function	value	description	range
9:7	reserved	0		
6:0	TOL		linear offset of TempComp	Fehler! Textmarke nicht definiert. -64 … 63

Figure 39 Address 0x0F: TOL Register[1)]

bit	function	value	description	range
9:5	reserved	0		
4:0	TOQ		quadratic offset of TempComp	Fehler! Textmarke nicht definiert. -16 … 15

Figure 40 Address 0x10: TOQ Register[1)]

1) Values are set during calibration
2) Values are set during calibration

bit	function	value	description	range
9:6	reserved	0		
5:0	TGL		linear gain of TempComp	Fehler! Textmarke nicht definiert. -32… 31

Figure 41 Address 0x11: TGL Register[1)]

bit	function	value	description	range
9:4	reserved	0		
3:0	TGQ		quadratic gain of TempComp	[1] -8 … 7

Figure 42 Address 0x12: TGQ Register[1)]

bit	function	value	description	remark
9:0	IIR_LSB		read IIR values from filter / write IIR values into linearization	lower 10 bits of 12 bit IIR value write access only possible when signal path test is active

Figure 43 Address 0x13: IIR_LSB Register

bit	function	value	description	remark
9:2	reserved	0		
1:0	IIR_MSB		read IIR values from filter / write IIR values into linearization	upper 2 bits of 12 bit IIR value, write access only possible when signal path test is active

Figure 44 Address 0x14: IIR_MSB Register

bit	function	value	description	remark
9:0	LIN_LSB	0	linearization output	lower 10 bits of 12 bit linearization value, only read access possible

Figure 45 Address 0x15: LIN_LSB Register[1)]

bit	function	value	description	remark
9:2	reserved	0		
1:0	LIN_MSB		linearization output	upper 2 bits of 12 bit linearization value, only read access possible

Figure 46 Address 0x16: LIN_MSB Register[1)]

1) Values are set during calibration

7.4 Test Modes

Test mode must be activated by writing “2CEh” to the status register (Addr. 08h). Any other sequence written to the status register disables the test mode and brings the chip back to normal operation. The cyclic EEPROM refresh and the FEC ERR / ACT flag calculation is deactivated in test mode, therefore refresh and calc FEC has to be triggered manually.

Available test modes are encoded in four bits in the test mode selection register (see **Figure 29**). Therefore only 1 test is selectable at a time. The Iddq test mode and the scan test mode can only be deactivated by a power on reset. Available test modes are shown in **Figure 44**.

TSTMD(3:0)	description
0000	no test (default)
0001	diag1
0010	diag2
0011	reserved
0100	analog measurement
0101	reserved
0110	reserved
0111	clock test, internal 3MHz clock switched to data_out
1000	sd-stream test, SD data stream switched to data_out
1001	reset test
1010	contact test, VDD can be measured on V_{out}
1011	DAC test
1100	reserved
1101	reserved
1110	reserved
1111	reserved

Figure 47 Available Test Modes

Diag 1

In this mode, the sensing elements are disconnected from the complete signal path. The sensor gets an input the correlates to a mid input pressure. By this the whole signal path can be checked without the pressure cells.

Diag 2

In this mode, malfunction of the sensor cell can be detected (e.g. broken membrane). The User’s Manual provides the optimal concept by realizing two separate pressure cells. In the normal mode the two sensing and reference cells are connected in a Wheatstone bridge. In Diag2 mode the cells are switched in a way that sensing and reference cells are parallel within the Wheatstone bridge (refer to **Figure 45**).

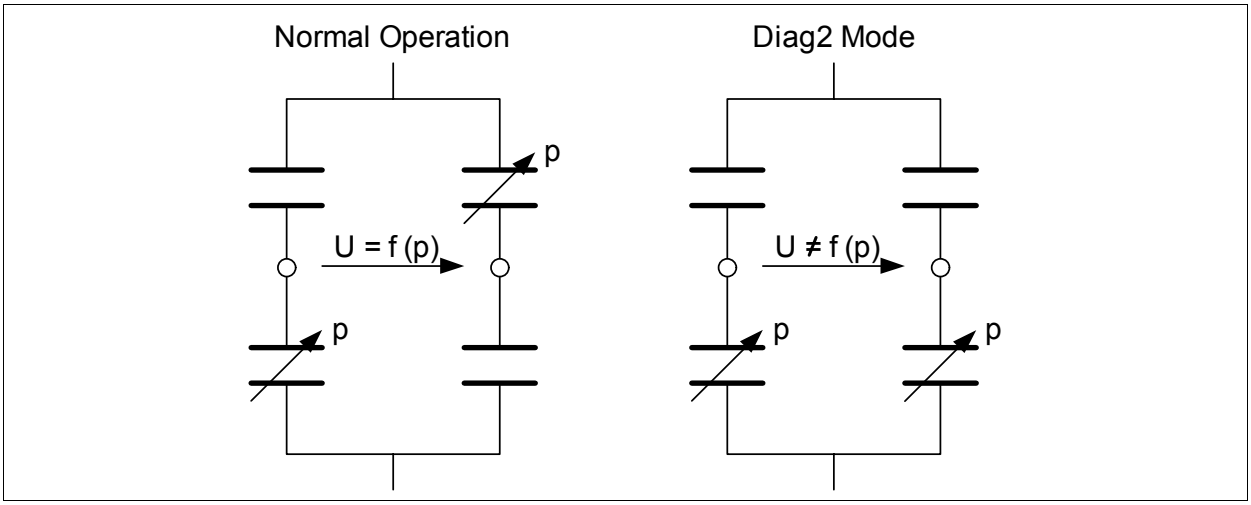


Figure 48 Diag 2 functionality

The output value measured in Diag 2 mode is pressure independent and must be inside a sensor's individual range. Limits of this range could be stored on application level and be used for pressure cell diagnosis.

Analog measurement

If *analog measurement* is selected, several internal voltages can be switched to the DATA_OUT pad. The internal voltages are selected via the analog test multiplexer (see **Figure 46**).

TSTMUX_SEL(3:0)	description	data_out
0000	no test (default)	open
0001	reserved	GND
0010	reserved	GND
0011	reserved	GND
0100	reserved	GND
0101	analog supply	VDDA
0110	reserved	GND
0111	reserved	GND
1000	reserved	GND
1001	reserved	GND
1010	reserved	GND
1011	reserved	GND
1100	digital supply	VDDD
1101	reserved	GND
1110	digital supply	VDDQ
1111	reserved	GND

Figure 49 Analog Test Multiplexer

Clock Test

In clock test mode the internal 3 MHz clock is switched to DATA_OUT pin.

SD-Stream Test

In SD-Stream test mode the Sigmadelta stream is switched to DATA_OUT pin.

Contact Test

In contact test mode V_{DD} can be measured on V_{out} pin.

DAC Test

In DAC test mode a digital input value between 0 and 1023 can be written to the DAC input register and the respective output value can be measured at the V_{out} pin.

7.5 Communication Conditions

7.5.1 Communication Pad Parameters

Table 3 Input Pad CLOCK/V_{PROG} (Clock Mode)[1)]

V_{DD} = 5.0V, GND = 0V, T_A = 20°C to 30°C

Parameter	Symbol	Values			Unit	Note / Test Condition
		min.	typ.	max.		
'H' Input voltage	V_{HCLK}	2.2	–	3.2	V	
'L' Input voltage	V_{LCLK}	0	–	0.5	V	

1) Not subject to production test - verified by characterization/design.

Table 4 Input Pad DATA IN[1)]

V_{DD} = 5.0V, GND = 0V, T_A = 20°C to 30°C

Parameter	Symbol	Values			Unit	Note / Test Condition
		min.	typ.	max.		
Input capacitance	C_{DTA_IN}	–	10		pF	
'H' Input voltage	V_{HDIN}	2.2	–	3.2	V	
'L' Input voltage	V_{LDIN}	0	–	0.5	V	

1) Not subject to production test - verified by characterization/design.

Table 5 Output Pad DATA OUT[1)]

V_{DD} = 5.0V, GND = 0V, T_A = 20°C to 30°C

Parameter	Symbol	Values			Unit	Note / Test Condition
		min.	typ.	max.		
'H' output current	I_{OH}	–	–	0.1	mA	
'L' output current	I_{OL}	-0.1	–	–	mA	
'H' output voltage	V_{HDOUT}	2.3	–	3.4	V	
'L' output voltage	V_{LDOUT}	0	–	1	V	

1) Not subject to production test - verified by characterization/design.

7.5.2 Bus Timing

Table 6 Bus Timing and Tolerances[1)]

V_{DD} = 5.0V, GND = 0V, T_A = 20°C to 30°C

Parameter	Symbol	Values			Unit	Note / Test Condition
		min.	typ.	max.		
Clock frequency	f_{CLK}	1	–	250	kHz	
Clock 'H' pulse width	t_{CLKH}	2	–	–	µs	
Clock 'L' pulse width	t_{CLKL}	2	–	–	µs	
DATA IN setup time	t_{SU}	0	–	–	µs	
DATA IN hold time	t_H	2	–	–	µs	
DATA OUT delay time	t_D	–	–	1	µs	

1) Not subject to production test - verified by characterization/design.

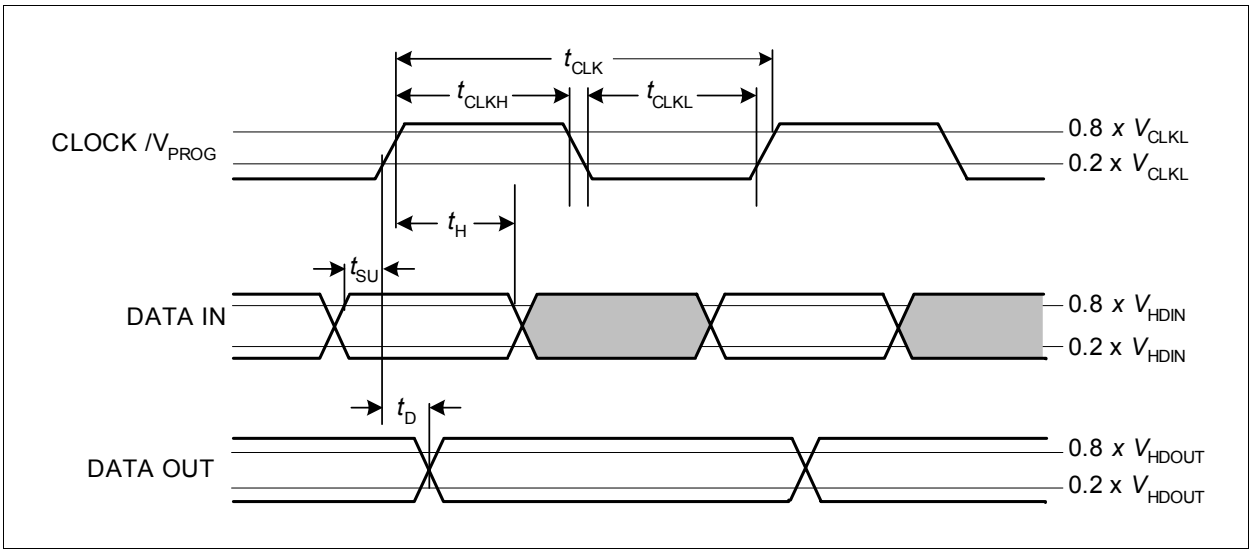


Figure 50 Definition of timing parameters

Note: DATA IN has always to be low on the falling clock edge. Only on the last falling clock edge of a write frame DATA IN must be high to generate an enable condition and to complete the data frame. Setup time and hold time for the enable are the same as for the data, i.e. a setup time of 0µs before the falling clock edge and a hold time of at least 2µs after detecting the falling clock edge is necessary.

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