

PIIPM50P12B004



Programmable Isolated IPM

PI-IPM Features:

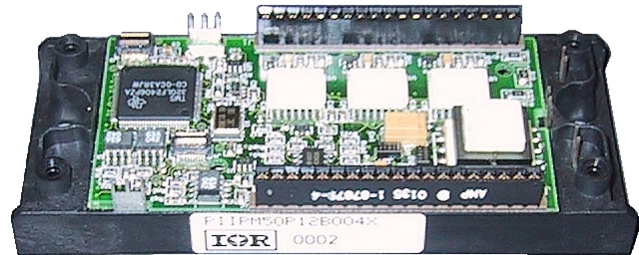
■ Power Module:

- NPT IGBTs 50A, 1200V
- 10us Short Circuit capability
 - Square RBSOA
 - Low $V_{ce(on)}$ (2.15Vtyp @ 50A, 25°C)
 - Positive $V_{ce(on)}$ temperature coefficient
- Gen III HexFred Technology
 - Low diode V_F (1.78Vtyp @ 50A, 25°C)
 - Soft reverse recovery
- 2mΩ sensing resistors on all phase outputs and DCbus minus rail
 - T/C < 50ppm/°C

■ Embedded driving board

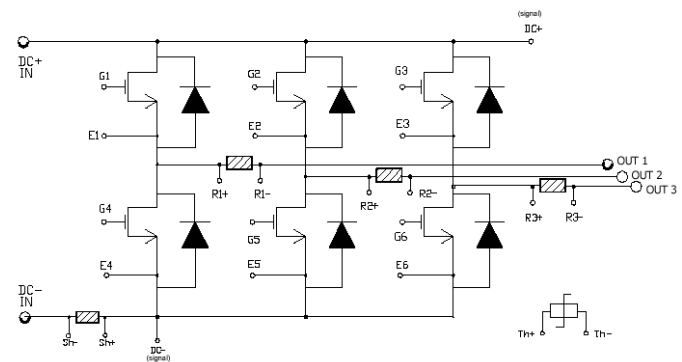
- Programmable 40 Mips DSP
- Current sensing feedback from all phases
- Full protection from ground and line to line faults
- UVLO, OVLO on DCbus voltage
- Embedded flyback smps for floating stages (single 15Vdc @ 300mA input required)
- Asynchronous isolated 2.5Mbps serial port for DSP communication and programming
- IEEE standard 1149.1 (JTAG port interface) for program downloading and debugging
- Separated turn on / turn off outputs for IGBTs di/dt control
- Isolated serial port input with strobe signal for quadrature encoders or SPI communication

Package:



PI-IPM – Inverter (EconoPack 2 outline compatible)

Power Module schematic:



Three phase inverter with current sensing resistors on all output phases

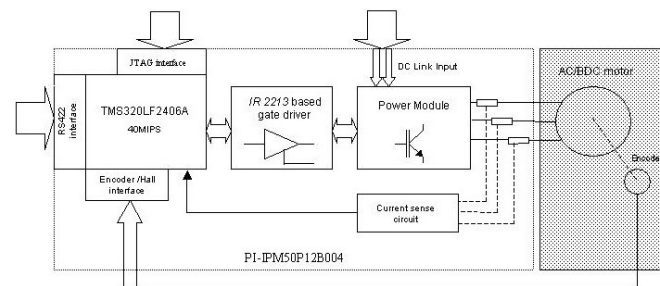
Description

The PIIPM50P12B004 is a fully integrated Intelligent Power Module for high performances Servo Motor Driver applications. The device core is a state of the art DSP, the TMS320LF2406A* at 40 Mips, interfaced with a full set of peripheral designed to handle all analog feedback and control signals needed to correctly manage the power section of the device. The PIIPM has been designed and tailored to implement internally all functions needed to close the current, speed and position loops of a high performances servo motor driver.

The use of the flash memory version of the DSP and the JTAG port connector allows the user to easily develop and download his own proprietary algorithm.

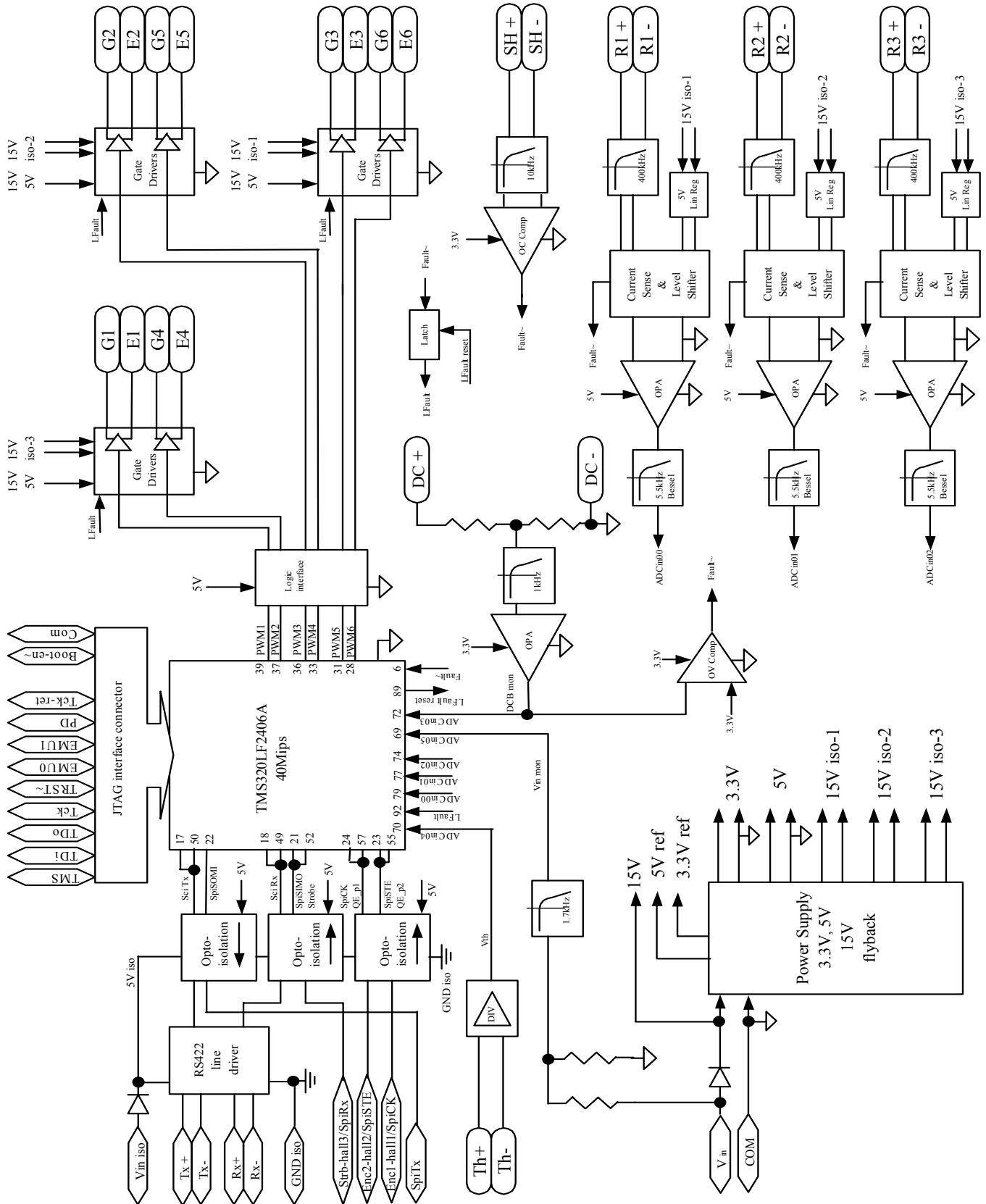
The device comes in the EMP™ package, fully compatible in length, width and height with the popular EconoPack 2 outline.

PI-IPM System Block Schematic:



*Part numbers ending with X may come with the TMS320LF2406 at 30Mips, please refer to TI datasheet, for further information about performances.

Detailed Block Diagram



Signal pins on RS422 serial port

| Symbol | Lead Description | Pin number | |
|-----------------------|---|------------|----------------------------------|
| Vin iso | External 5V supply voltage for opto-couplers and line driver supply | 6 | RS422 serial port |
| GND iso | External 5V supply ground reference for opto-couplers and line driver supply | 7 | |
| Tx+ | RS422 Trasmmitter Non inverting Driver Output | 1 | |
| Tx- | RS422 Trasmmitter Inverting Driver Output | 2 | |
| Rx+ | RS422 Receiver Non inverting Driver Input, | 4 | |
| Rx- | RS422 Receiver Inverting Driver Input | 3 | |
| Enc1 – Hall1 / SpiCK | Incremental Encoder 1 / Hall effect sensor input 1/ SpiCK input (GND iso referenced) | 5 | |
| Enc2 – Hall2 / SpiSTE | Incremental Encoder 2 / Hall effect sensor input 2 / SpiSTE input (GND iso referenced) | 9 | |
| Strb – Hall3 / SpiRx | Incremental Encoder Strobe / Hall effect sensor input 3 / SpiRx input (GND iso ref.) Also used for DSP boot feature using DSP boot ROM. Please see note below. | 10 | |
| SpiTx | SpiTx output (GND iso referenced) | 8 | |
| Vin | External 15V supply voltage. Internally referred to DC bus minus pin (DC -) | 17-18 | |
| COM | External 15V supply ground reference. This pin is directly connected to DC - | 19-20 | |

Signal pins on IEEE1149.1 JTAG connector

CAUTION DO NOT APPLY DC BUS VOLTAGE WHEN JTAG INTERFACE IS CONNECTED, SEVERE DAMAGE WILL OCCUR ON POWER MODULE AND ON YOUR EQUIPMENT!

| Symbol | Lead Description | State | Pin number | |
|-----------|--|--------|------------|----------------------------|
| TMS | JTAG test mode select | Input | 12 | IEEE1149.1 JTAG |
| TMS2 | JTAG test mode select 2 | Input | 5-6 | |
| TDI | JTAG test data input | Input | 14 | |
| TDO | JTAG test data output | Output | 13 | |
| TCK | JTAG test clock. TCK is a 10MHz clock source from the emulation pod. This signal can be used to drive the system test clock. | Input | 15 | |
| TRST~ | JTAG test reset | Input | 11 | |
| EMU0 | Emulation pin 0 | I/O | 9-10 | |
| EMU1/OFF~ | Emulation pin 1 | I/O | 7-8 | |
| PD | Presence detect. Indicates that the emulation cable is connected and that the PI-IPM log ic is powered up. PD is tied to the DSP 3.3V supply through a 1k resistor. | Output | 1 | |
| TCK_RET | JTAG test clock return. Test clock input to the emulator. Internally short circuited to TCK. | Output | 16 | |
| Boot-En~ | Boot ROM enable. This pin is sampled during DSP reset, pulling it low enables DSP boot ROM (Flash version only). 47k internal pull-up. Please see note below. | Input | 17 | |
| COM | External 15V supply ground reference. This pin is directly connected to DC- | N/A | 20 | |

~ indicates active low signals

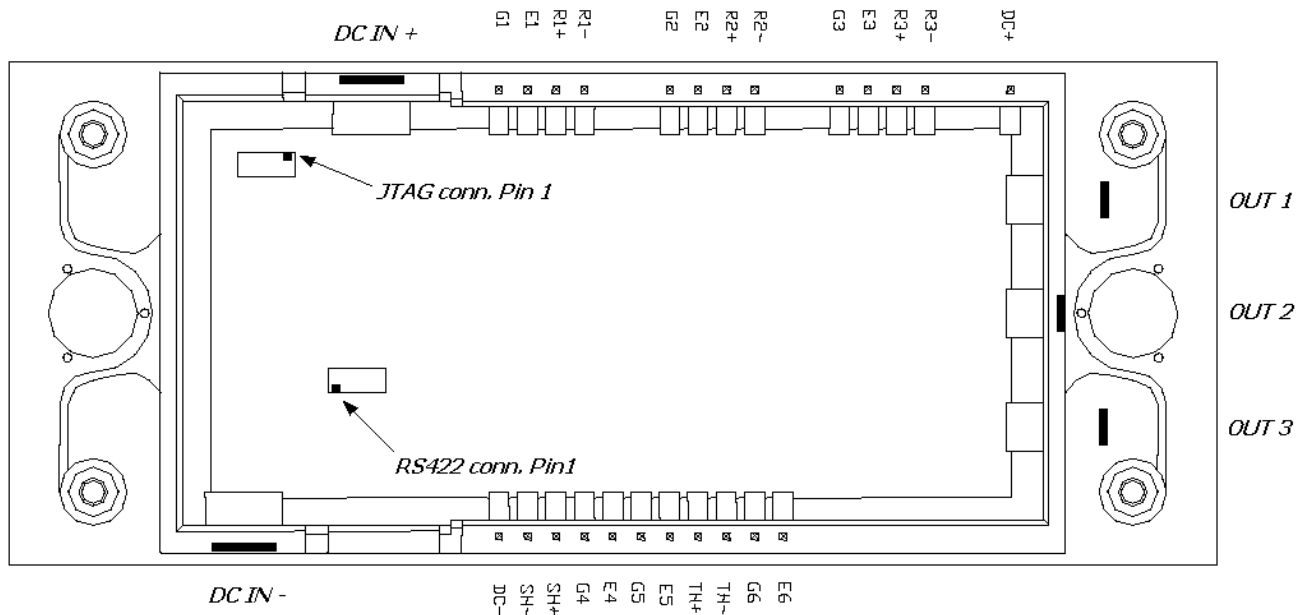
¹ To enable DSP boot ROM for boot load feature through SCI at 40Mhz clock operation follow these steps:

- 1) Connect Boot-En~ to COM;
- 2) Connect STR – Hall3 / SpiRx to GND iso;
- 3) Apply voltage to Vin iso;
- 4) Apply-voltage to Vin (after Vin iso to allow proper configuration).

Following pins are intended for signal communication between driving board and power module only, though here described for completeness, they are on purpose not available to the user.

| Symbol | Lead Description | Pin number |
|----------|---|--|
| DC + | DC Bus plus input signal | Lateral connectors on embedded driving board |
| DC - | DC Bus minus input signal (internally connected to COM) | |
| Th + | Thermal sensor positive input | |
| Th - | Thermal sensor negative input (internally connected to COM) | |
| Sh + | DC Bus minus series shunt positive input (Kelvin point) | |
| Sh - | DC Bus minus series shunt negative input (Kelvin point) | |
| G1/2/3 | Gate connections for high side IGBTs | |
| E1/2/3 | Emitter connections for high side IGBTs (Kelvin points) | |
| R1/2/3 + | Output current sensing resistor positive input (IGBTs emitters 1/2/3 side, Kelvin points) | |
| R1/2/3 - | Output current sensing resistor negative input (Motor side, Kelvin points) | |
| G4/5/6 | Gate connections for low side IGBTs | |
| E4/5/6 | Emitter connections for low side IGBTs (Kelvin points) | |

Power Module Frame Pins Mapping



Absolute Maximum Ratings ($T_C=25^\circ\text{C}$)

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur.

All voltage parameters are absolute voltages referenced to V_{DC-} , all currents are defined positive into any lead.

Thermal Resistance and Power Dissipation ratings are measured at still air conditions.

| | Symbol | Parameter Definition | Min. | Max. | Units |
|-------------------------------|--|---|----------|-------------|--------|
| Inverter | V_{DC} | DC Bus Voltage | 0 | 1000 | V |
| | V_{CES} | Collector Emitter Voltage | 0 | 1200 | |
| | $I_C @ 100^\circ\text{C}$ | IGBTs continuous collector current ($T_C = 100^\circ\text{C}$) | | 50 | A |
| | $I_C @ 25^\circ\text{C}$ | IGBTs continuous collector current ($T_C = 25^\circ\text{C}$) | | 100 | |
| | I_{CM} | Pulsed Collector Current (Fig. 3, Fig. CT.5) | | 200 | |
| | $I_F @ 100^\circ\text{C}$ | Diode Continuous Forward Current ($T_C = 100^\circ\text{C}$) | | 50 | |
| | $I_F @ 25^\circ\text{C}$ | Diode Continuous Forward Current ($T_C = 25^\circ\text{C}$) | | 100 | |
| | I_{FM} | Diode Maximum Forward Current | | 200 | |
| | V_{GE} | Gate to Emitter Voltage | -20 | +20 | V |
| | $P_D @ 25^\circ\text{C}$ | Power Dissipation (One transistor) | | 354 | W |
| $P_D @ 100^\circ\text{C}$ | Power Dissipation (One transistor, $T_C = 100^\circ\text{C}$) | | 142 | | |
| Embedded Driving Board | V_{in} | Non isolated supply voltage (DC- referenced) | -20 | 20 | V |
| | V_{in-iso} | Isolated supply voltage (GND iso referenced) | -5 | 5.5 | |
| | Rx | RS422 Receiver input voltage (GND iso referenced) | -7 | 12 | |
| | T_{A-EDB} | Operating Ambient Temperature Range | -25 | +70 | °C |
| | $T_{STG-EDB}$ | Board Storage Temperature Range | -40 | +125 | |
| | $V_{ISO-CONT}$ RS232 | Input-Output Continuous Withstand Voltage ($RH \leq 50\%$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$) | AC DC | 800 1000 | V V |
| | $V_{ISO-TEMP}$ RS232 | Input-Output Momentary Withstand Voltage ($RH \leq 50\%$, $t = 1$ min, $T_A = 25^\circ\text{C}$) | RMS | 2500 | V |
| Power Module | MT | Mounting Torque | | 3.5 | Nm |
| | T_J | Operating Junction Temperature | -40 | +150 | °C |
| | T_{STG} | Storage Temperature Range | -40 | +125 | |
| | V_C -iso | Isolation Voltage to Base Copper Plate | -2500 | +2500 | V |

Electrical Characteristics: Inverter

For proper operation the device should be used within the recommended conditions.

T_J = 25°C (unless otherwise specified)

| Symbol | Parameter Definition | Min. | Typ. | Max. | Units | Test Conditions | Fig. |
|---------------------------------------|---|------|------|------|-------|--|--------|
| V _{(BR)CES} | Collector To Emitter Breakdown Voltage | 1200 | | | V | V _{GE} = 0V, I _C = 250μA | |
| ΔV _{(BR)CES / ΔT} | Temperature Coeff. of Breakdown Voltage | | +1.2 | | V/°C | V _{GE} = 0V, I _C = 1mA (25 - 125 °C) | |
| V _{CE(on)} | Collector To Emitter Saturation Voltage | | 2.15 | 2.55 | V | I _C = 50A, V _{GE} = 15V | 5, 6 |
| | | | 2.70 | 3.78 | | I _C = 100A, V _{GE} = 15V | 7, 9 |
| | | | 2.45 | 3.22 | | I _C = 50A, V _{GE} = 15V, T _J = 125 °C | 10, 11 |
| V _{GE(th)} | Gate Threshold Voltage | 4.4 | 4.7 | 5.5 | V | V _{CE} = V _{GE} , I _C = 250μA | 12 |
| ΔV _{GE(th) / ΔT_J} | Temp. Coeff. of Threshold Voltage | | -1.2 | | mV/°C | V _{CE} = V _{GE} , I _C = 1mA (25 - 125 °C) | |
| g _{fe} | Forward Transconductance | 29 | 33 | 38 | S | V _{CE} = 50V, I _C = 50A, PW = 80μs | |
| I _{CES} | Zero Gate Voltage Collector Current | | | 500 | μA | V _{GE} = 0V, V _{CE} = 1200V | |
| | | | 650 | 1350 | | V _{GE} = 0V, V _{CE} = 1200V, T _J = 125 °C | |
| | | | | 4000 | | V _{GE} = 0V, V _{CE} = 1200V, T _J = 150 °C | |
| V _{FM} | Diode Forward Voltage Drop | | 1.78 | 2.12 | V | I _C = 50A | 8 |
| | | | 1.90 | 2.22 | | I _C = 50A, T _J = 125 °C | 8 |
| I _{RM} | Diode Reverse Leakage Current | | | 20 | μA | V _R = 1200V, T _J = 25 °C | |
| I _{GES} | Gate To Emitter Leakage Current | | | ±200 | nA | V _{GE} = 20V | |
| R1/2/3 | Sensing Resistors | 1.98 | 2 | 2.02 | mΩ | | |
| Rsh | DC bus minus series shunt resistor | 1.98 | 2 | 2.02 | | | |

Switching Characteristics: Inverter

For proper operation the device should be used within the recommended conditions.

T_J = 25°C (unless otherwise specified)

| Symbol | Parameter Definition | Min | Typ | Max | Units | Test Conditions | Fig. |
|----------------------|---|-------------|-------|-------|-------|---|------------------------------------|
| Q _g | Total Gate Charge (turn off) | | 400 | 411 | nC | I _C = 50A | 23 CT1 |
| Q _{ge} | Gate – Emitter Charge (turn off) | | 46 | 55 | | V _{CC} = 600V | |
| Q _{gc} | Gate – Collector Charge (turn off) | | 181 | 200 | | V _{GE} = 15V | |
| E _{on} | Turn on Switching Loss | | 2814 | 3220 | μJ | I _C = 50A, V _{CC} = 600V, T _J = 25 °C | CT4 WF1 WF2 |
| E _{off} | Turn off Switching Loss | | 5293 | 5825 | | V _{GE} = 15V, R _G = 10Ω, L = 250μH | |
| E _{tot} | Total Switching Loss | | 8107 | 9145 | | Tail and Diode Rev. Recovery included | |
| E _{on} | Turn on Switching Loss | | 3963 | 4415 | μJ | I _C = 50A, V _{CC} = 600V, T _J = 125 °C | 13, 15 CT4 WF1 WF2 |
| E _{off} | Turn off Switching Loss | | 7810 | 8965 | | V _{GE} = 15V, R _G = 10Ω, L = 250μH | |
| E _{tot} | Total Switching Loss | | 11773 | 13380 | | Tail and Diode Rev. Recovery included | |
| t _d (on) | Turn on delay time | | 66 | 72 | ns | I _C = 50A, V _{CC} = 600V, T _J = 125 °C V _{GE} = 15V, R _G = 10Ω, L = 250μH | 14,16 CT4 WF1 WF2 |
| T _r | Rise time | | 72 | 83 | | | |
| t _d (off) | Turn off delay time | | 593 | 641 | | | |
| T _f | Fall time | | 95 | 117 | | | |
| C _{ies} | Input Capacitance | | 5884 | 6052 | pF | V _{CC} = 30V | 22 |
| C _{oes} | Output Capacitance | | 950 | 968 | | V _{GE} = 0V | |
| C _{res} | Reverse Transfer Capacitance | | 167 | 193 | | f = 1MHz | |
| RBSOA | Reverse Bias Safe Operating Area | FULL SQUARE | | | | T _J = 150 °C, I _C = 200A, V _{GE} = 15V to 0V V _{CC} = 1000V, V _p = 1200V, R _G = 5Ω | 4 CT2 |
| SCSOA | Short Circuit Safe Operating Area | 10 | | | μs | T _J = 150 °C, V _{GE} = 15V to 0V V _{CC} = 900V, V _p = 1200V, R _G = 5Ω | CT3 WF4 |
| E _{REC} | Diode reverse recovery energy | 693 | 1114 | 1535 | μJ | T _J = 125 °C | 17,18 19,20 21 CT4 WF3 |
| t _{rr} | Diode reverse recovery time | 156 | 260 | 363 | ns | I _F = 50A, V _{CC} = 600V, | |
| I _{rr} | Peak reverse recovery current | 35 | 42 | 43 | A | V _{GE} = 15V, R _G = 10Ω, L = 250μH | |
| R _{thJC-T} | Each IGBT to copper plate thermal resistance | | | 0.35 | °C/W | See also fig.24 and 25 | 24,25 |
| R _{thJC-D} | Each Diode to copper plate thermal resistance | | | 0.70 | °C/W | | |
| R _{thC-H} | Module copper plate to heat sink thermal resistance. Silicon grease applied = 0.1mm | | | 0.03 | °C/W | | |
| P _{diss} | Total Dissipated Power | | 100 | | W | I _C = 7A, V _{DC} = 530V, f _{sw} = 8kHz, T _C = 55 °C | PD1 |
| | | | 150 | | | I _C = 10A, V _{DC} = 530V, f _{sw} = 8kHz, T _C = 55 °C | PD2 |
| | | | 250 | | | I _C = 10A, V _{DC} = 530V, f _{sw} = 16kHz T _C = 55 °C, | PD3 |
| | | | 200 | | | I _C = 20A, V _{DC} = 530V, f _{sw} = 4kHz, T _C = 40°C | |

Electrical Characteristics: Embedded Driving Board (EDB) communication ports

For proper operation the device should be used within the recommended conditions.

V_{in} = 15V, V_{in-iso} = 5V, T_A = 0 to 55C, T_C = 75C (unless otherwise specified)

| Symbol | Parameter Definition | Min. | Typ. | Max. | Units | Test Conditions | Conn. |
|--|---|--|------|------|-------|---|------------|
| V _{in} | EDB Input supply Voltage | 12 | 15 | 18 | V | | RS422 port |
| I _{supp} | EDB input Supply Current with EEprom not programmed | 90 | 100 | 110 | mA | | |
| I _{supp} | EDB Input Supply Current | 131 | 149 | 166 | mA | V _{DC} = 0V, f _{PWM} = 8kHz (*) | |
| I _{supp} | EDB Input Supply Current | 132 | 152 | 170 | mA | V _{dc} =600V, f _{PWM} = 8kHz (*) | |
| V _{in iso} | EDB isolated supply voltage | 4.5 | 5 | 5.5 | V | | |
| I _{q. iso} | EDB isolated quiescent supply current | | 9 | 20 | mA | R _{x+} = +5V, R _{x-} = 0V Hall1/2/3 = open | |
| I _{supp. iso} | EDB isolated supply current | 24 | 29 | 34 | mA | Hall1/2/3 low R _{x+} = 0V, R _{x-} = +5V Tx+ and Tx- open | |
| | | 37 | 48 | 59 | mA | Hall1/2/3 low R _{x+} = 0V, R _{x-} = +5V Tx+ and Tx- on 120Ω | |
| V _{DO-TX} | Differential Driver Output Voltage | 2 | | | V | R _{load} = 120 Ω | RS422 port |
| V _{CO-TX} | Driver Common mode output voltage | | | 3 | V | | |
| V _{DI-RX} | Receiver Input Differential Threshold Voltage | -0.2 | | 0.2 | V | -7V ≤ V _{CM} ≤ +12V | |
| R _{IN-RX} | Receiver Input Resistance | | 120 | | Ω | | |
| f _{MAX} | RS422 maximum data rate | | | 2.5 | Mbps | | |
| V _{enc-high} / V _{hall-high} | Logic High Input Voltage | 3.6 | | | V | Enc1 / Hall1 Enc2 / Hall2 Strb / Hall3 input pins | RS422 port |
| V _{enc-low} / V _{hall-low} | Logic Low Input Voltage | | | 2 | V | | |
| I _{enc-low} / I _{hall-low} | Logic Low Input Current | -5.2 | | | mA | | |
| TMS TMS2 TDI TDO TCK TRST- EMU0 EMU1/OFF~ PD | JTAG interface pins | Please see TMS320LF2406A datasheet from Texas Instruments and V _{PD} specifications | | | | Directly connected from DSP to connector pins. EMU0 and EMU1 with 4.7k internal pull up. | JTAG |
| V _{PD} | Presence detect voltage | 3.2 | 3.3 | 3.4 | V | I _{PD} = -100μA | JTAG |
| V _{Boot-En~} | Boot ROM enable input voltage | | | 0.5 | V | Active low | JTAG |
| I _{Boot-En~} | Boot ROM enable input current | | | -100 | μA | | |

~ indicates active low signals

* these values are obtained with internal DSP clock, EVA, EVB, SCI peripherals enabled at 40MHz, A/D peripheral at 20MHz and 50% PWM duty cycle on all legs.

AC Electrical Characteristics: Embedded Driving Board (EDB)

DSP pins mapping

For proper operation the device should be used within the recommended conditions.

V_{in} = 15V, V_{in-iso} = 5V, T_A = 0 to 55C, T_C = 75C (unless otherwise specified)

| Symbol | Parameter Definition | Min. | Typ. | Max. | Units | Test Conditions | DSP name ; pin N |
|-----------------------|--|--|------|------|-------|-----------------|---|
| V _{DCgain} | DC bus voltage feedback partition coefficient | 2.39 | 2.44 | 2.49 | mV/V | | ADCin03;72 |
| V _{DC-MAX} | Maximun DC bus voltage read | 1309 | | | V | | |
| V _{DCpole} | DC bus voltage feedback filter pole | 950 | 1000 | 1050 | Hz | | |
| V _{DC-OVth} | DC bus voltage over-voltage threshold | 870 | 920 | 970 | V | | PDPINTA;6 |
| V _{TH25C} | Thermal sensor voltage feedback at 25 °C (Fig. TF1) | 2.65 | 2.75 | 2.85 | V | | ADCin04;70 |
| V _{TH100C} | Thermal sensor voltage feedback at 100 °C (Fig. TF1) | 1.04 | 1.09 | 1.14 | V | | |
| V _{in-gain} | Input voltage feedback partition coefficient | 125 | 128 | 131 | mV/V | | ADCin05;69 |
| V _{in-pole} | Input voltage feedback filter pole | 1600 | 1700 | 1800 | Hz | | |
| I _{ph-GAIN} | Current feedback gain | 16.6 | 16.9 | 17.2 | mV/A | all phases | ADCin00: 79 ADCin01: 77 ADCin02: 74 |
| I _{ph-pole} | Current feedback filter pole | 5.0 | 5.5 | 6.0 | kHz | | |
| I _{ph-MAX} | Maximun Current feedback read | 95 | | | A | | |
| I _{ph-MIN} | Minimum Current feedback read | | | -95 | A | | |
| I _{ph-LAT} | Current feedback signal delay | | | 12 | μs | | |
| I _{ph-Zero} | Zero current input voltage level | 1.64 | 1.67 | 1.70 | V | | |
| I _{sc} | Short Circuit Threshold Current | 110 | 128 | 146 | A | all phases | PDPINTA;6 |
| I _{sc-DEL} | Short Circuit detection delay time | | 3 | 6 | μs | all phases | |
| DC _{Oc} | DC bus minus over-current level | 130 | 140 | 150 | A | DC bus minus | PDPINTA;6 |
| DC _{Oc-pole} | DC bus minus over-current filter pole | 14 | 15 | 16 | kHz | DC bus minus | |
| WD | External watchdog timeout (see also RS~ signal) | 0.9 | 1.6 | 2.5 | Sec | | WD;85 |
| COM | DSP Ground | 2, 3, 5, 7, 11, 12, 13, 14, 15, 16, 19, 26, 27, 29, 32, 34, 38, 41, 43, 45, 46, 48, 53, 56, 58, 60, 63, 65, 66, 67, 68, 71, 73, 75, 76, 78, 80, 81, 84, 90, 97 | | | | | |
| 3.3V | DSP 3.3V supply | 4, 10, 20, 30, 35, 47, 54, 59, 64, 91, 98 | | | | | |
| floating | The following pins are left unconnected | 42,44,51,88 | | | | | |
| Ref3.3V | 3.3V reference voltage | | 3.33 | | V | | VCCA,VREFHI; 83,82 |
| | | | | | | | |

~ indicates active low signals

Other DSP pins mapping

| Symbol | Signal Definition | DSP pin name ;pin N | Comments |
|-----------------------|--|--------------------------|---|
| PWM1 | OUT 1 high side IGBT gate drive signal | PWM1;39 | DSP Event Manager A output |
| PWM2 | OUT 1 low side IGBT gate drive signal | PWM2;37 | DSP Event Manager A output |
| PWM3 | OUT 2 high side IGBT gate drive signal | PWM3;36 | DSP Event Manager A output |
| PWM4 | OUT 2 low side IGBT gate drive signal | PWM4;33 | DSP Event Manager A output |
| PWM5 | OUT 3 high side IGBT gate drive signal | PWM5;31 | DSP Event Manager A output |
| PWM6 | OUT 3 low side IGBT gate drive signal | PWM6;28 | DSP Event Manager A output |
| Enc1-Hall1 / SpiCK | Incremental Encoder 1 / Hall effect sensor input 1/ SpiCK input (GND iso referenced) | SPICK;24 QEP1;57 | Optically isolated input |
| Enc2 - Hall2 / SpiSTE | Incremental Encoder 2 / Hall effect sensor input 2 / SpiSTE input (GND iso referenced) | SPISTE~;23 QEP2; 55 | Optically isolated input |
| Strb - Hall3 / SpiRx | Incremental Encoder Strobe / Hall effect sensor input 3 / SpiSIMO input (GND iso ref.) | SPISIMO;21 CAP3; 52 | Optically isolated input |
| SpiTx | SpiSOMI output (GND iso referenced) | SPISOMI;22 | Optically isolated input |
| Ref3.3V | 3.3V reference voltage | Vrefhi;82 Vcca; 83 | 3.33V reference voltage for ADC converter |
| 5V supp. | Flash programming voltage pin | Vccp;40 | Supplied by the embedded flyback regulator |
| Boot En~ | Boot ROM enable signal | BOOT_EN~;86 | See also EDB electrical characteristics |
| Tx | SCI transmit data | SCITXD;17 CANTX ; 50 | Drives Tx+ and Tx- through an opto-isolator and a line driver |
| Rx | SCI receive data | SCIRX ; 18 CANRX ; 49 | Driven by Rx+ and Rx- through an opto-isolator and a line driver |
| LFAULT | System general fault input (latched) | IOPF6;92 | Activated by short circuits on output phases and DC bus minus and by DC bus over-voltage comparator |
| LFAULT reset | System general fault output reset signal | IOPF5;89 | LFAULT Reset signal, to be activated via software after a fault or system boot |
| FAULT~ | System general fault input (not latched) | PDPINTA~;6 | Activated by short circuits on output phases and DC bus minus and by DC bus over-voltage comparator |
| RS~ | DSP reset input signal (see also WD signal) | RS~;93 | Forces a DSP reset if WD signal holds too long (see also EDB electrical char.) |
| Xtal1 | PLL oscillator input pin | XTAL1;87 | A 10Mhz oscillator at 100ppm frequency stability feeds this pin. |
| PLL1 | PLL filter input 1 | PLL1;9 | PLL filter for 40Mhz DSP clock frequency |
| PLL2 | PLL filter input 2 | PLL2;8 | PLL filter for 40Mhz DSP clock frequency |
| PDPINTB | External protection interrupt for EVB | PDPINTB~;95 | Not used pull up 4.7K to 3.3V |
| | | | |

~ indicates active low signals

General Description

The PI-IPM is a new generation of Intelligent Power Module designed specifically to implement itself a complete motor driver system. The device contains all peripherals needed to control a six IGBTs inverter, including voltage, temperature and current output sensing, completely interfaced with a 40Mips DSP, the TMS320LF2406A from Texas Instruments. All communication between the DSP and the local host, including DSP software installing and debugging, is realized through an asynchronous isolated serial port (SCI), an isolated port for incremental encoder inputs or synchronous serial port communication (SPI) is also provided making this module a complete user programmable solution connected to the system only through a serial link cable.

System Description

The PI-IPM is realized in two distinct parts: the Power Module "EMP" and the Embedded Driving Board "EDB," these two elements assembled together constitute the complete device with all performances described in the following.

The complete block schematic showing all functions implemented in the product is represented on the System Block Schematic on page 1. The new module concept includes everything depicted within the dotted line, the EMP power module includes IGBTs, Diodes and Sensing Resistors while all remaining electronics is assembled on the EDB that is fitted on the top of it as a cover with also mechanical protective functions.

Connections between the two parts are realized through a single-in-line connector and the EDB only, without disassembling the power module from the system mechanic, can be easily substituted "at the factory" for an upgrade, a system configuration change (different control architecture) or a board replacement. Also software upgrades are possible but this does not even require any hardware changes thanks to the DSP programmability through the serial or JTAG ports.

THE "EMP™" POWER MODULE

This module contains six IGBTs + HexFreds Diodes in a standard inverter configuration. IGBTs used are the new NPT 1200V-50A (current rating measured @ 100C), generation V from International Rectifier; the HexFred diodes have been designed specifically as pair elements for these power transistors. Thanks to the new design and technologic realization, this gen V devices do not need any negative gate voltage for their complete turn off and the tail effect is also substantially reduced compared to competitive devices of the same family. This feature simplifies the gate driving stage that will be described in a dedicated chapter. Another not standard feature in this type of power modules is the presence of sensing resistors in the three output phases, for precise motor current sensing and short circuit protections, as well as another resistor of the same value in the DC bus minus line, needed only for device protections purposes. A complete schematic of the EMP module is shown on page 1 where sensing resistors have been clearly evidenced, a thermal sensor is also embedded and directly coupled with the DSP inputs.

The package chosen is mechanically compatible with the well known EconoPack outline, also the height of the plastic cylindrical nuts for the external PCB positioned on its top is the same, so that, with the only re-layout of the main motherboard, this module can fit into the same mechanical fixings of the standard Econo II package thus speeding up the device evaluation in an already existing driver.

An important feature of this new device is the presence of Kelvin points for all feedback and command signals between the board and the module with the advantage of having all emitter and resistor sensing independent from the power path. The final benefit is that all low power signal from/to the controlling board are unaffected by parasitic inductances or resistances inevitably present in the module power layout.

The new package outline is show on page 4, all signal and power pins are clearly listed, note that because of high current spikes on those inputs the DC bus power pins are doubled in size comparing to the other power pins. Module technology uses the standard and well know DBC: over a thick Copper base an allumina (Al₂O₃) substrate with a 300µm copper foil on both side is placed and IGBTs and Diodes dies are directly soldered, through screen printing process. These dies are then bonded with a 15 mils aluminum wire for power and signal connections. All components are then completely covered by a silicone gel with mechanical protection and electrical isolation purposes.

THE “EDB” EMBEDDED DRIVING BOARD

This is the core of the device intelligence, all control and driving functions are implemented at this level, the board finds its natural placement as a cover of the module itself and has a double function of mechanical cover and intelligent interface. DSP and all other electronics are here assembled; figure on page 2 shows the board schematic and all connection pins.

Looking at the schematic, all diamond shaped pins are signal connections, some belonging to the RS422 port interface and some to the IEEE 1149.1 (JTAG) connector. All other pins are used for communication between the board and the module, they are positioned laterally in the board and the module doesn’t have any pins in the middle of its body.

From the top left, in anti-clockwise direction we identify the following blocks that will be then described in details:

1. DSP and opto isolated serial and JTAG ports
2. Flyback Power Supply
3. Current Sensing interfaces, over-current protections and signal conditioning
4. Gate drivers
5. DC bus and Input voltage feedback

1. DSP and opto isolated serial and JTAG ports.

The DSP used in this application is the new TMS320LF2406A from TI, it is a improvement of the well known in the motor driver market “F240” used in many motor driver applications. If we compare this new device with the predecessor, the new DSP has some added features that let the software designer significantly improve the system control performances, the following table shows a list of relevant data, for all other information please refer to the related device datasheet. To be noted is the increased number of instruction per second, (40MIPS) and of I/O pins, the availability of a boot ROM and a CAN, a much faster ADC and the reduced supply voltage from 5V down to 3.3V, to follow the global trend for this type of products. The choice of the DSP has been done looking at the high number of applications already existing in the market using devices of this family, however it is clear that the same kind of approach could be followed using products from different suppliers to let the customer work on its preferred and well known platform.

TMS320LF2406A vs TMS320F240

| | ‘F2406 | ‘F240 |
|--------------------|--------|-------|
| MIPS | 40 | 20 |
| RAM | 2.5Kw | 544w |
| Flash | 32Kw | 16Kw |
| ROM | — | — |
| Boot ROM | 256w | — |
| Ext. Memory I/F | — | Yes |
| Event manager | Yes | Yes |
| • GP timers | 4 | 3 |
| • CMP/PWM | 10/16 | 9/12 |
| • CAP/QEP | 6/4 | 4/2 |
| Watchdog timer | Yes | Yes |
| 10-bit ADC | Yes | Yes |
| • Channels | 16 | 16 |
| • Conv. time (min) | 500ns | 6.6µs |
| SPI | Yes | Yes |
| SCI | Yes | Yes |
| CAN | Yes | — |
| Digital I/O pins | 37 | 28 |
| Voltage range | 3.3V | 5 V |

The “2406A” has three different serial interfaces available: SCI, SPI, and CAN bus. In the PI-IPM50P12B004 communication is made through the asynchronous port (SCI) while four other opto-isolated lines can be used for the SPI or for the hall effect sensor interface. Maximum bit rate for this asynchronous serial port is 2.5Mbps while the SPI (synchronous) could reach 10Mbps. The choice of the SCI has been taken for easy interfacing with a standard computer serial port, the only component needed is a line driver to adapt the RS232 voltage standard with the RS422 at 3.3V used on this application.

In a standard Brushless motor application usually 1Mbps are far enough to transmit all information needed for the torque reference updates and other fault and feedback signals at a maximum frame rate of 10kHz (100bits/frame), in this way the on-board line driver let the application use long connecting wires between the host and the module, leaving the user the possibility of having the PI-IPM displaced near the motor, e.g. in its connecting box, thus avoiding long and noisy three phase cables between driver and load.

The JTAG port is the standard one, neither isolation nor signal conditioning are provided here and all signal, except the Tck-ret, are directly connected from the related DSP pins to the connector; however, due to the limited board space, the connector used is not the standard 14 pins at two rows header, then an adaptor has to be realized to connect it to the JTAG adapter interface provided by Texas Instruments.

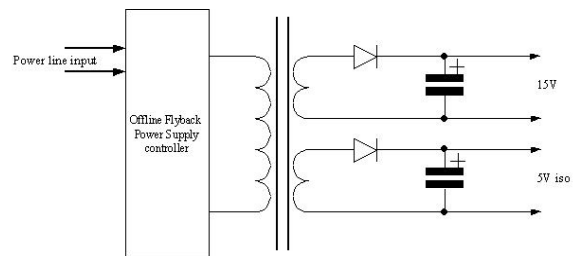
Last but not least is the ADC speed and load characteristic: as the table shows the conversion time is 500ns, in fact the 2406A DSP has a single ADC handling, in time sharing, all 16 inputs, then, using 6 inputs, the total conversion time, which is a fixed delay to wait for before having all data updated, is around 3.0µs.

2. Flyback Power Supply

A flyback power supply for the floating stages is provided in the EDB. As the block schematic on page 2 shows, we have three 15V outputs for the

floating stages, isolated from each other at 1.5kV minimum, and a single 5V and 3.3V output.

The 5V supplies all low voltage electronics and a 3.3V linear regulator is used to feed the DSP and some analog and logic interfaces to it. This 5V and 3.3V are directly referred to the DC bus minus, so that all control circuitry is alternately at one of the input lines potential, isolation is provided at the DSP serial link level, then avoiding all delays due to opto couplers insertion between DSP and control logic. Note that also the required 15V input voltage is referred to the same DC bus minus and directly supplies the low side gate drivers stages, the user should pay some attention on how this supply line is realized in his application. Just for completeness, the following figure gives a possible solution to that that doesn't impact heavily on the user application.



**Examples of power supply for PI-IPM
15V and 5V iso inputs**

Normally a 5V power supply is already present, for displays, electronics and micro processor, the same 5V could be used for the 5V iso supply of opto-couplers and line driver, the 15V could be realized as an added winding in the secondary side of the flyback transformer, the only care that should be taken is in keeping its isolation from the above mentioned 5V at the required level (at least 1.5kV).

To avoid noise problems in the measuring lines due to the commutating electronics during normal functioning of the system, references are kept separated. A 5V linear regulator, directly supplied from the 15V input, is used to provide the reference voltage to the current sensing amplifying and conditioning components while a precise op-amp, configured as a voltage follower,

acts as a buffer of the partition at 3.30V created down the 5V reference. This 3.30V is used also as reference for the DSP A/D converter. It has to be noted that in the schematic we are using the same linear regulator as a starting point for all reference voltages. In fact if the 5V linear regulator drifts in temperature or time, then all references (even the 3.30V being this a simple partitioning) follow in track and still keep the overall chain precision. The trimming is then done only once, in a single point of the measuring chain, that is the conditioning op-amp collecting the current sensing ICs signal as will then be described in the following chapter.

3. Current sensing interfaces, over-current protections and signal conditioning.

This block is the real critical point of the system. Current measuring performances directly impact on motor control performances in a servo application: errors in current evaluation, delay in its measuring chain or poor overall precision of the system, such as scarce references or lower number of significant A/D bits, inevitably results in unwanted trembling and unnatural noise coming from the motor while running at lower speed or at blocked shaft conditions.

In the PI-IPM50P12B004 the current sensing function is done through three sensing resistors dropout measurement, one on each output phase, with the benefit of a lower area and somewhat a lower cost compared to the well-known Hall effect devices. This solution has the added value of having the shunts element embedded in the power module with all Kelvin connections available, avoiding any noise due to long routing of power paths.

As the block schematic on page 2 shows, the voltage across each sensing resistor is applied, through an anti-aliasing 400kHz filter, at the input of a current sense IC and then to a signal conditioning circuit.

Though the block schematic here shows an Op-Amp plus an external passive filter this is simply realized implementing a VCVS cell (i.e. a Constant Gain or Sallen – Key cell) configured

so that the offset and gain is easily trimmed by three on board resistors. The filter implemented is a second order Bessel with 5.5kHz pole frequency, the reason for this is that this type of polynomials are calculated with the aim of having a constant group delay within the pass-band frequencies, thus giving the minimum waveform distortion to the output signal up to almost twice the filter pole. In other words we could also say that the group delay of the signal chain from the sensing resistor up to the ADC input of the DSP is constant from 0 to 5.5kHz.

Signal outputted from the overall chain has a 0 to +3.30V dynamic, with a sensing resistor of 2mohms the input measured current range is +/- 100A then we have a situation as follows:

$$\begin{aligned}
 -100A &= 0.0V \\
 0.00A &= 1.65V \\
 +100A &= 3.30V
 \end{aligned}$$

Summing up our current measurements performances are shown in the following table:

PI-IPM Current sensing chain typical performances

| | Value | Units |
|---------------------------|---------|-------|
| current range | +/- 100 | A |
| Gain and Offset precision | +/- 1.8 | % |
| Bandwidth | 5.5 | kHz |
| latency time | 10 | µs |

The “2406A” DSP has a 10bit ADC, consequently the PI-IPM50P12B004 has a minimum appreciable current step of approximately:

$$LSB = \frac{2*100}{2^{10}} = 0.1953A$$

that is: $1LSB \cong 195mA$

The over current protection is provided also through the current sensing ICs, the related fault signal is activated when a 250mV voltage across

sensing pins is detected, this means an over-current detection level of approximately 25%. The delay of this line is around 3 μ s, fast enough to let the DSP react within the 10 μ s IGBTs short circuit rating, thus providing full device protection for any phase-to-ground and phase-to-phase short circuits. The only failure not covered in this way is the shoot-through, where high current levels cannot be detected from outside the module rather internally between two IGBTs of the same leg. In this case the protection is implemented by means of the fourth sensing element, with the same resistive value of the other shunts present in the power module, inserted in series to the DC bus minus. The related dropout voltage is then filtered by a 15kHz passive filter to avoid false fault detections due to unwanted induced voltage spikes and finally applied to an operational amplifier configured as a comparator. All data referred to the OC protection are listed on page 9 of this datasheet.

4. Gate Drivers

Devices used to perform this task are the well-known IR2213, capable of 2A sink and 2A source maximum gate driving current, in a SO16W package; on page 2 is shown also the block schematic of the gate driving section of the module.

The IGBTs used in the PI-IPM (genV NPT 1200V - 50A from IR) do not need any negative gate drive voltage for their complete turn off, this simplifies the flyback power supply design avoiding the need of center tapped transformer outputs or the use of zener diodes to create the central common reference for the gate drivers floating ground. Though the IR2213 do have +/- 2A of gate current capability, in the PI-IPM50P12B004 we use different gate resistor values for turn on and turn off as follows:

$$\text{turn - on} = 330\text{ohm}$$

$$\text{turn - off} = 7.60\text{ohm}$$

Commonly realized through a diode-resistor series in parallel with a single resistor used in

turn on only. Observed rise and fall times are around 250ns – 300ns depending on the output current level, this values are considered as pretty adequate for a 25A application at 16kHz symmetric PWM carrier, space vector modulation.

These gate drivers do provide levels shifting without any galvanic isolation, that is no optocouplers are built inside. This turns out to be a major benefit in this stage where the usual 1 μ s delay of optos impacts on the system control as a systematic and fastidious delay.

5. DC bus and Input voltage feedback

The purpose of this block is to continuously check the voltage of the two supply lines of the system: Vin and DC bus. Vin is the only external power supply needed for all electronics in the EDB. The internal flyback regulator has its own under-voltage lockout to prevent all electronics from start working when an insufficient supply voltage is present; minimum recommended supply voltage is 12V. Low side gate drivers are directly fed from the Vin line and there is no further control to this voltage than their own under-voltage lockout. This is typically set at 8.5V and this level could be not sufficient to properly drive the IGBT gates, then it is advisable to check with the DSP the input voltage and impose that the system could start switching only when the Vin voltage is between 10V and 18V thus providing also an over-voltage control.

The DC bus voltage is also important for the system functioning and needs to be continuously kept under control. A resistor divider provides a partition coefficient of 2.44mV/V and a maximum mapped voltage of around 1100V

As the block schematic shows, it has to be taken into account that, to avoid false detections due to voltage spikes inevitably present on the partitioned voltage, a 1kHz passive filter has been inserted between the divider and the voltage follower buffer whose output is connected to one of the ADC inputs.

Fig. 1 – Maximum DC collector Current vs. case temperature

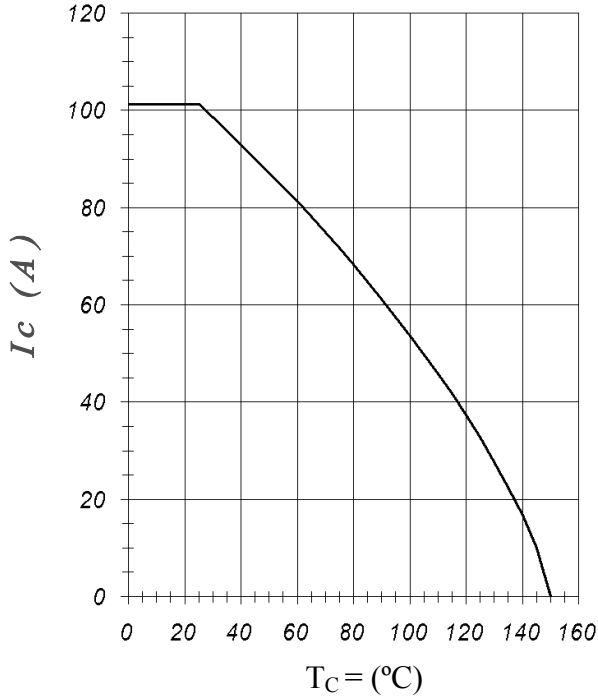


Fig. 2 – Power Dissipation vs. Case Temperature

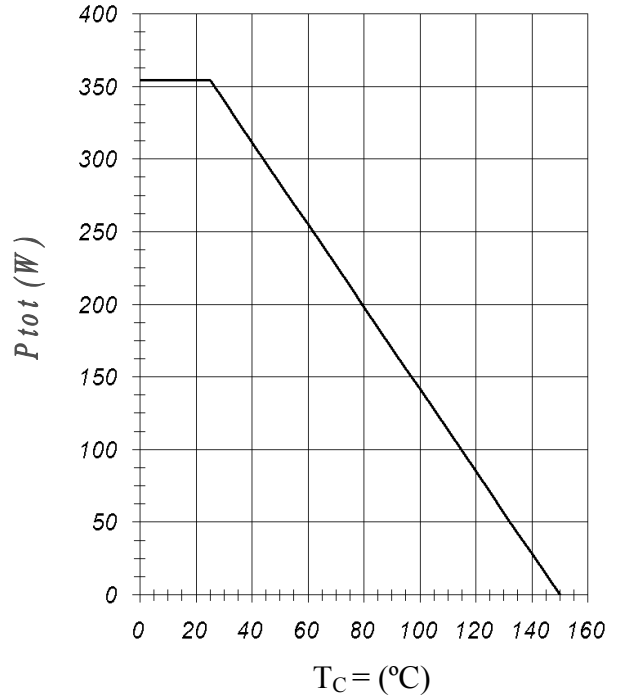


Fig. 3 – Forward SOA
 $T_C = 25^\circ\text{C}; T_j \leq 150^\circ\text{C}$

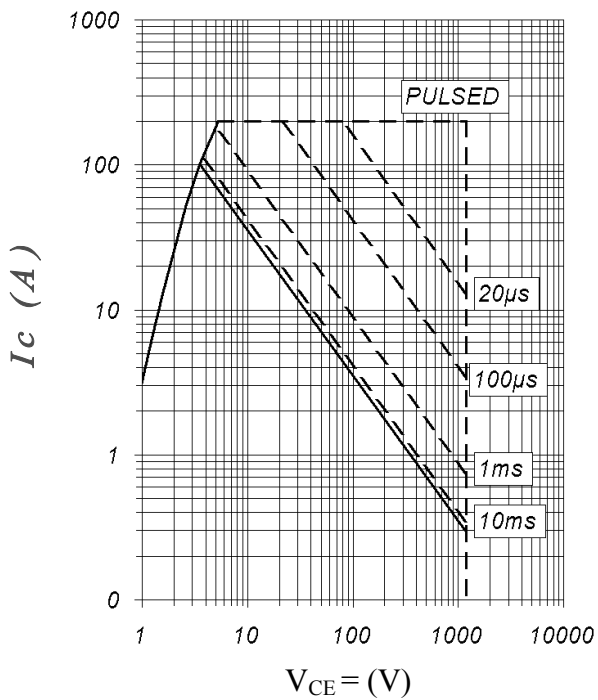


Fig. 4 – Reverse Bias SOA
 $T_j = 150^\circ\text{C}, V_{GE} = 15\text{V}$

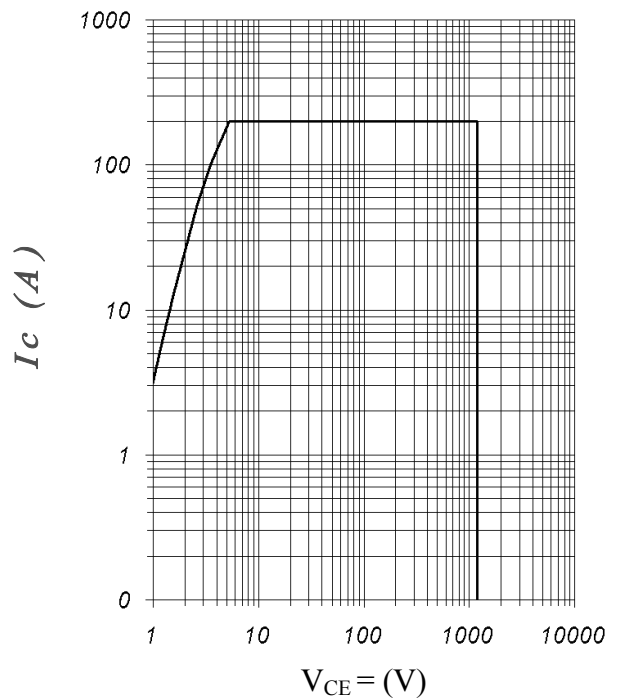


Fig. 5 – Typical IGBT Output Characteristics
 $T_j = -40^{\circ}\text{C}$; $t_p = 500\mu\text{s}$

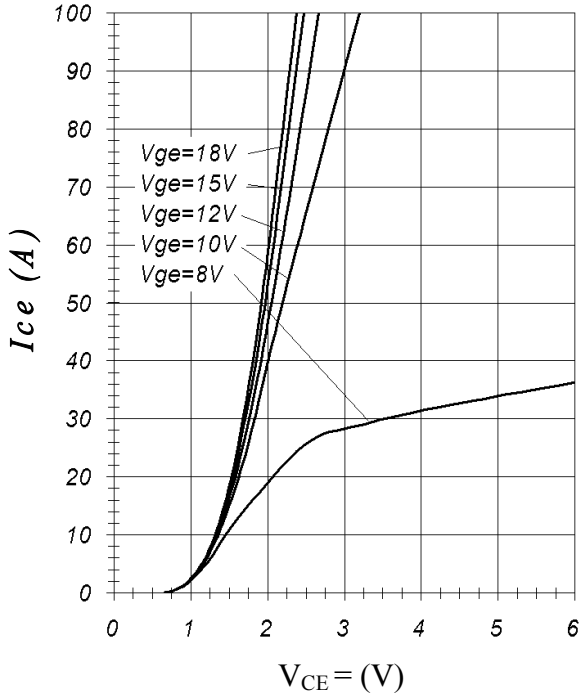


Fig. 6 – Typical IGBT Output characteristics
 $T_j = 25^{\circ}\text{C}$; $t_p = 500\mu\text{s}$

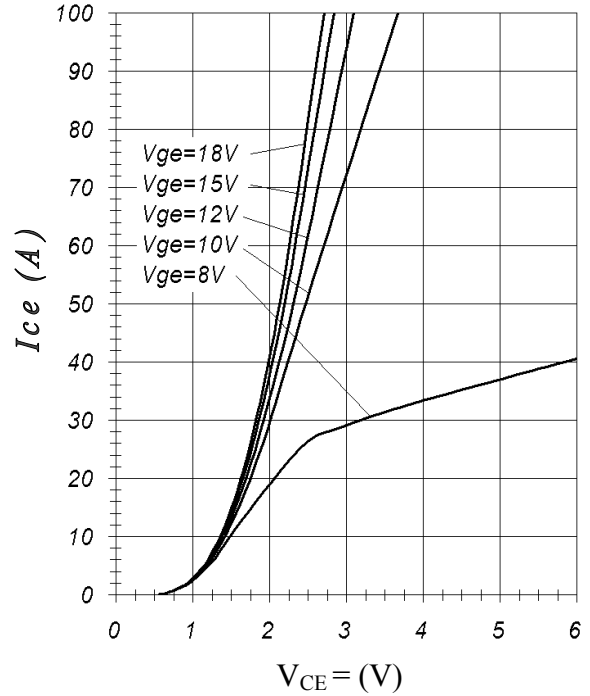


Fig. 7 – Typical IGBT Output Characteristics
 $T_j = 125^{\circ}\text{C}$; $t_p = 500\mu\text{s}$

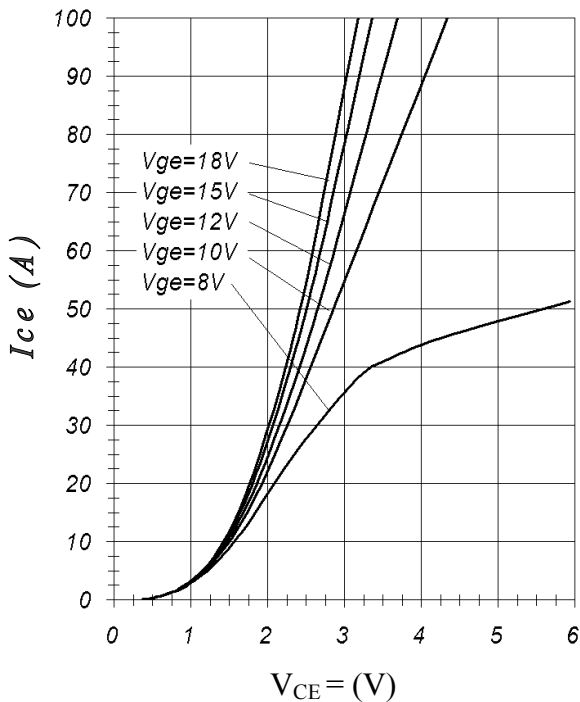


Fig. 8 – Typical Diode Forward Characteristics
 $t_p = 500\mu\text{s}$

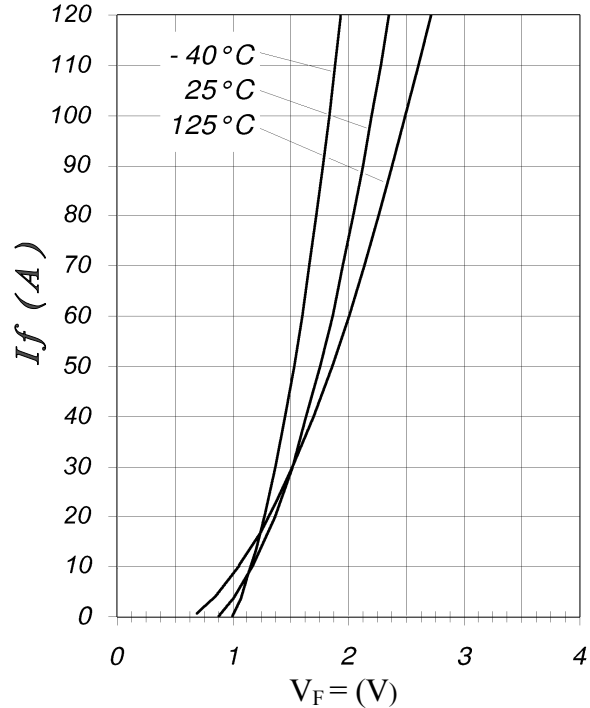


Fig. 9 – Typical V_{CE} vs. V_{GE}
 $T_j = -40^\circ\text{C}$

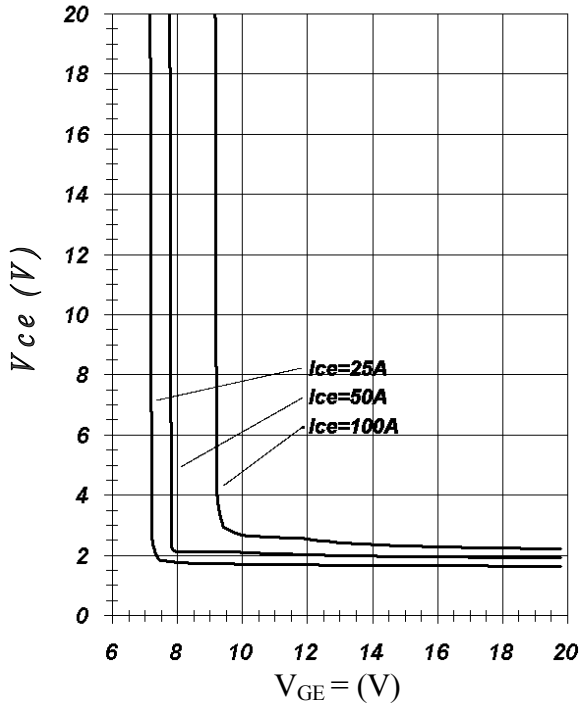


Fig. 10 – Typical V_{CE} vs. V_{GE}
 $T_j = 25^\circ\text{C}$

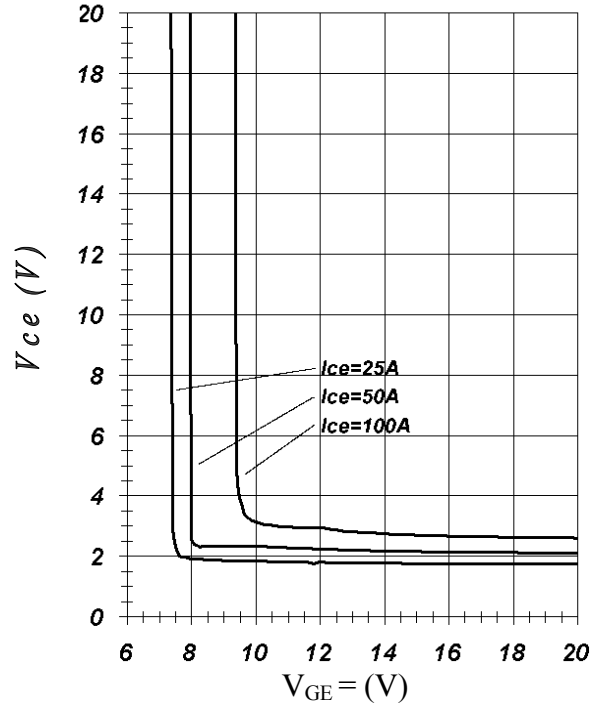


Fig. 11 – Typical V_{CE} vs. V_{GE}
 $T_j = 125^\circ\text{C}$

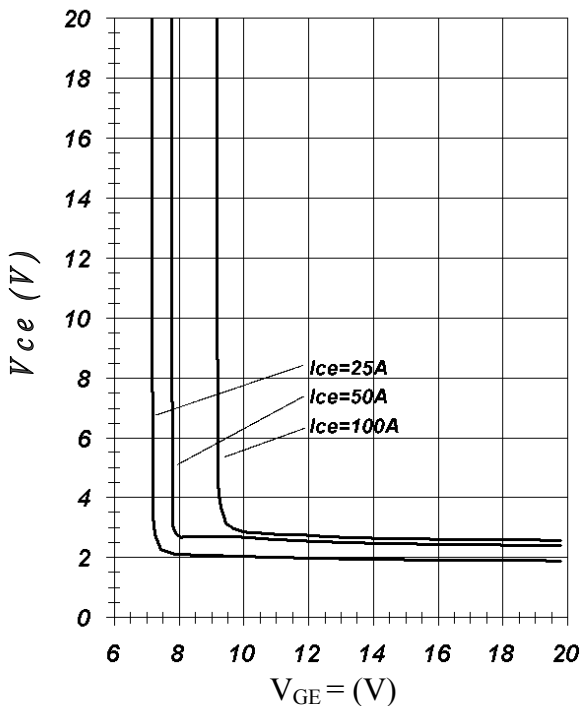


Fig. 12 – Typical Transfer Characteristics
 $V_{CE} = 20\text{V}$; $t_p = 20\mu\text{s}$

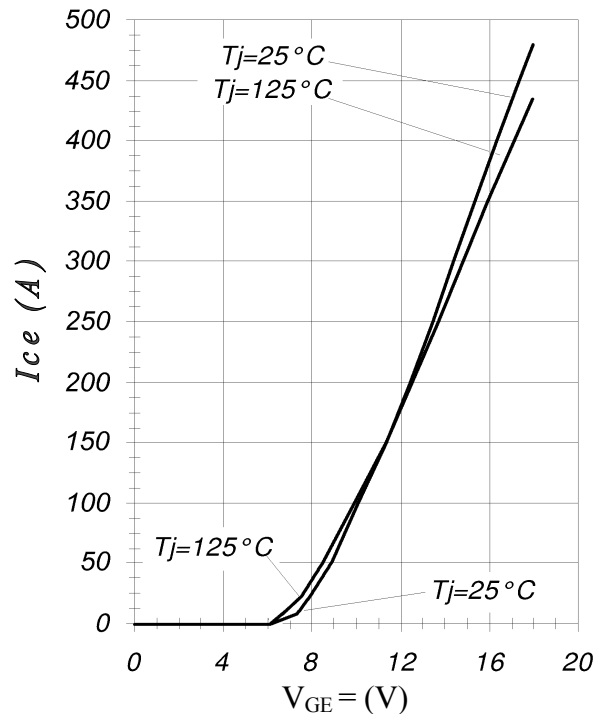


Fig. 13 – Typical Energy Loss vs. I_C
 $T_j = 125^\circ\text{C}$; $L = 250\mu\text{H}$; $V_{CE} = 600\text{V}$;
 $R_g = 10\Omega$; $V_{GE} = 15\text{V}$

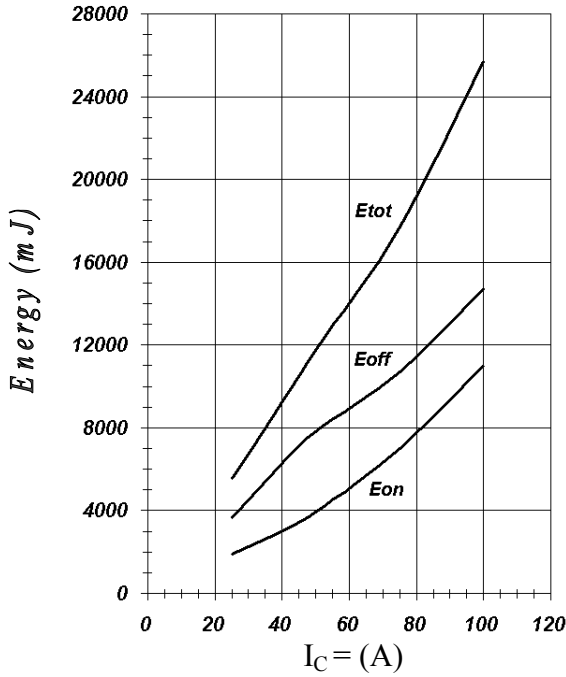


Fig. 14 – Typical Switching Time vs. I_C
 $T_j = 125^\circ\text{C}$; $L = 250\mu\text{H}$; $V_{CE} = 600\text{V}$;
 $R_g = 10\Omega$; $V_{GE} = 15\text{V}$

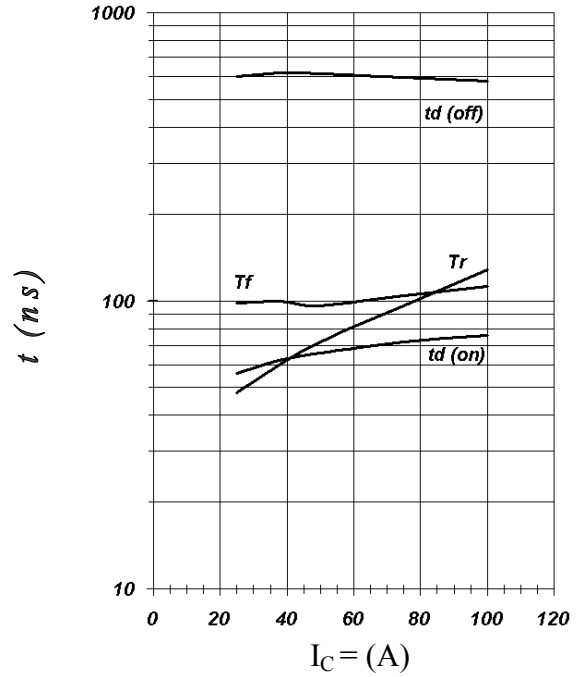


Fig. 15 – Typical Energy Loss vs. R_g
 $T_j = 125^\circ\text{C}$; $L = 250\mu\text{H}$; $V_{CE} = 600\text{V}$;
 $I_{CE} = 50\text{A}$; $V_{GE} = 15\text{V}$

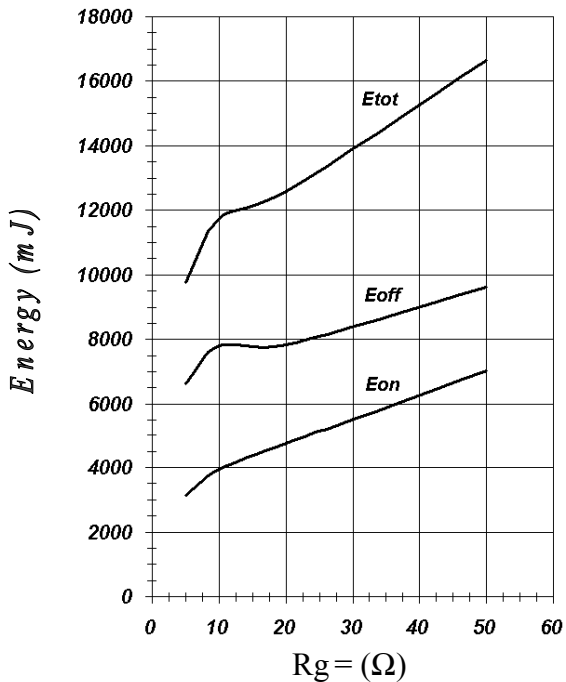


Fig. 16 – Typical Switching Time vs. R_g
 $T_j = 125^\circ\text{C}$; $L = 250\mu\text{H}$; $V_{CE} = 600\text{V}$;
 $I_{CE} = 50\text{A}$; $V_{GE} = 15\text{V}$

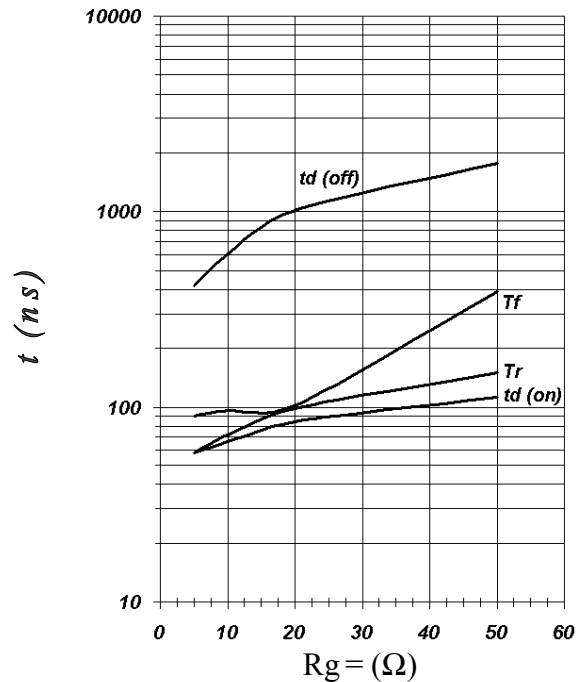


Fig. 17 – Typical Diode I_{RR} vs. I_F
 $T_j = 125^\circ\text{C}$

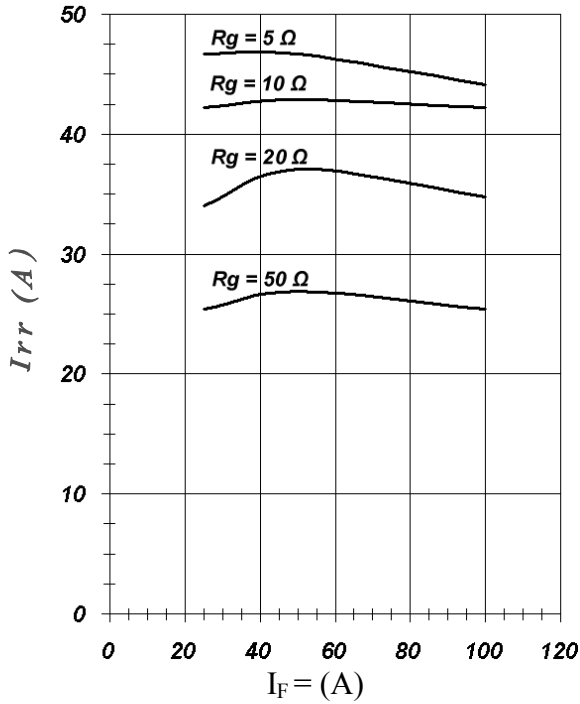


Fig. 18 – Typical Diode I_{RR} vs. R_g
 $I_F = 50\text{A}; T_j = 125^\circ\text{C}$

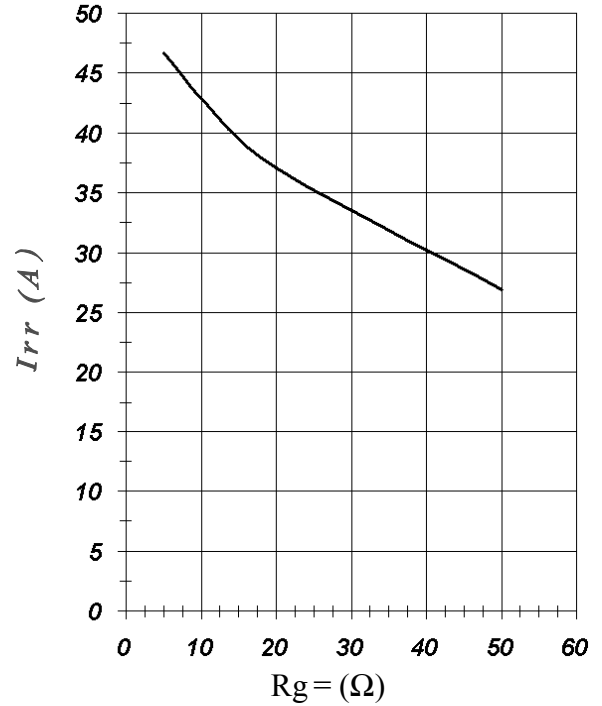


Fig. 19 – Typical Diode I_{RR} vs. dI_F/dt
 $V_{DC} = 600\text{V}; V_{GE} = 15\text{V}; I_F = 50\text{A}; T_j = 125^\circ\text{C}$

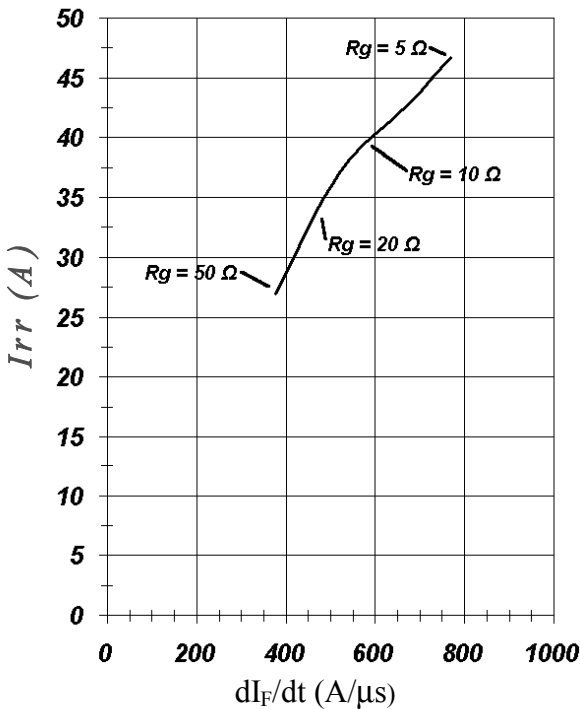


Fig. 20 – Typical Diode Q_{RR}
 $V_{DC} = 600\text{V}; V_{GE} = 15\text{V}; T_j = 125^\circ\text{C}$

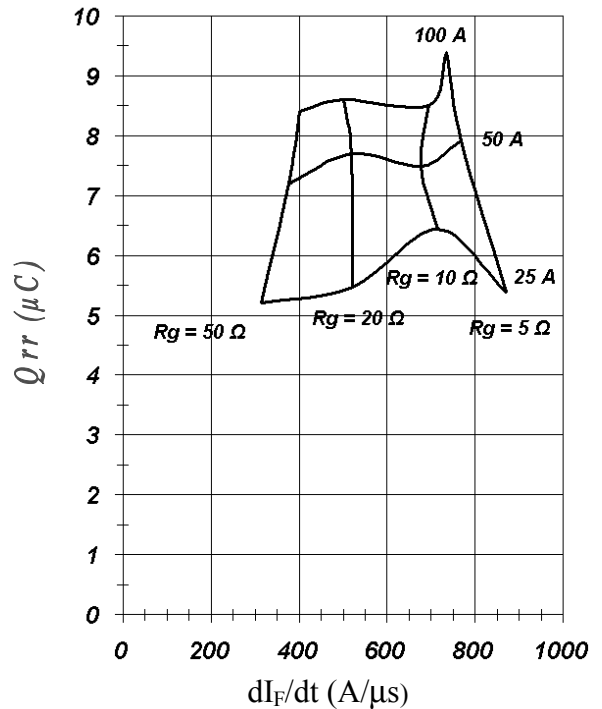


Fig. 21 – Typical Diode E_{REC} vs. I_F
 $T_j = 125^\circ\text{C}$

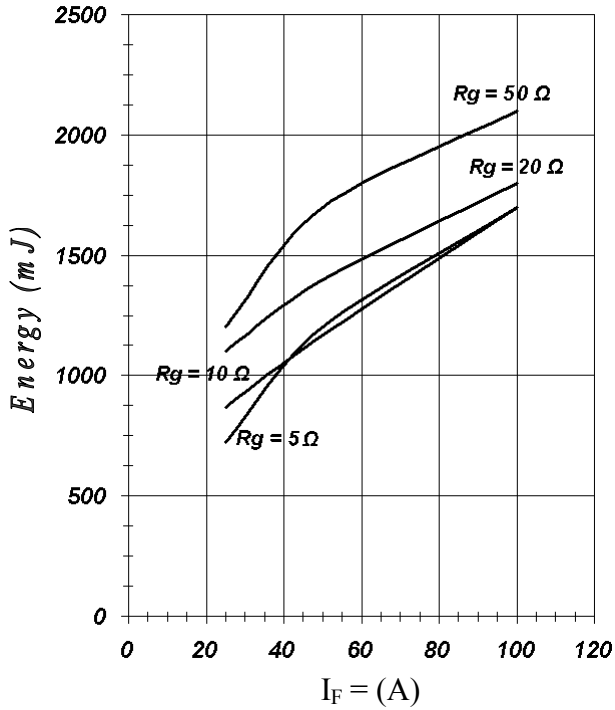


Fig. 22 – Typical Capacitance vs. V_{CE}
 $V_{GE} = 0\text{V}$; $f = 1\text{MHz}$

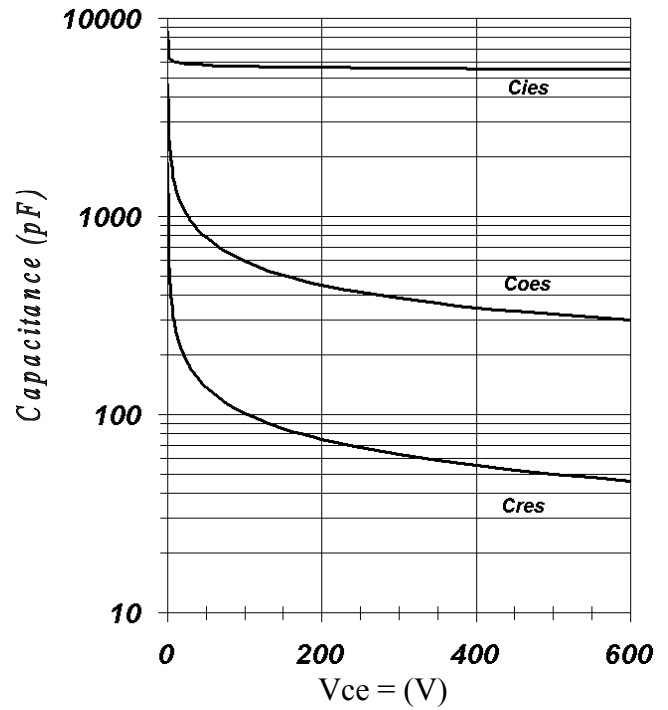


Fig. 23 – Typical Gate Charge vs. V_{GE}
 $I_C = 50\text{A}$; $L = 600\ \mu\text{H}$; $V_{CC} = 600\text{V}$

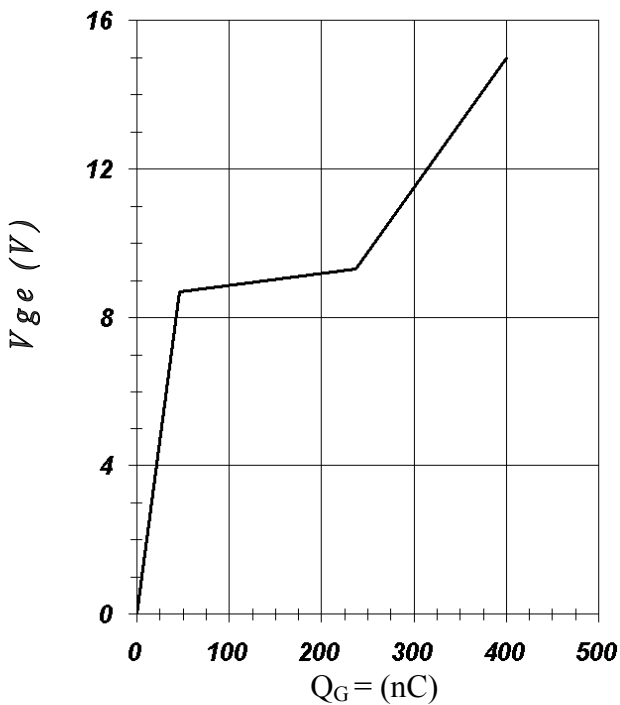


Fig. 24 – Normalized Transient Thermal Impedance, Junction-to-copper plate (IGBTs)

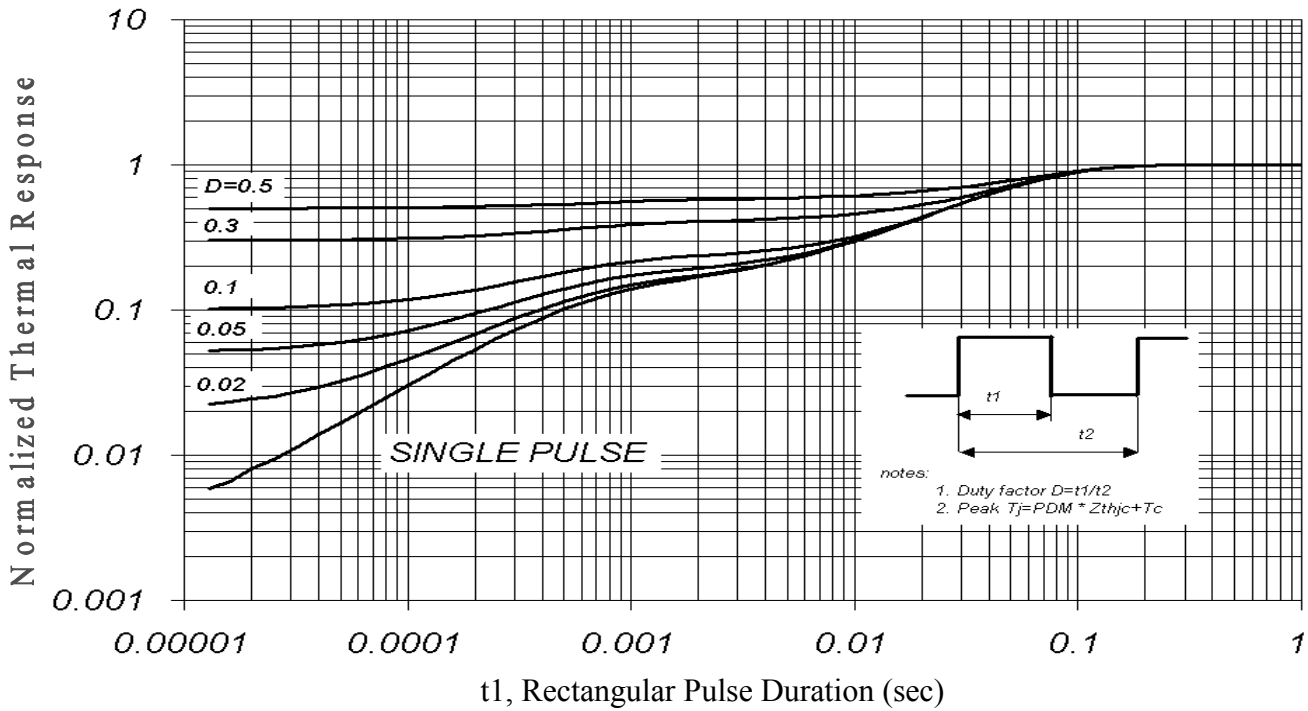


Fig. 25 – Normalized Transient Impedance, Junction-to-copper plate (FRED diodes)

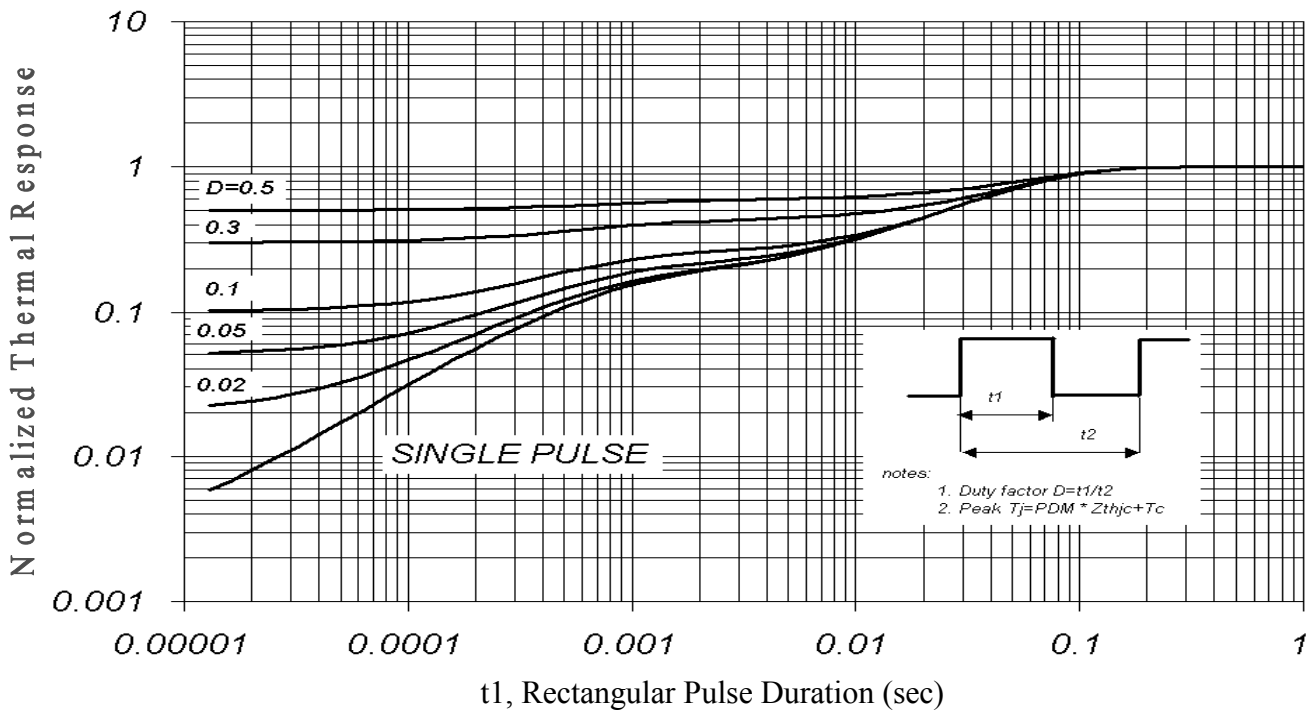


Fig. CT.1 - Gate Charge Circuit (turn-off)

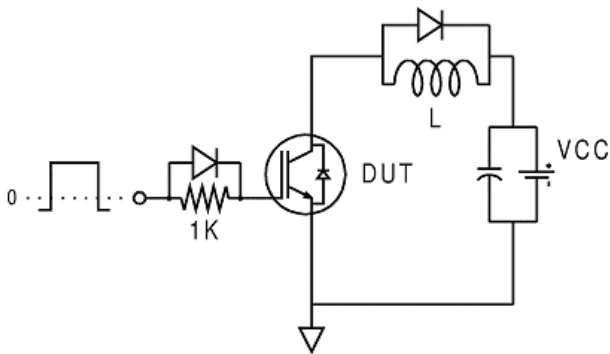


Fig. CT.2 - RBSOA Circuit

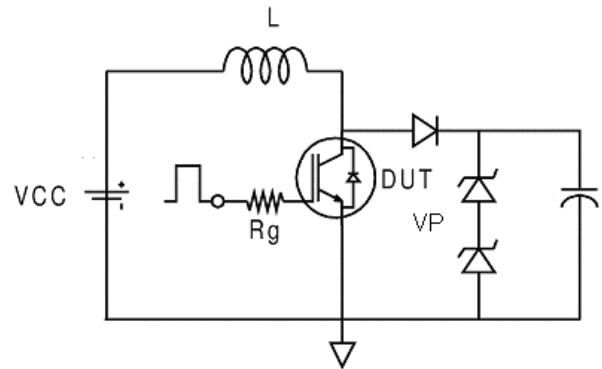


Fig. CT.3 - S.C. SOA Circuit

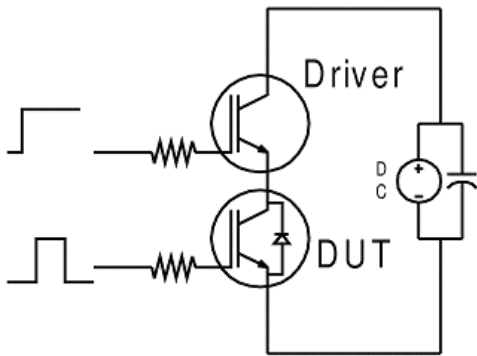


Fig. CT.4 - Switching Loss Circuit

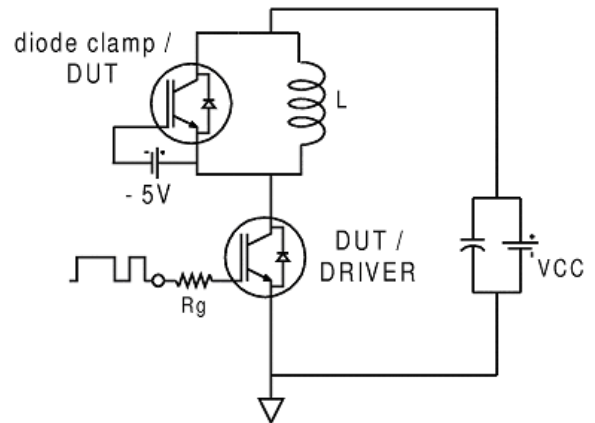


Fig. CT.5 - Resistive Load Circuit

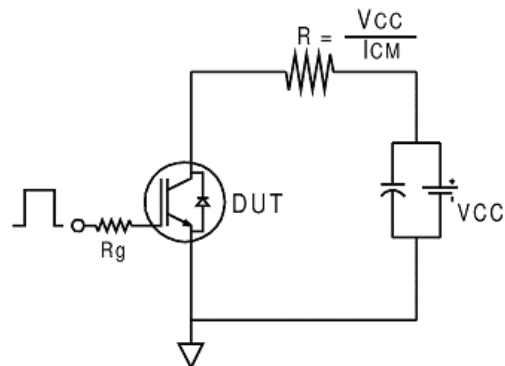


Fig. WF.1 - Typ. Turn-off Loss Waveform
@ $T_j=125^\circ\text{C}$ using Fig. CT.4

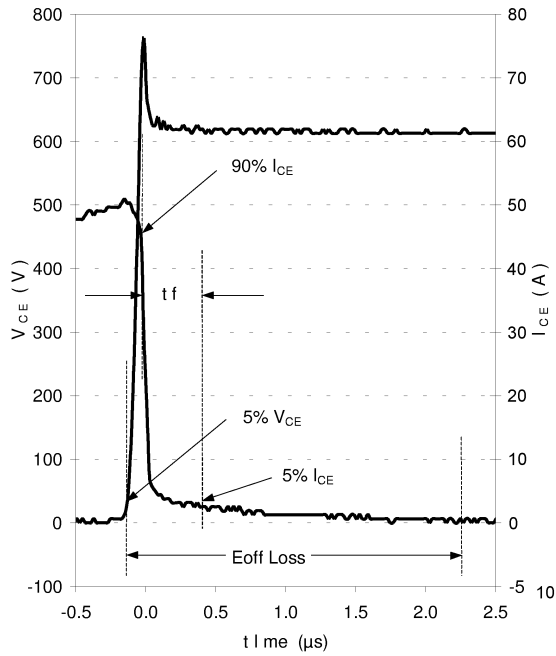


Fig. WF.2 - Typ. Turn-on Loss Waveform
@ $T_j=125^\circ\text{C}$ using Fig. CT.4

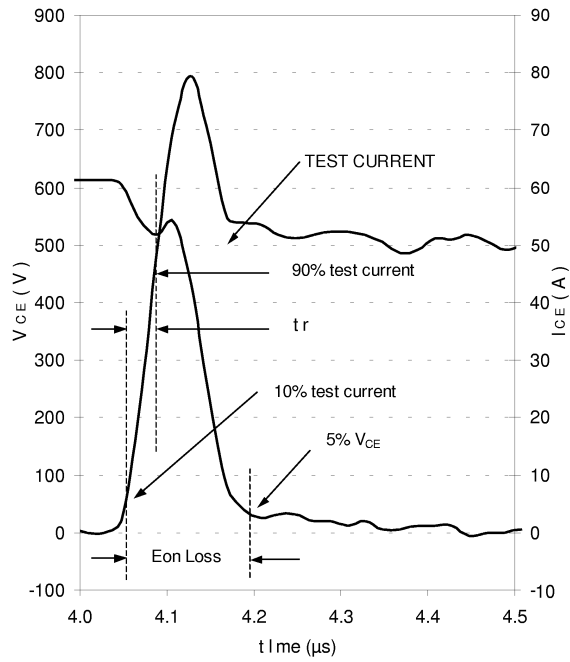


Fig. WF.3 - Typ. Diode Recovery Waveform
@ $T_j=125^\circ\text{C}$ using Fig. CT.4

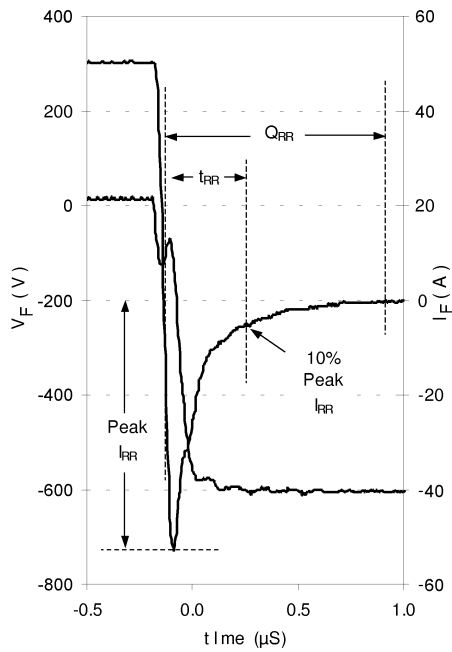


Fig. WF.4 - Typ. S.C. Waveform
@ $T_C=150^\circ\text{C}$ using Fig. CT.3

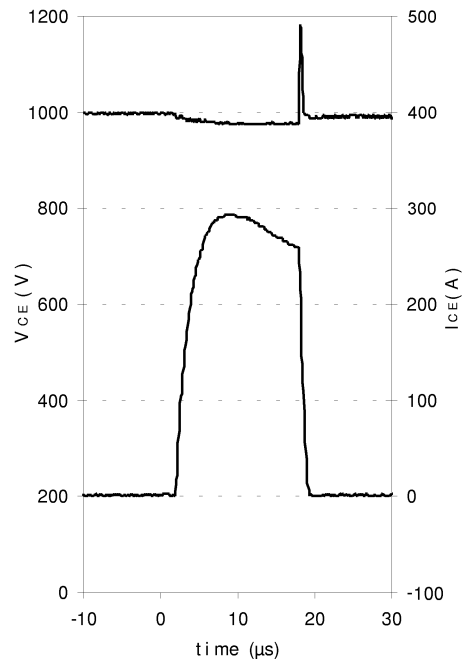


Fig. PD1 – Total Dissipated Power vs. f_{sw}
 $I_{out_{RMS}} = 7A, V_{DC} = 530V, T_C = 55^\circ C$

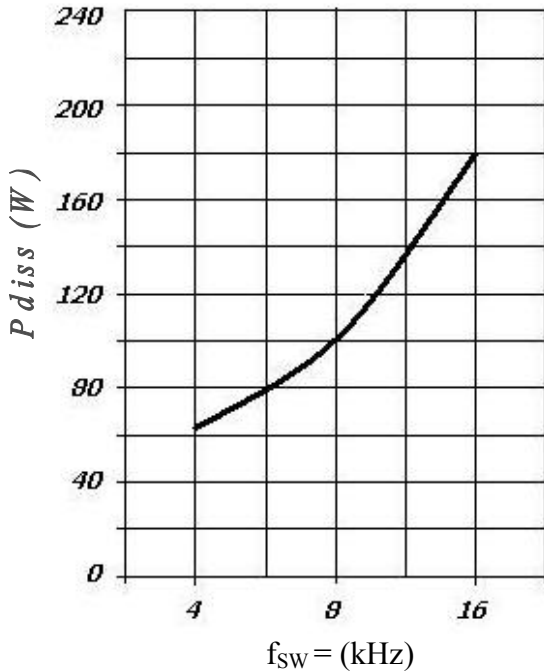


Fig. PD2 – Total Dissipated Power vs. f_{sw}
 $I_{out_{RMS}} = 10A, V_{DC} = 530V, T_C = 55^\circ C$

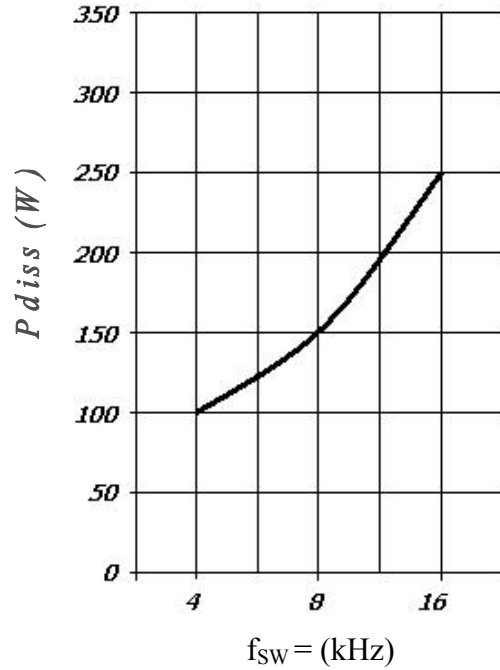


Fig. PD3 – Total Dissipated Power vs. f_{sw}
 $I_{out_{RMS}} = 20A, V_{DC} = 530V, T_C = 40^\circ C$

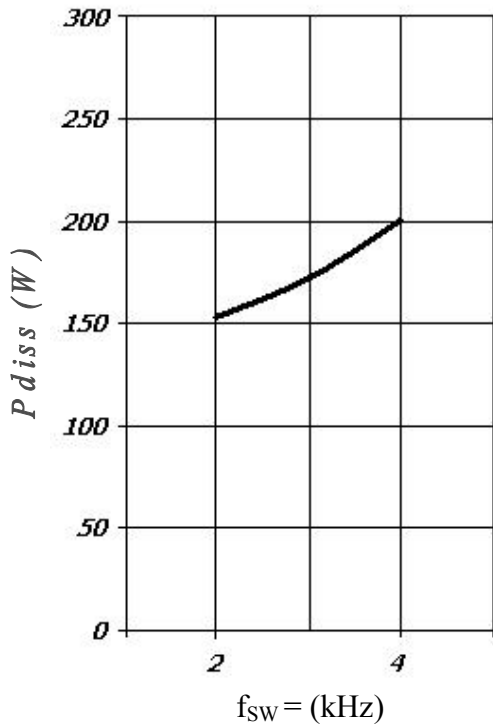
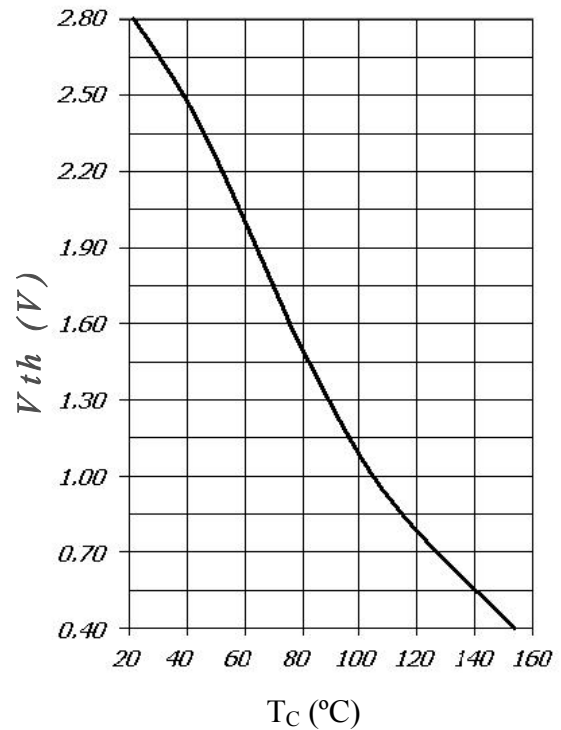
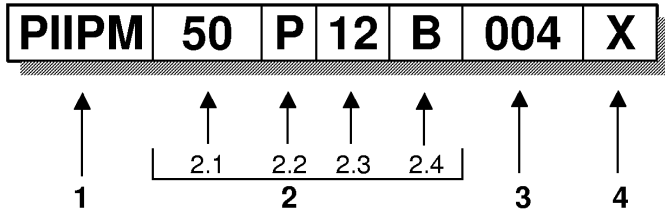


Fig. TF1 – Thermal Sensor Voltage Feedback vs. Base-plate Temperature



PIIPM family part number identification



1- Device type (**Programmable Isolated Intelligent Power Module**)

2- Power package code

| | | | | | | | | | | | | | | |
|---|--|-----------------|---------------------|--|-------------------|-----------------------|----------------------|-----------|------------|----------------------|--------------|----------------------|---------------------------------|----------------|
| <p>2.1- Current rating Code [A]</p> <p>2.2- Sensing Resistors configuration</p> <p>2.3- Voltage rating Code [V/100]</p> <p>2.4- Power Module configuration code</p> | <table border="1" style="border-collapse: collapse; width: 100%;"> <tr> <td style="padding: 2px;">P = on 3 phases</td> </tr> <tr> <td style="padding: 2px;">Q = on 2 phases (*)</td> </tr> <tr> <td style="padding: 2px;">R = on 1 phase (only for Matrix config.) (*)</td> </tr> <tr> <td style="padding: 2px;">E = on 3 emitters</td> </tr> <tr> <td style="padding: 2px;">F = on 2 emitters (*)</td> </tr> <tr> <td style="padding: 2px;">G = on 1 emitter (*)</td> </tr> </table> <table border="0" style="width: 100%;"> <tr> <td style="padding-right: 10px;">06 = 600V</td> </tr> <tr> <td>12 = 1200V</td> </tr> </table> <table border="1" style="border-collapse: collapse; width: 100%;"> <tr> <td style="padding: 2px;">A = Bridge brake (*)</td> </tr> <tr> <td style="padding: 2px;">B = Inverter</td> </tr> <tr> <td style="padding: 2px;">C = Inverter + brake</td> </tr> <tr> <td style="padding: 2px;">D = BBI (Bridge Brake Inverter)</td> </tr> <tr> <td style="padding: 2px;">M = Matrix (*)</td> </tr> </table> | P = on 3 phases | Q = on 2 phases (*) | R = on 1 phase (only for Matrix config.) (*) | E = on 3 emitters | F = on 2 emitters (*) | G = on 1 emitter (*) | 06 = 600V | 12 = 1200V | A = Bridge brake (*) | B = Inverter | C = Inverter + brake | D = BBI (Bridge Brake Inverter) | M = Matrix (*) |
| P = on 3 phases | | | | | | | | | | | | | | |
| Q = on 2 phases (*) | | | | | | | | | | | | | | |
| R = on 1 phase (only for Matrix config.) (*) | | | | | | | | | | | | | | |
| E = on 3 emitters | | | | | | | | | | | | | | |
| F = on 2 emitters (*) | | | | | | | | | | | | | | |
| G = on 1 emitter (*) | | | | | | | | | | | | | | |
| 06 = 600V | | | | | | | | | | | | | | |
| 12 = 1200V | | | | | | | | | | | | | | |
| A = Bridge brake (*) | | | | | | | | | | | | | | |
| B = Inverter | | | | | | | | | | | | | | |
| C = Inverter + brake | | | | | | | | | | | | | | |
| D = BBI (Bridge Brake Inverter) | | | | | | | | | | | | | | |
| M = Matrix (*) | | | | | | | | | | | | | | |

3- EDB configuration code

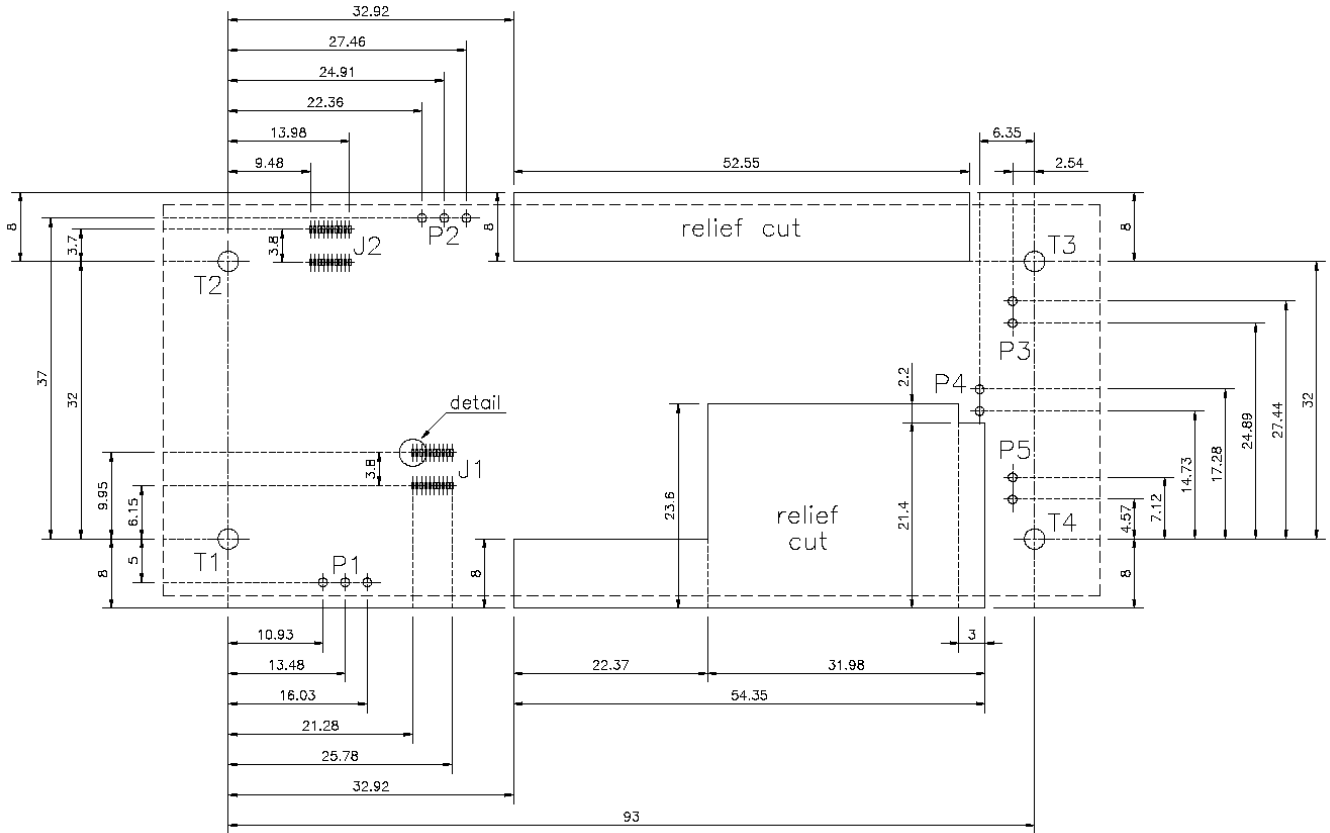
See detailed Block Diagram

4- Status code

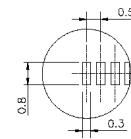
| |
|--|
| X = Sample (product with pre-qualification approval) |
| Mating connectors included in the box |
| blank = Fully qualified product |

note: *= contact factory for availability

Top board suggested footprint
(top view)



ENLARGED VIEW
OF DETAIL

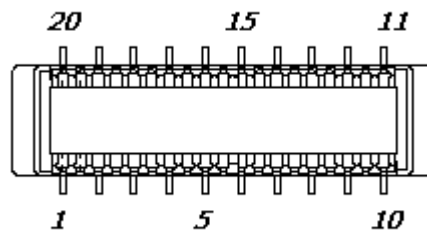


NOTES

- all dimension are in millimeter
- T1/T2/T3/T4 : diameter=3
- P1/P2/P3/P4/P5 : diameter=1
- : PIIPM outline
- : relief cut minimum outline

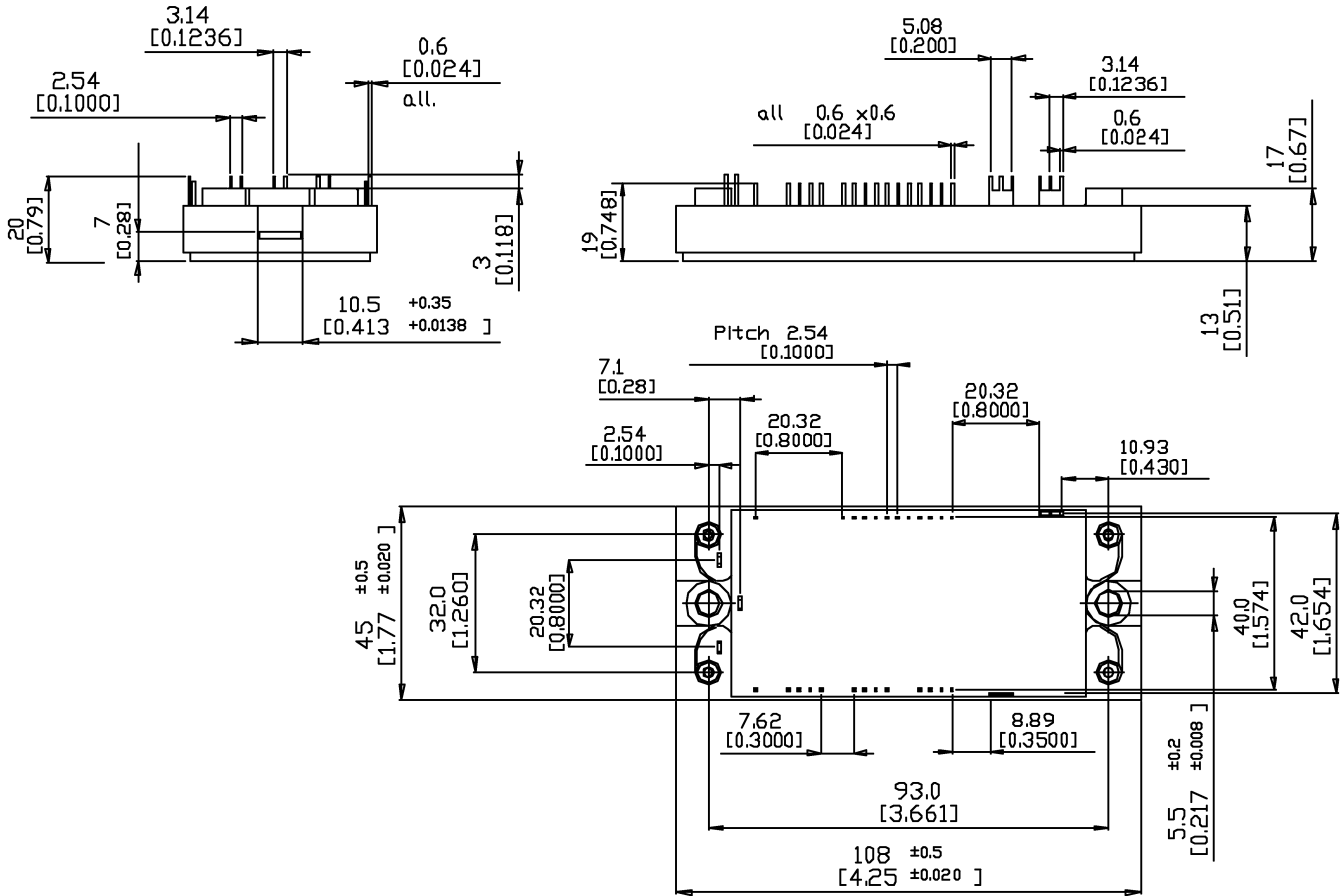
RS422 and JTAG Connectors top view

These connectors do not have any orientation tag; please check their Pin 1 position on Power Module Frame Pins Mapping before inserting mate part.



Molex 53916-0204
mates with 54167-0208 or 52991-0208

PIIPM50P12B004 case outline and dimensions



Data and specifications subject to change without notice
This product has been designed and qualified for Industrial Level.
Qualification Standards can be found on IR's Web Site.