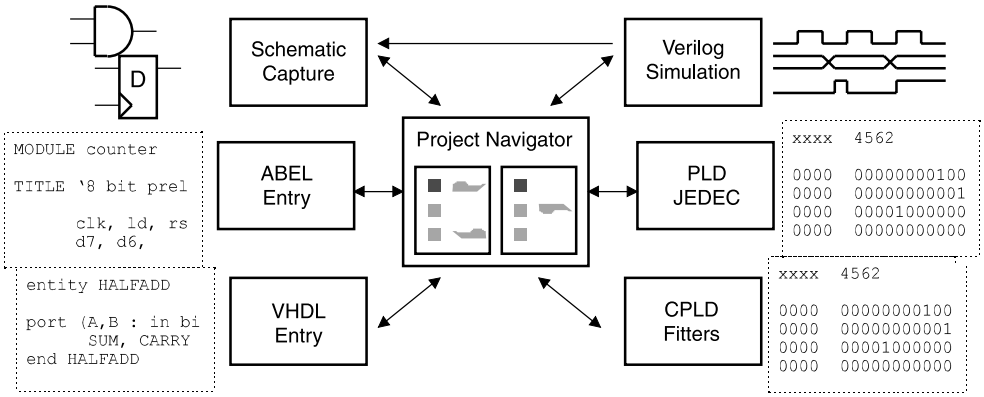
Features

- **Comprehensive CPLD/PLD Design Environment**
- **User-friendly Microsoft Windows™ Interface (Win 95, Win 98, Win NT)**
- **Powerful Project Navigator**
  - **Utilizes Intelligent Device Fitters for Automatic Logic Synthesis and Device Resource Assignment**
  - **Allows Design Specification with Schematic Entry or the ABEL-HDL**
- **Integrated ABEL Text Design Entry and Synthesis**
  - **Friendly Windows-based User Interface is Easy to Learn and Use**
  - **ABEL-HDL Design Entry Provides Detailed Support for Programmable Logic Devices**
  - **Full Hierarchical Support Makes Large Designs Easier to Manage; Large All-behavioral Designs can be Created without Drawing any Schematics**
- **Integrated Verilog™ Timing Simulator (Optional)**
  - **Fast, Functional Simulation is Performed Directly from the Schematic or Behavioral Source File, Providing Quick Feedback on Logic Errors as the Design is Entered**
  - **Full Timing Simulation with Delay-annotated Models Provides Comprehensive Support for Timing Problems in Routed Devices**
  - **Logic-analyzer-like Waveform Viewer Provides Flexible Results Viewing, and Updates Every Time you Single-step the Simulator**
  - **Cross-probing Capabilities between the Schematic and Waveform Viewer Tie Simulation Results Directly Back to the Source Design, Making Results Easier to Interpret**
  - **Interactive Debugging Provides Force/Preset/Monitor Access to all of the Design's Signals, for Fast and Easy, On-the-fly Changes**
  - **Industry-standard Verilog HDL Simulation Language Ensures Timely Support for New Device Architectures**
- **IEEE 1076 VHDL Synthesis and Simulation (Optional)**

Description

Atmel-Synario is an integrated CPLD/PLD design tool. It supports all proprietary, and JEDEC standard devices offered by Atmel. The usual CAE tool capability is combined with CPLD specific functionality. A tightly integrated Windows environment gives the user a friendly, and powerful interface. The system combines schematic and behavioral entry methods. Functional and timing simulation are also supported. An intelligent design manager, supervises file manipulation and controls the design flow. This function allows a user to move quickly from one design to another and evaluate different implementations for an optimal solution.



Atmel-Synario CPLD/PLD Design Software

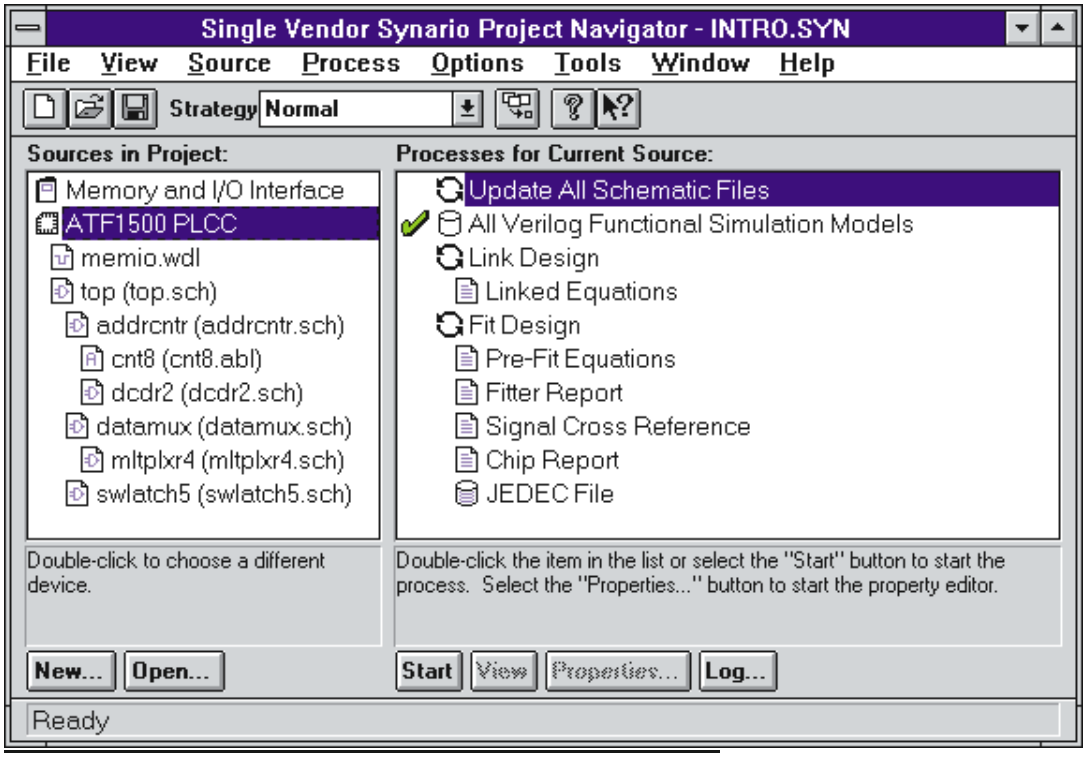
ATDS1100PC
ATDS1120PC
ATDS1130PC
ATDS1140PC

Rev. 0714C–09/99

Project Navigator

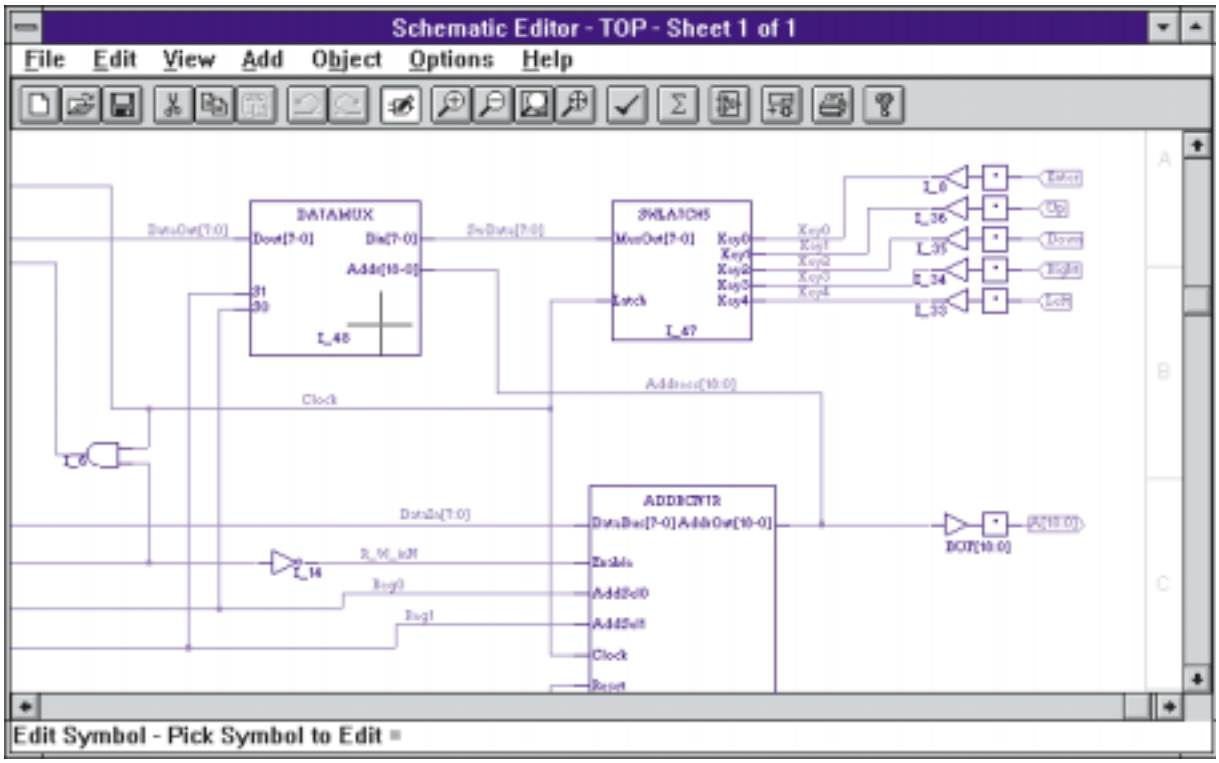
Atmel-Synario *Project Navigator* is the core of the system. It is a powerful and simple design flow controller. Built-in intelligence, gives file and run option knowledge for each device. Select the ATF1500 and all the steps required to design, simulate, compile and fit will appear. Change to ATF22V10 and the steps change accordingly. You may even choose to design without a particular architecture and pick it later in the design process (Virtual or Generic Device).

Project Navigator also tracks and displays status of the design process. Each design step is clearly delineated, and can be performed independently of the complete flow. Or, you can perform a complete compilation in a single step. Project Navigator will netlist all the schematics in your design, and compile, optimize, and synthesize all the behavioral modules. If only a portion of the design changes (a module or a single schematic), you don't have to netlist and compile the whole design. Project Navigator knows everything else is current by keeping track of all the files. Finally, processing options are intelligently defaulted (but can also be customized). Detailed device-specific help is available for each step.



ECS – Schematic Entry

Atmel-Synario schematic tool is a MS Windows-based environment. Schematic Capture in Navigator mode gives an online view of the connectivity database. Push into a lower-level schematic and upper level signal names are visible below. Highlight a net and you can follow it up and down the hierarchy. Run a design-rule check, and errors appear in a box; click on an error, and the schematic jumps to the page and location of the error. Whenever a new device is targeted, libraries are changed automatically.



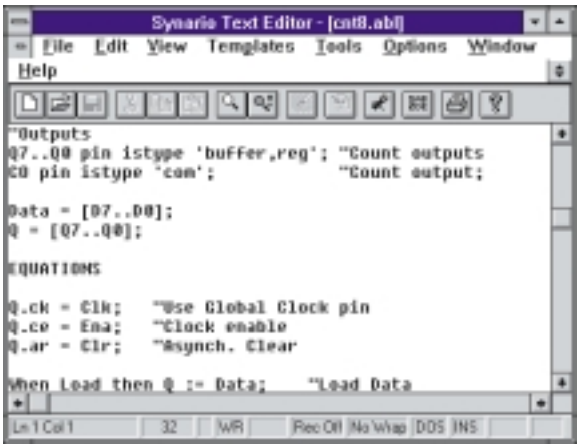
Device-independent Design

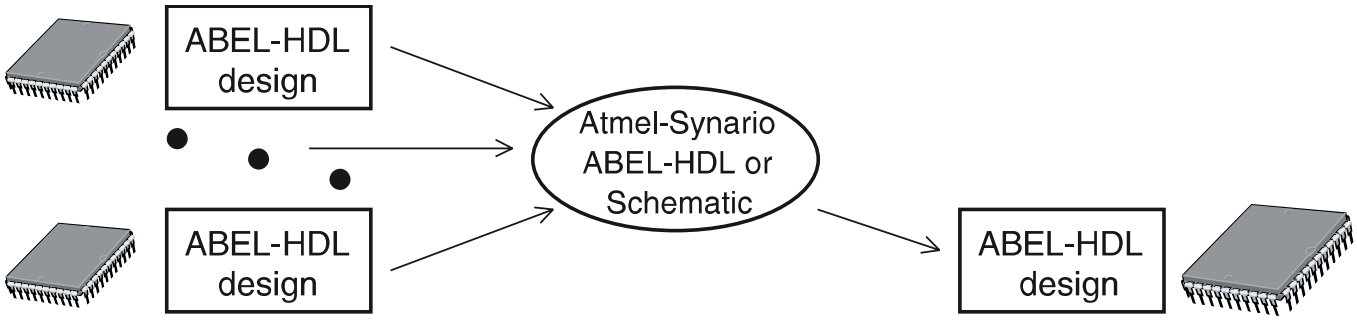
Device-independent design is a useful design technique. It frees the designer from architectural knowledge, and allows the best device fit to each application. Until now each architecture required a different library, with different symbols. Atmel-Synario solves this problem with its powerful and unique device-independent library. Using the standard building blocks the device-independent library provides, you can draw entire schematics that can be targeted to any device. The symbols have all the “smarts” to map efficiently and simulate correctly in any target device. You can build device-independent soft macros the same way. If you desire architecture specific functions, simply use the Atmel-Specific library for more efficient utilization. Now going from a 5 ns ATF16V8C to a high-density ATF1508 CPLD is only a compilation away.

ABEL Integration into Atmel-Synario: Behavioral Entry and Simulation

ABEL is one of the tools integrated into Atmel-Synario. Therefore, importing existing PLD designs into a larger designs is straight forward. Adding new logic, and reimplementing into a larger CPLD is simple. Experienced ABEL users can get started using Synario ABEL tool, then gradually use more of the extended Atmel-Synario capability.

Atmel-Synario Behavioral Entry has hierarchical capability. Large, all-behavioral designs can be entered without drawing any schematics. Device-specific logic synthesis allows easy design migration to all supported devices.





Fastest way to migrate from simple PLDs to CPLDs:

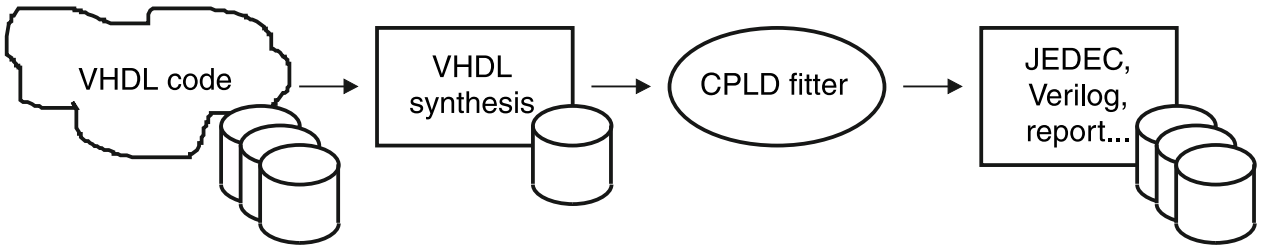
- Use existing legacy designs in new designs
- Convert from one architecture to another
- Upgrade designs to new technologies

ABEL – Functional Simulation

ABEL has built-in functional simulation capability. This allows for early design cycle verification (before fitting). This also enables quick design on small projects. Full Synario functionality with legacy ABEL designs is also an advantage of ABEL functional simulation.

VHDL – Synthesis Option

Atmel-Synario gives you full VHDL support. IEEE-1076 compliant synthesis is tightly integrated into the environment, which allows quick implementation into all supported devices. Atmel-Synario VHDL provides a full package of IEEE-1076 analysis, synthesis, and source-level simulation capability. Even mixing VHDL entry with ABEL and schematics is a simple task. A full capability VHDL design environment can be created with an additional functional simulator.

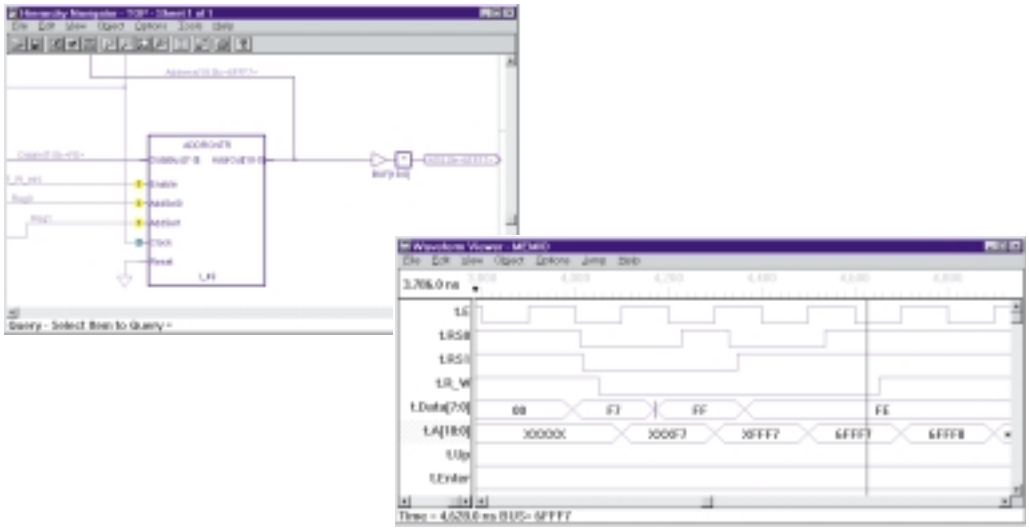


Verilog – Functional and Timing Simulation Option

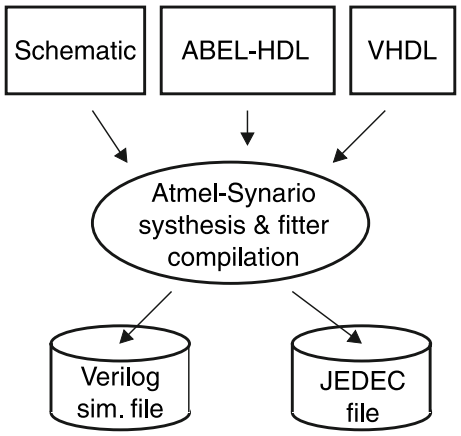
Verilog simulation is another of the Atmel-Synario tools. This standard simulation package gives functional and full timing simulation. The simulation package is fully compatible with Open-Verilog, which allows construction of powerful test benches and result analysis and summary functions. Atmel-Synario Simulation creates simulation models directly from Synario's source files. This, coupled with an extremely fast simulator, quickly tells you whether your logic is correct while you're entering it – even before the synthesis and fitting steps. After fitting to a specific device, the user may verify the desired timing. Solve tough timing problems with full delay-annotated simulation models created by the fitter.

Atmel-Synario Simulator doesn't need architecture specific libraries and models. Simply identify which portion of the design you want to simulate and the stimulus you want applied. Then press "go". In batch mode, you can start and stop simulation from the control panel. Or you can explore your circuit's functionality interactively. Verilog language support also assures timely device support.

The Verilog simulation option includes a waveform viewer display that resembles a logic analyzer format. The waveform viewer updates whenever you simulate, even after each step of single-step session. Once a simulation runs, the values at the cursor in the waveform viewer are "dynamically backnotated" into the schematic. This allows you to debug your hierarchical design by viewing the logic values of the buried nets in the schematic as you move the cursor in the waveform viewer. To view a new signal, just "probe" the new in the schematic and the signal will appear in the waveform viewer.



Note: Cross-probing between the schematic and waveform viewer ties simulation results directly back to the source for faster and easier interpretation. Results update each time you single-step the simulator.

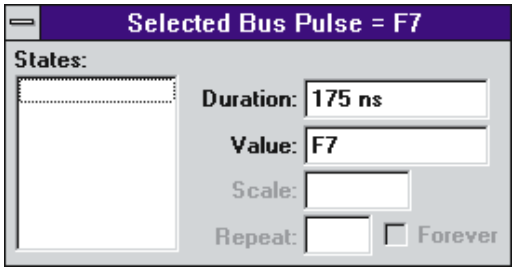


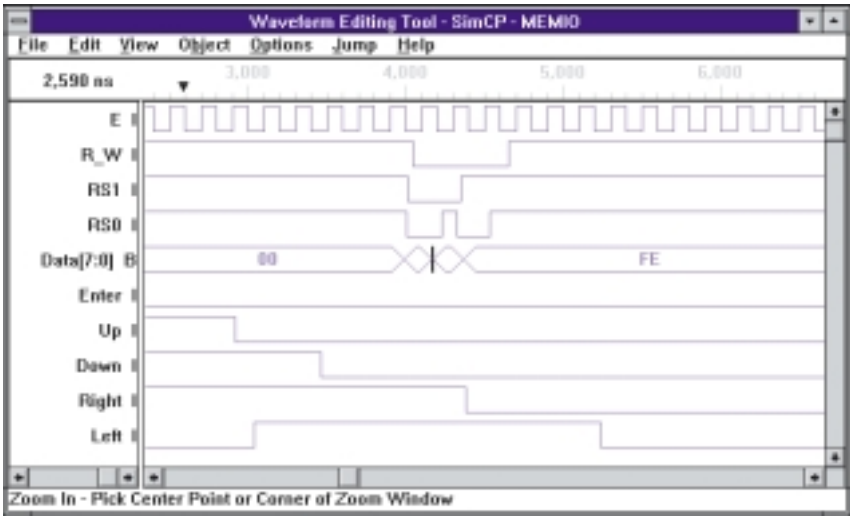
Multiple entry methods:

- Use the best one fir the application
- Mix methods for efficient design
- Quick translation of existing designs

Waveform Editor/Viewer

Fast simulation analysis and debug are at your fingertips with waveform editor. The powerful waveform editor enables simple stimulus generation, and easy result viewing. It's simple to add, delete, or move signals and show buses as a group. The viewer display is updated while simulating (for each simulation step).





Peak VHDL – Simulator Option

The Accolade Peak VHDL professional edition simulator is a powerful, easy-to-use system for design entry and simulation using VHDL. The product includes advanced, high-speed VHDL analyzer and elaborator, and support for IEEE-1076.1987 and IEEE-1076.1993 language standards. Built-in, accelerated support for IEEE-1164 standard logic is included as well as support for IEEE-1076.3 (synthesis/numeric) package. A VHDL hierarchy browser, waveform interface and context-sensitive VHDL code editor add to the powerful capabilities of this option.

Ordering Information

Part Number	System	Description
ATDS1100PC	Atmel-Synario Basic	Schematic and ABEL entry with fitters
ATDS1120PC	Atmel-Synario Verilog Simulation (Option)	Verilog functional and timing simulator
ATDS1130PC	Atmel-Synario VHDL Synthesis (Option)	Synthesis - IEEE-1076.1993
ATDS1140PC	Atmel-Synario VHDL Simulation (Option)	Peak VHDL simulator

System Requirements

Environment	Windows (95, 98 or NT)	
RAM	16MB	
Hard Disk	80MB	
Processor	Intel or compatible	Pentium
System Peripherals	Parallel Port	For security key
	Microsoft Mouse or compatible	Pointing device
	CD-ROM	For program loading and updates
	3-1/2" disk drive	For program updates

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

0714C–09/99/xM