NBSG11BAEVB

Evaluation Board Manual for NBSG11

ON Semiconductor®

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EVALUATION BOARD MANUAL

DESCRIPTION

This document describes the NBSG11 evaluation board and the appropriate lab test setups (See Figure 1). It should be used in conjunction with the NBSG11 data sheet which contains full technical details on the device specification and operation.

The evaluation board is designed to facilitate a quick evaluation of the NBSG11 GigaComm™ Clock Driver. The NBSG11 is designed to support the distribution of clock/data signals at high operating frequencies and produces two equal differential clock/data outputs from a single input clock/data. The Reduced Swing ECL (RSECL) output ensures minimal noise and fast switching edges.

The evaluation board is implemented in two layers for higher performance. For standard lab setup and test, a split (dual) power supply is required enabling the 50 ohm impedance from the scope to be used as termination of the ECL signals ($V_{TT} = V_{CC} - 2.0$ V, in split power supply setup, V_{TT} is the system ground).

What measurements can you expect to make?

With this evaluation board, the following measurements could be performed in single-ended(1) or differential modes of operation:

- Jitter
- Output Skew
- Gain/Return Loss
- Eye Pattern Generation
- Frequency Performance
- Output Rise and Fall Time
- V_{IHCMR} (Input High Common Mode Range)

1. Single-ended measurements can only be made at V_{CC} - V_{EE} = 3.3 V using this board setup.

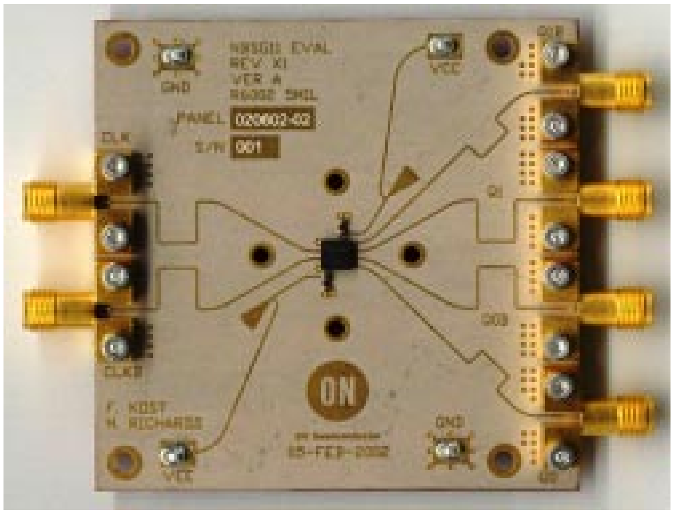


Figure 1. NBSG11 Evaluation Board

Setup for Time Domain Measurements

Table 1. Basic Equipment

Description	Example Equipment (Note 1)	Qty.
Power Supply with 2 outputs	HP6624A	1
Oscilloscope	TDS8000 with 80E01 Sampling Head (Note 2)	1
Differential Signal Generator	HP 8133A, Advantest D3186	1
Matched high speed cables with SMA connectors	Storm, Semflex	6
Power Supply cables with clips		3

1. Equipment used to generate example measurements within this document.
2. 50 GHz sample module used (for effective rise, fall and jitter performance measurement)

Setup

Step 1:

Connect Power

1a: Three power levels must be provided to the board for V_{CC}, V_{EE}, and GND via the surface mount clips. Using the split power supply mode, GND = V_{TT} = V_{CC} – 2.0 V.

Power Supply Connections	
3.3 V Setup	**2.5 V Setup**
V_{CC} = 2.0 V (Two Places)	V_{CC} = 2.0 V (Two Places)
V_{TT} = GND (One Place)	V_{TT} = GND (One Place)
V_{EE} = -1.3 V (One Place)	V_{EE} = -0.5 V (One Place)

Step 2:

Connect Inputs

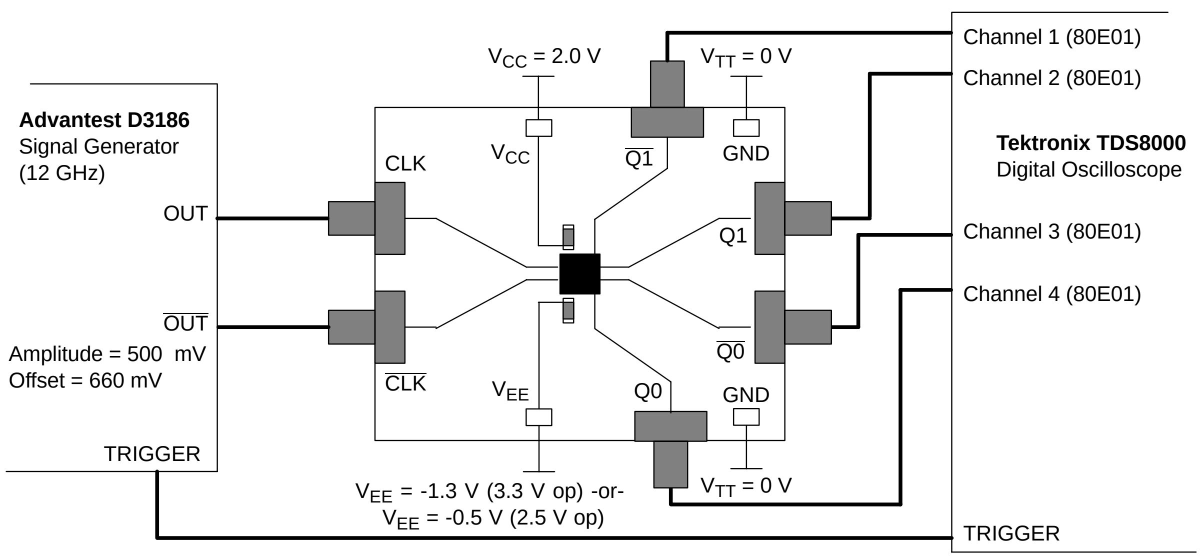
For Differential Mode (3.3 V and 2.5 V operation)

2a: Connect the differential output of the generator to the differential input of the device (CLK and $\overline{CLK}$).

For Single-Ended Mode (3.3 V operation only)

2a: Connect the AC coupled single-ended output generator to input.

NOTE: For best results, unconnected input should be terminated to V_{TT} through 50 Ω resistor



NOTE: All differential cable pairs ***must be*** matched.

Figure 2. NBSG11 Board Setup - Time Domain (Differential Mode)

Setup (continued)

Step 3:

Setup Input Signals

3a: Set the signal generator amplitude to 500 mV.

NOTE: The signal generator amplitude can vary from 75 mV to 900 mV to produce a 400 mV DUT output.

3b: Set the signal generator offset to 660 mV (the center of a nominal RSECL output).

NOTE: The V_{IHCMR} (Input High Voltage Common Mode Range) allows the signal generator offset to vary as long as V_{IH} is within the V_{IHCMR} range. Refer to the device data sheet for further information.

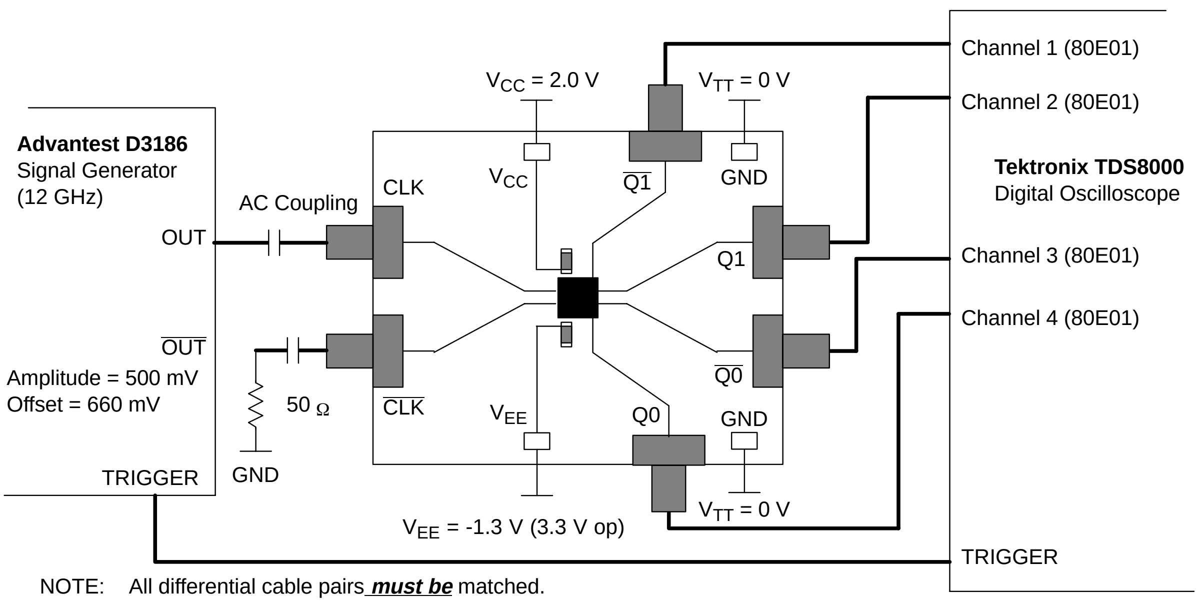
3c: Set the generator output for a PRBS data signal, or for a square wave clock signal with a 50% duty cycle.

Step 4:

Connect Output Signals

4a: Connect the outputs of the device (Q0, Q1, …) to the oscilloscope. The oscilloscope sampling head must have internal 50 Ω termination to ground.

NOTE: Where a single output is being used, the unconnected output for the pair ***must be*** terminated to V_{TT} through a 50 Ω resistor for best operation. Unused pairs may be left unconnected. Since V_{TT} = 0 V, a standard 50 Ω SMA termination is recommended.



NOTE: All differential cable pairs ***must be*** matched.

Figure 3. NBSG11 Board Setup - Time Domain (Single-Ended Mode)

Setup for Frequency Domain Measurements

Table 2. Basic Equipment

Description	Example Equipment (Note 3)	Qty.
Power Supply with 2 outputs	HP 6624A	1
Vector Network Analyzer	R&S ZVK (10MHz to 40 GHz)	1
180° Hybrid Coupler	Krytar Model #4010180	1
Bias Tee with 50 Ω resistor termination	Picosecond Model #5542-219	1
Matched high speed cables with SMA connectors	Storm, Semflex	3
Power Supply cables with clips		3

3. Equipment used to generate example measurements within this document.

Setup

Step 1:

Connect Power

1a: Three power levels must be provided to the board for V_{CC}, V_{EE}, and GND via the surface mount clips. Using the split power supply mode, GND = V_{TT} = V_{CC} – 2.0 V.

Power Supply Connections	
3.3 V Setup	**2.5 V Setup**
V_{CC} = 2.0 V (Two Places)	V_{CC} = 2.0 V (Two Places)
V_{TT} = GND (One Place)	V_{TT} = GND (One Place)
V_{EE} = -1.3 V (One Place)	V_{EE} = -0.5 V (One Place)

NOTE: For frequency domain measurements, 2.5 V power supply is not recommended because additional equipment (bias tee, etc.) is needed for proper operation. The input signal has to be properly offset to meet V_{IHCMR} range of the device.

Setup Test Configurations For Differential Operation

Small Signal Setup

Step 2:	**Input Setup** 2a: Calibrate VNA from 1.0 GHz to 12 GHz. 2b: Set input level to –35 dBm at the output of the 180° Hybrid coupler (input of the DUT).
Step 3:	**Output Setup** 3a: Set display to measure S21 and record data.

Large Signal Setup

Step 2:	**Input Setup** 2a: Calibrate VNA from 1.0 GHz to 12 GHz. 2b: Set input levels to -2.0 dBm (500 mV) at the input of DUT.
Step 3:	**Output Setup** 3a: Set display to measure S21 and record data.

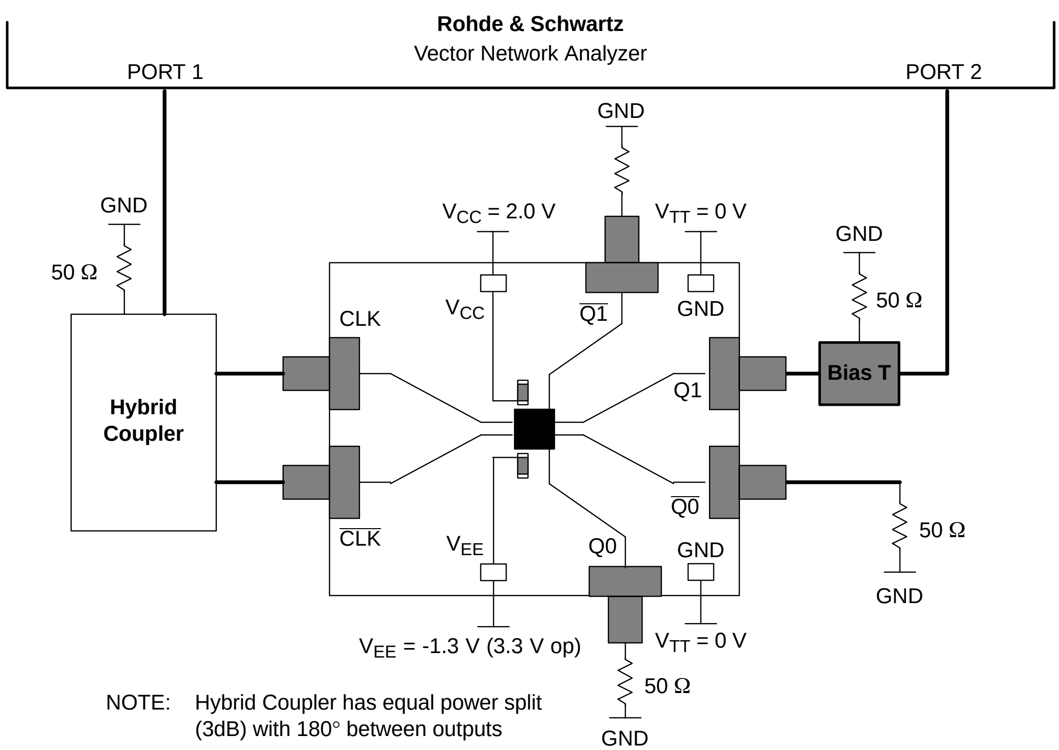


Figure 4. NBSG11 Board Setup – Frequency Domain (Differential Mode)

Setup Test Configurations For Single-Ended Operation

Single-Ended Mode – Small Signal

Step 2:	**Input Setup** 2a: Calibrate VNA from 1.0 GHz to 12 GHz. 2b: Set input level to –35 dBm at the input of DUT.
Step 3:	**Output Setup** 3a: Set display to measure S21 and record data.

Single-Ended Mode – Large Signal

Step 2:	**Input Setup** 2a: Calibrate VNA from 1.0 GHz to 12 GHz. 2b: Set input levels to +2.0 dBm (500 mV) at the input of DUT.
Step 3:	**Output Setup** 3a: Set display to measure S21 and record data.

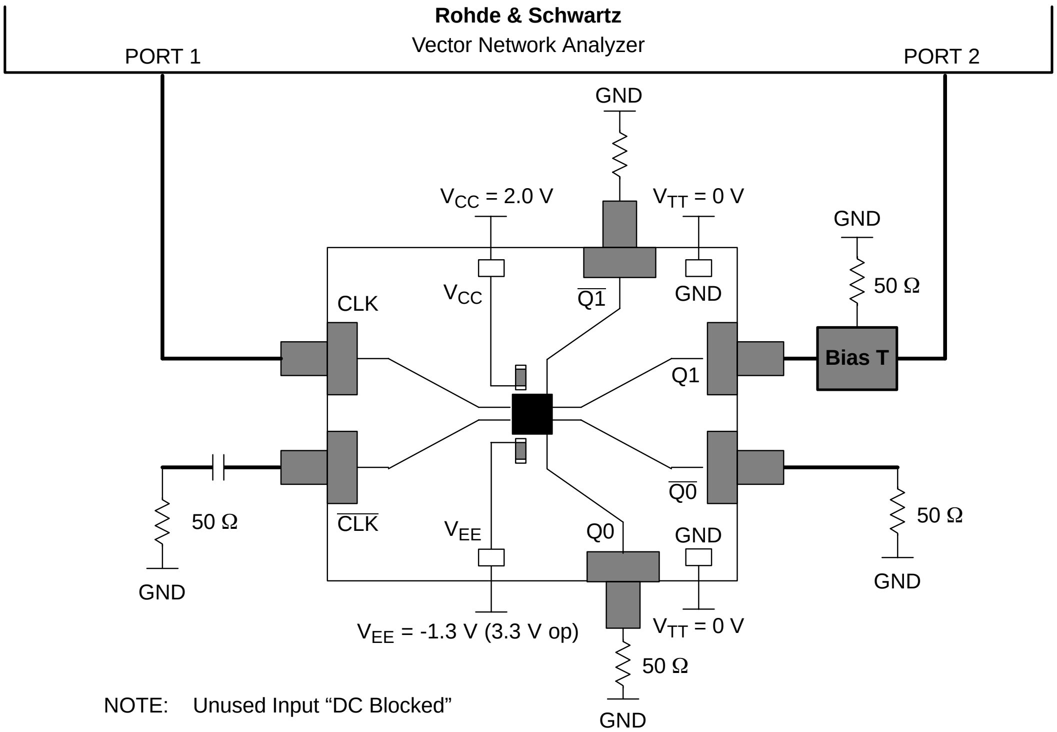


Figure 5. NBSG11 Board Setup – Frequency Domain (Single-Ended Mode)

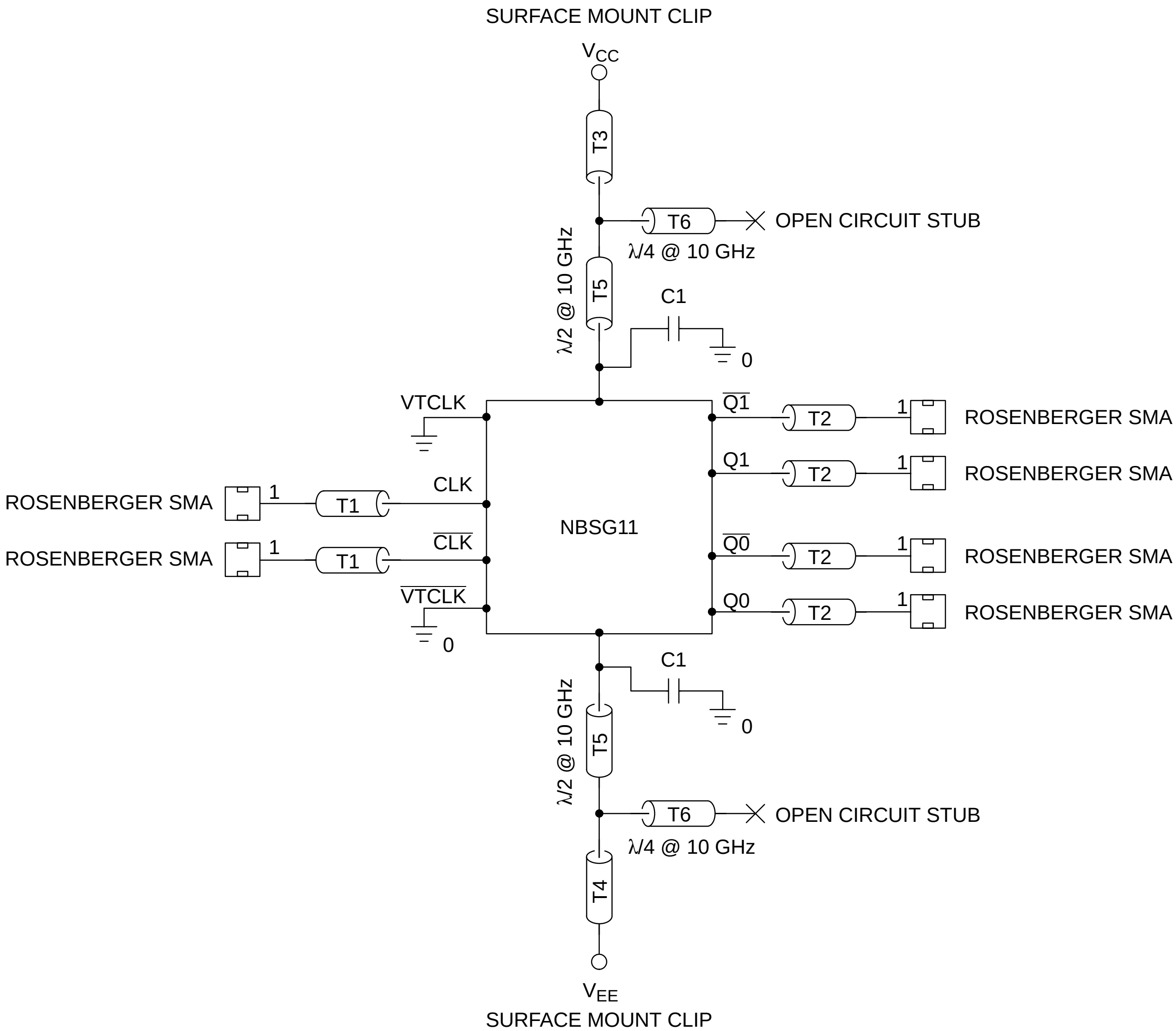
More Information About Evaluation Board

Design Considerations for >10 GHz operation

While the NBSG11 is specified to operate at 12GHz, this evaluation board is designed to support operating frequencies up to 20 GHz.

The following considerations played a key role to ensure this evaluation board achieves high-end microwave performance:

- Optimal SMA connector launch
- Minimal insertion loss and signal dispersion
- Accurate Transmission line matching (50 ohms)
- Distributed effects while bypassing and noise filtering



NOTE: C1 = Decoupling cap and Tx = 50 Ω Transmission line

Figure 6. Evaluation Board Schematic

Table 3. Parts List

Part No	Description	Manufacturer	WEB address
NBSG11BA	Differential Receiver/Driver with RSECL Outputs	ON Semiconductor	http://www.onsemi.com/nbsg11
32K243-40ME3	Gold plated connector	Rosenberger	http://www.rosenberger.de
CO6BLBB2X5UX	2 MHz – 30 GHz capacitor	Dielectric Laboratories	http://www.dilabs.com

Table 4. Board Material

Material	Thickness
Rogers 6002	5.0 mil
Copper Plating	32 mil

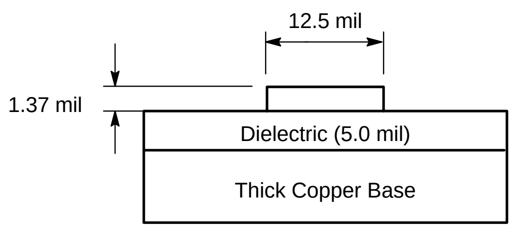


Figure 7. Board Stack-up

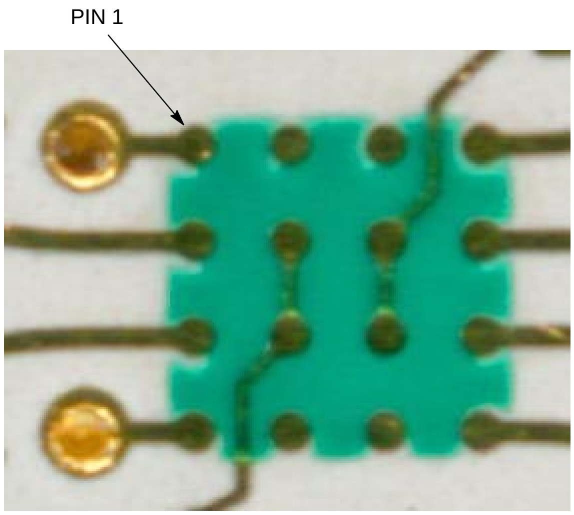
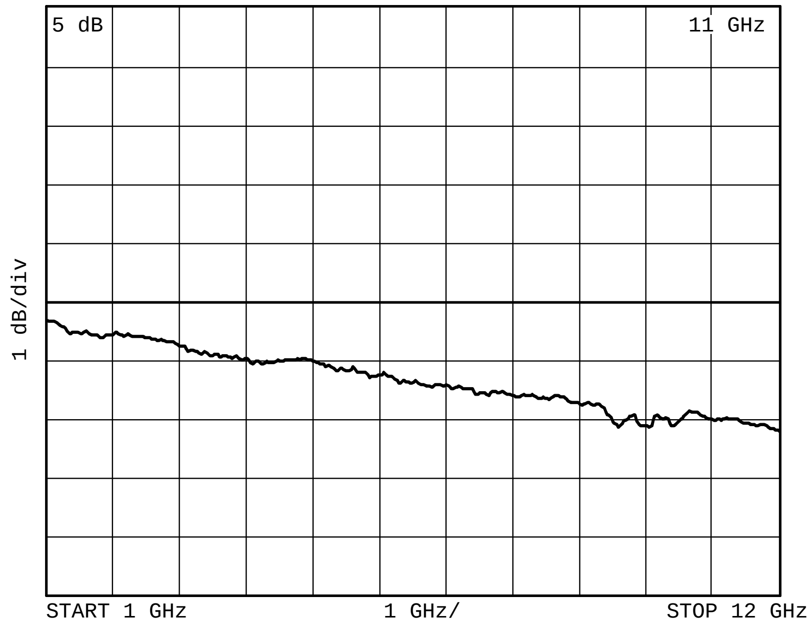


Figure 8. Layout Mask for NBSG11



NOTE: The insertion loss curve can be used to calibrate out board loss if testing under small signal conditions.

Figure 9. Insertion Loss

EXAMPLE MEASUREMENTS IN TIME DOMAIN ($V_{CC} - V_{EE}$ = 3.3 Volts)

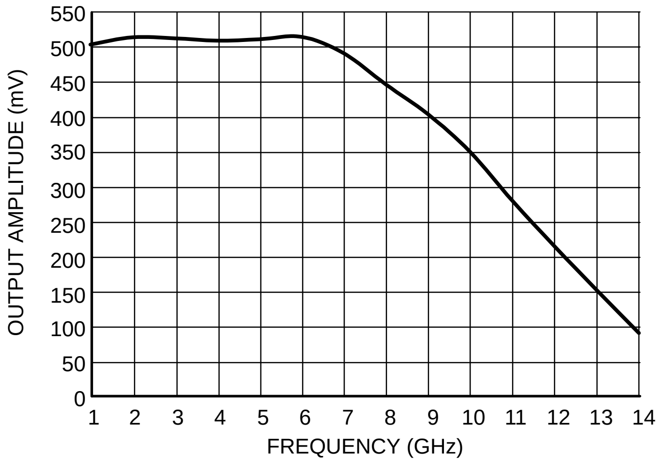


Figure 10. Fmax - Amplitude vs. Frequency (NBSG11: V_{CC} - V_{EE} = 3.3 V @ 25°C, Input Amplitude 500 mV)

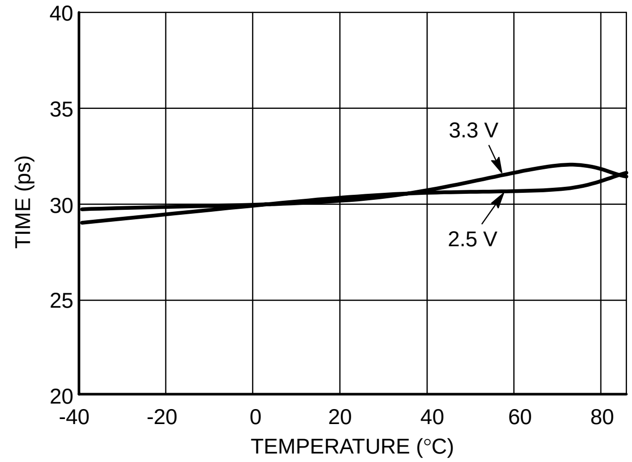


Figure 11. NBSG11 T_r vs. Temperature and Supply Voltage

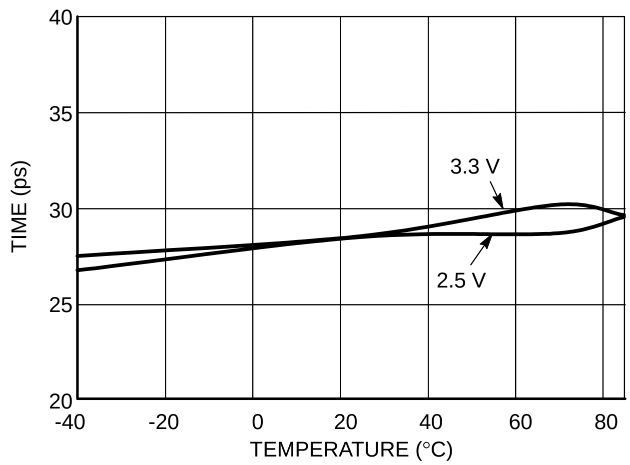
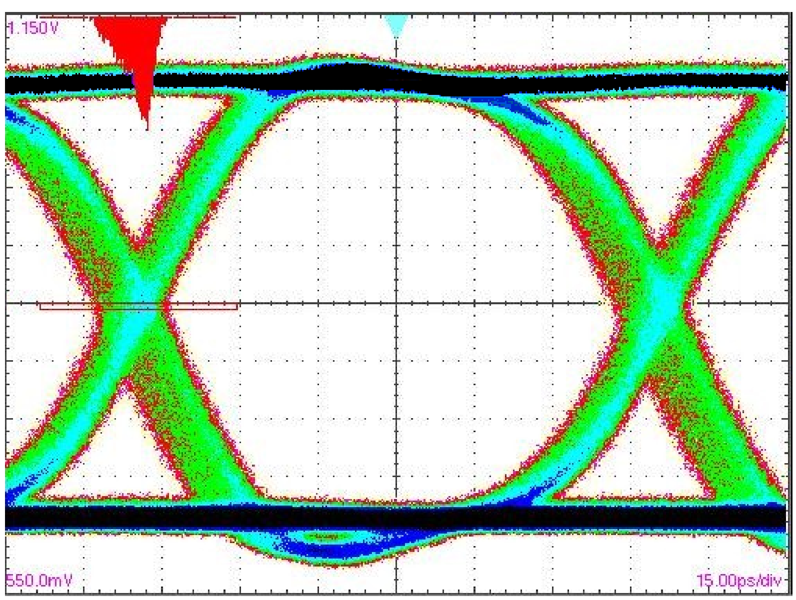


Figure 12. NBSG11 T_f vs. Temperature and Supply Voltage



Pk-Pk Jitter = 18 ps

Figure 13. NBSG11: Eye Diagram at 10 Gbps with PRBS 2^31-1 (total system jitter including signal generator is shown)

EXAMPLE MEASUREMENTS IN FREQUENCY DOMAIN (V_{CC} – V_{EE} = 3.3 Volts)

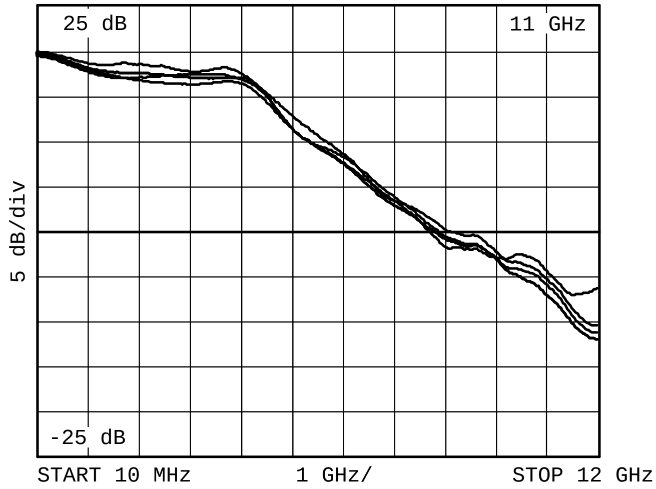


Figure 14. NBSG11: Small Signal Gain (S21) Q0 - Q1B

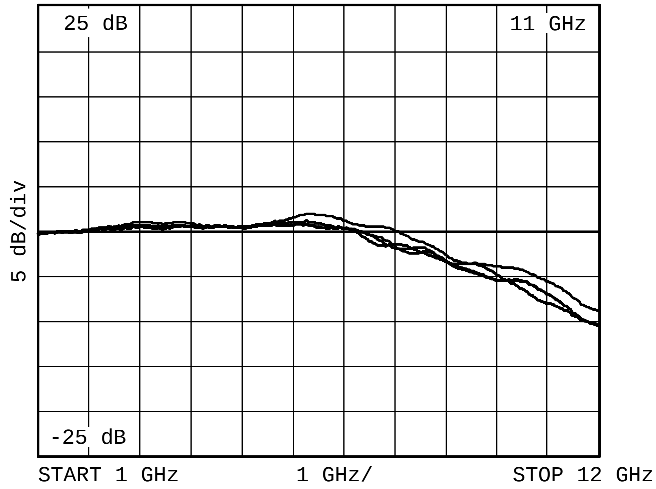


Figure 15. NBSG11: Large Signal Gain (S21) Q0 – Q1B

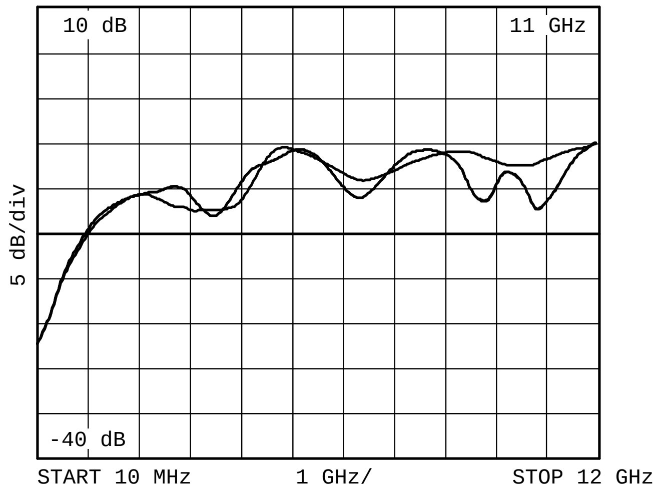


Figure 16. NBSG11: D, DB Return Loss (S11) Q0 – Q1B

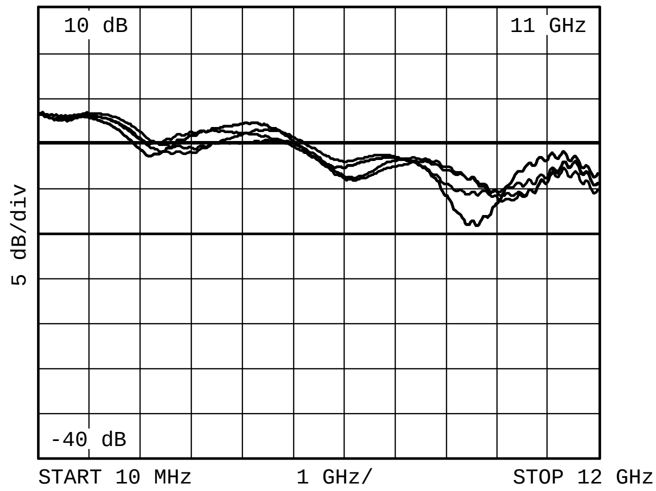


Figure 17. NBSG11: Return Loss (S22) Q0 - Q1B

ADDITIONAL EVALUATION BOARD INFORMATION

www.onsemi.com

In all cases, the most up-to-date information can be found on our website.

- Sample orders for devices and boards
- New Product updates
- Literature download/order
- IBIS and Spice models

References

NBSG11/D, Data Sheet, *NBSG11 Differential Receiver/Driver with RSECL Outputs.*

AND8077/D, Application Note, *GigaComm™ (SiGe) SPICE Modeling Kit.*

AND8075/D, Application Note, *Board Mounting Considerations for the FCBGA Packages.*

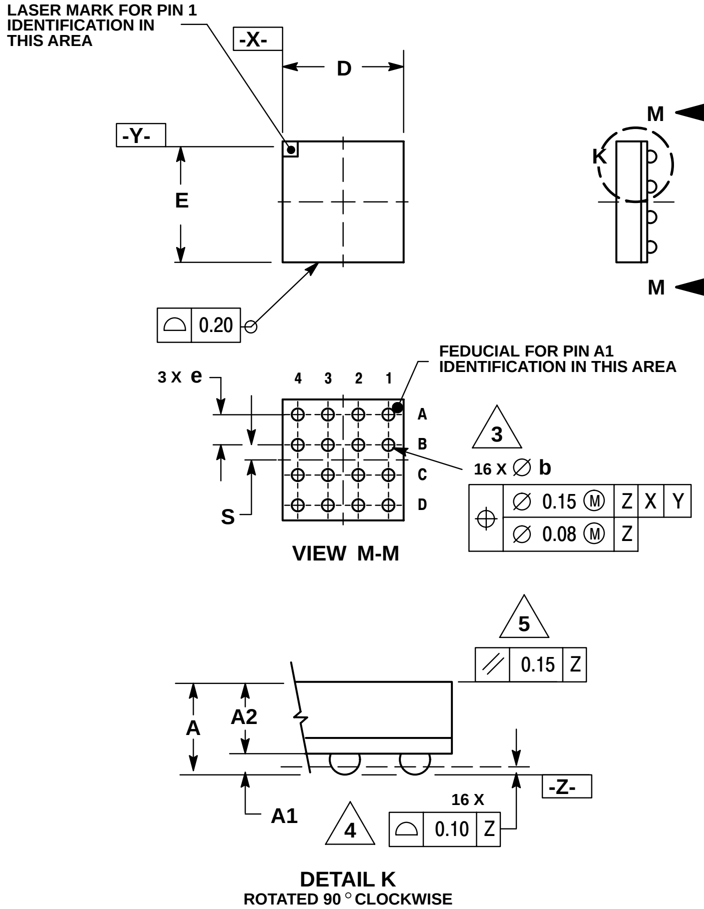
BRD8017/D, Brochure, *Clock and Data Management Solutions.*

ORDERING INFORMATION

Orderable Part No	Description	Package	Shipping
NBSG11BA	Differential Receiver/Driver with RSECL Outputs	4X4 mm FCBGA/16	100 Units/Tray
NBSG11BAR2	Differential Receiver/Driver with RSECL Outputs	4X4 mm FCBGA/16	500 Units/Reel
NBSG11BAEVB	NBSG11 Evaluation Board		

PACKAGE DIMENSIONS

FCBGA-16
BA SUFFIX
PLASTIC 4X4 (mm) BGA FLIP CHIP PACKAGE
CASE 489-01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40 MAX	
A1	0.25	0.35
A2	1.20 REF	
b	0.30	0.50
D	4.00 BSC	
E	4.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

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