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April 1st, 2010 Renesas Electronics Corporation

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Customer Notification

IE-789860-NS-EM1[™]

Emulation Board

Operating Precautions

Target Devices

uPD789860 uPD78E9860A uPD789861 uPD78E9861A uPD789052 uPD789062

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IE-789860-NS-EM1

(A) Table of Operating Precautions

			IE-789860-NS-EM1			
No.	Outline	Control Code ^{Note}	A	В	С	D
1	No other interrupt is accepted w return interrupt is used (Technical Limitation)	hen key	x	1	1	~
2	Key return interrupt is static, not sensitive (Technical Limitation)	falling edge	x	x	1	1
3	Support for the uPD789052, uPl Subseries (Specification Change)	D789062	-	-	-	~
4	Modification of specification of 8 30 and 40 (Specification Change)	-bit timers	-	-	-	~
5	EEPROM guard function (Technical Limitation)		x	x	x	x

 \checkmark : Not applicable

X : Applicable

- : Specification is not supported

Note: The control code is the **second letter** from the left of the 10 digit serial number (version that have not been upgraded).

For upgraded versions, an upgrade label is affixed to the product. The version-up level on this sticker corresponds to the actual control code (i.e. the X in the V-UP LEVEL X indicates the control code X).

(B) Description of Operating Precautions

No. 1			cepted when ke	ey return interrupt is used		
	(Technical Lim Detail:	nitation)				
	Due to the interrupt request signal of the emulation chip is not cleared when the non - maskable interrupt of the key return signal is used, other interrupts cannot be accepted.					
	Workaround:.					
	The interrupt request signal of the emulation chip is cleared when the EI instruction has been executed. Therefore, be sure to execute the EI instruction in the key return interrupt vector routine if the non – maskable interrupt of the key return signal is used. If you do so, interrupt servicing of the key return signal is executed twice. Therefore it is necessary to suppress the second interrupt servicing. See the following example of software.					
	Example:		(Main routine	.)		
		 MOV STOP 	B,#0	; Clears interrupt counter		
	(Key return interrupt vector routine) VINTKR:			nterrupt vector routine)		
		INC EI MOV	B A,B	; Increments interrupt counter ; Clears interrupt request flag for emulation		
		CMP BZ	A,#02 \$KR_END0	; First interrupt ? ; Return processing if interrupt is second one.		
			Original key re	eturn processing.		
		BR	\$KR_END1			
	KR_END0:	MOV	B,#00			
	KR_END1:	RETI				
	Flow of operation in this example:					
	Occur Branc Incren El ins Execu Returr	rence of h to vector nenting in struction of tion of or n to main execut	or of key return nterrupt counter execution (kep iginal processir routine (pendi ion branches to	t pending while non-maskable interrupt is serviced) ng because interrupt is first interrupt (B = 1) ng El instruction is executed at this point and the vector of key return processing again)		
			rupt counter (E counter and brack	anch to return processing because interrupt is second one		

No. 2a	Key return interrupt is static, not falling edge sensitive (Technical Limitation)
	<u>Details</u> The key return interrupt (INTKR1) should be generated by the input of the falling edge of P40/KR10 to P43/KR13, but is inadvertently generated by a low level input.

No. 3	Support for the uPD789052, uPD789062 Subseries (Technical Limitation)
	<u>Details</u> The uPD789052, uPD789062 Subseries is supported in IE-789860-NS-EM1 control code D or later.

No. 4	Modification of specification of 8-bit timers 30 and 40 (Technical Limitation)
	<u>Details</u> The carrier generator output control register 40 (TCA40) has been changed from write-only (W) to read/write (R/W) in IE-789860-NS-EM1 control code D or later due to the specification change in the target device.

No. 5		EEPROM guard function			
	(Technical Lim	(Technical Limitation)			
	<u>Details</u> A guard break occurs when an instruction that selects the output of 8-bit timer 40 as the count clock (data write time) of the EEPROM timer is executed and reading the EEPROM is enabled (ERE10 = 1) after the operation of 8-bit timer counter 40 is stopped.				
	Example 1	MOV EEWC10,#68H SET1 ERE10	; Selects EEPROM timer count clock ; Enables EEPROM read		
	Example 2		; Selects EEPROM timer count clock ; Enables EEPROM read		
	the ins (2) When	stop the operation of 8-b truction in Example 1 or enabling EEPROM read the count clock for the El tion.	bit timer counter 40 when enabling EEPROM read using Example 2 . while the operation of 8-bit timer counter 40 is stopped, EPROM timer and enable EEPROM read using one ; Enables EEPROM read at the same time as selecting EEPROM timer count clock		

Valid Specification

ltem	Date published	Document No.	Document Title
1	July 2003	U16499EJ1V0UM00	User's Manual IE-789860-NS-EM1

(C) Revision History

ltem	Date published	Document No.	Comment
3	March 04 th ,2005	TPS-LE-OP-T9860-D	1 st release in new format