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User's Manual

LCE-780308-EM Emulation Board

Preliminary

Document No. U18142EU1V0UM00 (1st edition)
Preliminary Version 10/26/01

CHAPTER 1 GENERAL INFORMATION

The LCE-780308-EM is an emulation board or daughter board for the LCE-K0 development system, supporting NEC's uPD780058, uPD78054, uPD78064, and uPD780308 sub-series of 8-bit single-chip microcontrollers. By combining this daughter board with the LCE-78K0 motherboard, these sub-series can be emulated efficiently. The LCE-780308-EM is shipped with the following contents:

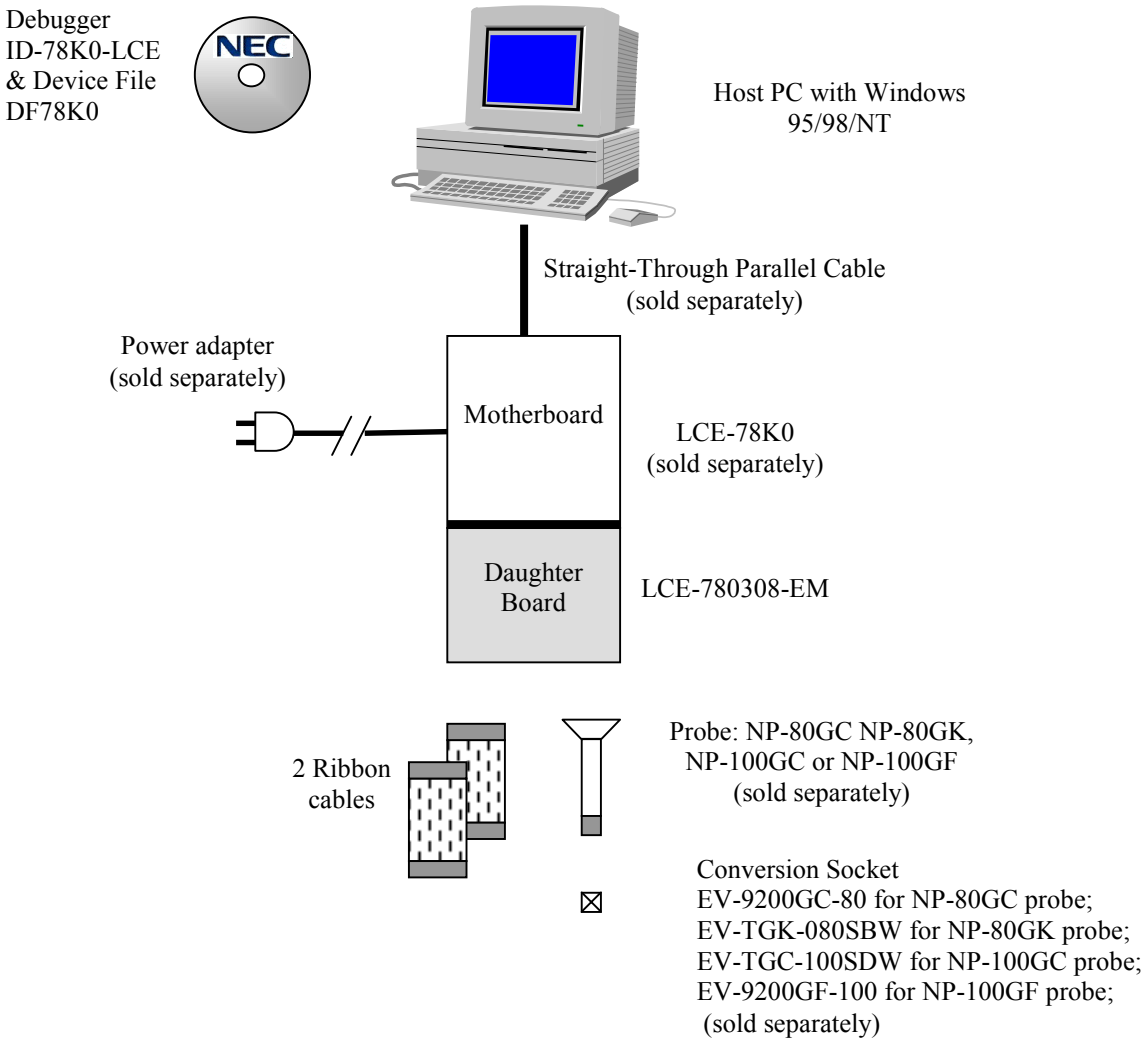
- LCE-780308-EM daughter board
- User's manual
- Two 50-pin ribbon cables
- CD-ROM containing debugger, assembler, compiler, device files, and documentation.

1.1. Basic Configuration

Parameter		Description
Subseries Supported		Target Devices
	uPD780058 subseries	uPD780053GC, uPD780053GK, uPD780054GC, uPD780054GK, uPD780055GC, uPD780055GK, uPD780056GC, uPD780056GK, uPD780058GC, uPD780058GK
	uPD78054 subseries	uPD78052GC, uPD78052GK, uPD78053GC, uPD78053GK, uPD78054GC, uPD78054GK, uPD78055GC, uPD78055GK, uPD78056GC, uPD78056GK, uPD78058GC, uPD78058GK
	uPD78064 subseries	uPD78062GC, uPD78062GF, uPD78063GC, uPD78063GF, uPD78064GC, uPD78064GF
	uPD780308 subseries	uPD780306GC, uPD780306GF, uPD780308GC, uPD780308GF
Clock supply		Internal: Installed on the motherboard External: Pulse input
Low-voltage compatible		At least 2V

1.2. LCE-K0 System Configuration

The LCE-K0 system configuration is as shown below. The system consists of a host PC, running the ID78K0-LCE debugger, communicating through the PC's LPT1: parallel port via a standard parallel cable, to the combination of LCE-78K0 motherboard plus LCE-780308-EM daughter board. For connection to a target system, either a pair of 50-pin ribbon cables, or the combination of an NEC probe plus socket adapter, can be used.



CHAPTER 2 COMPONENTS

This chapter introduces the main components of the LCE-780308-EM daughter board unit.

2.1. Daughter Board Layout

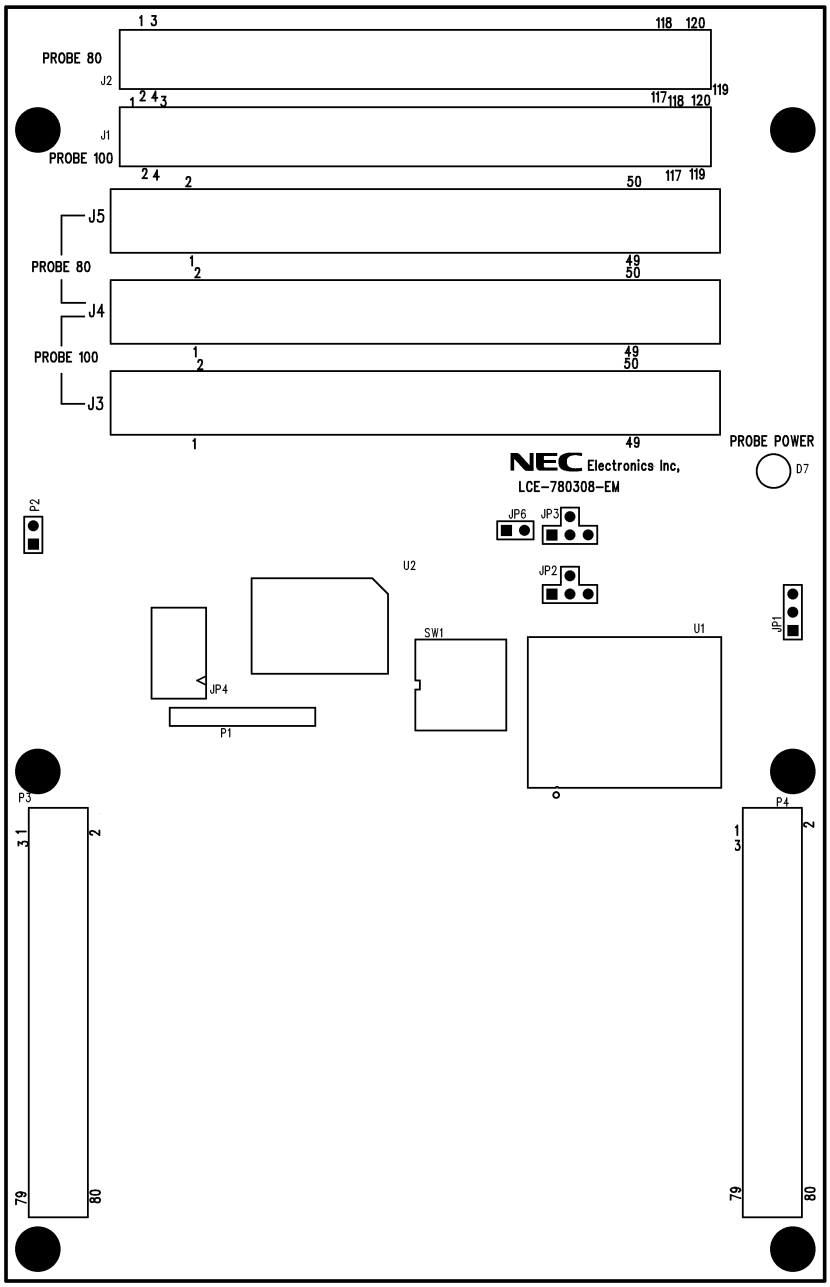


Figure 2.1-1 LCE-780308 Top Layout

This is a drawing of the top of the LCE-780308-EM board; this side will face upward in the assembled system.

U1 is a uPD78P0308 device, and U2 is a uPD78P054 device. Together these two devices provide emulation of the peripheral devices such as parallel ports, serial ports, timers, LCD drivers, etc., for the supported 78K0 devices.

J1, J2, J3, J4, and J5 are connectors to the user target system. These connectors contain all the pins available on the emulated device. J1 and J2 are KEL connectors for device probes, while J3, J4 and J5 are dual-row male shrouded headers with latching levers for the ribbon cables. Please see the section below about ribbon cables and probes, and Chapter 4 for pin assignments of these connectors.

D7 is an LED which is used to indicate that power is applied to the target system.

JP1, JP2, JP3, and JP6 are jumpers for analog voltages. They allow the optional connection of analog signals AVDD, AVREF0, AVREF1, and AVSS to power, ground or reference voltages provided on the LCE-780308-EM board, when these analog voltages are not provided in the user target system.

JP4 is provided for optional on-board connection of LCD display voltage divider resistors. In normal operation, the voltage divider for LCD display voltages should be located on the user target system, and JP4 should be left unconnected.

SW1 is a dip switch for enabling or disabling pull-up resistors on the P60-P63 input pins to emulate mask options of the target device. These mask option pull-up resistors are also switched in or not by software-controlled switches, under control of the ID78K0-LCE debugger. In normal operation, the switches on SW1 should all be set to the OFF position.

P1 is a connector for programming PLD logic on the LCE-780308-EM. It is used only for factory programming, and should be left unconnected in normal operation.

P2 is a connector for an external trigger input to the LCE-K0 system.

P3 and P4 are the connectors for the motherboard. The motherboard connects on top of the daughter board.

2.2. J3, J4, J5 Ribbon Cables

The ribbon cables are two 50-pin female-to-female cables that connect the LCE-K0 system to the user target. One end of the ribbon cables connects to the dual-row male shrouded headers with latching levers on the daughter board (either J3 and J4, or J4 and J5), and the other connects to matching connectors on the user target.

Devices supported by the LCE-780308-EM board fall into two categories: 80-pin devices in either a GC footprint (14 x 14 mm QFP) or a GK footprint (12 x 12 mm TQFP); or 100-pin devices in either a GC footprint (14 x 14 mm LQFP) or GF footprint (14 x 20 mm QFP).

In order to emulate 80 or 100 pins, two ribbon cables are necessary to carry the device signals. These ribbon cables are included with the daughter board. The side of the ribbon cable that has a red stripe is pin 1.

To emulate 80-pin devices, the ribbon cables are connected to J4 and J5; these connectors carry all signals necessary for emulation of 80-pin devices. The legend "PROBE 80" is marked on the board next to these connectors. Please refer to Table A-1 in Chapter 4 for pinouts of the Probe 80 ribbon cables.

To emulate 100-pin devices, the ribbon cables are connected to J3 and J4; these connectors carry all signals necessary for emulation of 100-pin devices. The legend "PROBE 100" is marked on the board next to these connectors. Please refer to Table A-2 in Chapter 4 for pinouts of the Probe 100 ribbon cables.

2.3. J1 and J2 Emulation Probe Connectors (Optional)

An emulation probe is optional. This is another method of connecting to the user target, provided a conversion socket/adapter is installed on the target. Select the probe best suited for your target device package.

For target devices in the 80-pin plastic QFP package (GC suffix) or 80-pin plastic TQFP package (GK suffix), an appropriate probe and socket adapter to accept the probe should be used. These are the NP-80GC and NP-80GK probes. For connection of these probes to the LCE-780308-EM, connector J2 should be used; this connector is labelled "PROBE 80".

For target devices in the 100-pin plastic LQFP package (GC suffix) or 100-pin plastic QFP package (GF suffix), an appropriate probe and socket adapter to accept the probe should be used. These are the NP-100GC and NP-100GF probes. For connection of this probe to the LCE-780078-EM, connector J1 should be used; this connector is labelled "PROBE 100".

Table 2.3-1 Emulation Probe and Socket

Example Target Device	Emulation Probe	Conversion Socket/Adapter
uPD780058GC	NP-80GC (connected to J2)	EV-9200GC-80
uPD780058GK	NP-80GK (connected to J2)	EV-TGK-080SBW
uPD780308GC	NP-100GC (connected to J1)	EV-TGC-100SDW
uPD780308GF	NP-100GF (connected to J1)	EV-9200GF-100

Please refer to Chapter 4 for pin assignments.

2.4. P60-P63 Pull-Up Resistor Mask Options

The uPD78054 and uPD780058 subseries target devices emulated by the LCE-780308-EM board have factory-programmable mask options, allowing pull-up resistors to be attached to the lower four bits of Port 6, P60 through P63. These ports are open-drain N-channel I/O ports, and can be configured as open-drain outputs by omitting the pull-up resistor mask option.

These optional pull-up resistors are provided on the LCE-780308-EM board, and can be connected or disconnected to the appropriate P60-P63 signals, emulating the mask options. The mask option pull-up resistors can be switched in or not by using either the ID78K0-LCE debugger software, or by using the SW1 hardware switch. In normal operation, the ID78K0-LCE debugger would be used to control this option, and the SW1 hardware switches would all be set to OFF.

2.4.1. Setting P60-P63 Mask Options with ID78K0-LCE Software

The factory-programmable mask options can be emulated by setting ID78K0-LCE debugger to turn on or off appropriate software-controllable switches, to connect or disconnect on-board pull-up resistors to P60-P63. These switches should be set for the mask options desired in the final target chip.

The software controlled switches are turned on or off using the Mask Options dialog box in the ID78K0-LCE debugger. From the Options menu, choose the Mask Options menu item. The Mask Options dialog box will be displayed. Select the desired port bit from the drop-down list box, select the desired setting (ON or OFF), and click the Set button. The appropriate software-controlled switch will be turned on or off.

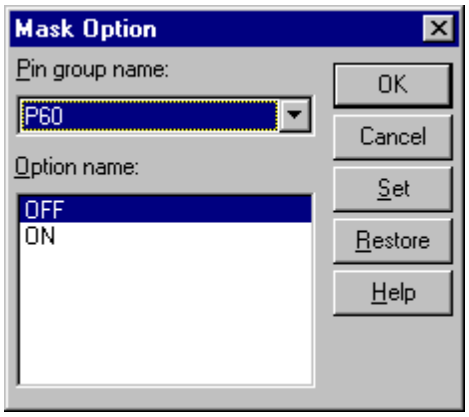


Figure 2.4-1 ID78K0-LCE Mask Option Dialog Box

Note: the ID78K0-LCE Mask Option dialog box also has an entry to set P07/XT1 as either P07 or XT1. This setting actually has no effect. See the section below on setting P07/XT1.

Table 2.4-1 ID78K0-LCE Settings for P60-P63 Mask Options

Port Bit	ID78K0-LCE Mask Option	Option Setting	Port Setting
P60	P60	OFF	P60 has no pull-up
		ON	P60 has 39K pull-up to VDD
P61	P61	OFF	P61 has no pull-up
		ON	P61 has 39K pull-up to VDD
P62	P62	OFF	P62 has no pull-up
		ON	P62 has 39K pull-up to VDD
P63	P63	OFF	P63 has no pull-up
		ON	P63 has 39K pull-up to VDD

The settings for the Mask Options may be saved in an ID78K0-LCE project file and reloaded, so it will not be necessary to set the Mask Options manually every time ID78K0-LCE is started.

However, it is also possible to set the hardware switch SW1 to switch in pull-up resistors for P60-P63. Note that if either the software switch or the hardware switch is on, the pull-up resistor is connected. In order to not have pull-up resistors connected to the P60-P63 bits, both the software and hardware switches must be off.

2.4.2. Setting P60-P63 Mask Options with SW1 Hardware Switches

The SW1 switches SW1-1 through SW1-4 will either connect or disconnect mask option pull-up resistors to the P60-P63 signals. Setting a switch to the ON position will connect the pull-up resistor, and setting it to OFF will disconnect the resistor.

Note that if the ID78K0-LCE software has set the corresponding software-controlled switch to ON, the pull-up resistor will be connected regardless of the setting of the hardware switch. Under normal operation, all SW1 switches should be set to OFF, so as not to interfere with the operation of the software-controlled switches in the ID78K0-LCE software.

Table 2.4-2 SW1 Settings for P60-P63 Mask Options

Port Bit	SW1 Switch	Switch setting	Port Setting
P60	SW1-1	Off	P60 has no pull-up
		On	P60 has 39K pull-up to VDD
P61	SW1-2	Off	P61 has no pull-up
		On	P61 has 39K pull-up to VDD
P62	SW1-3	Off	P62 has no pull-up
		On	P62 has 39K pull-up to VDD
P63	SW1-4	Off	P63 has no pull-up
		On	P63 has 39K pull-up to VDD

2.5. Using P07/XT1 As Input From Probe

The devices emulated by the LCE-780308-EM board have an input pin named P07/XT1 (or XT1/P07). This pin can be used either as a parallel input, read as bit 7 of port P0, or as the XT1 subclock source.

The ID78K0-LCE program has a Mask Option setting for port P07/XT1, setting it as either P07 (input port) or XT1 (subclock). This option setting has no effect. The actual probe pin for P07/XT1 can be used as either P07 or XT1 regardless of the Mask Option setting.

However, the LCE-78K0 motherboard does have an option allowing either a standard on-board 32KHz clock, or the input from the probe pin P07/XT1, to be supplied to the P07/XT1 input of the peripheral emulator device. In order to use the probe input as either P07 or XT1, the ID78K0-LCE configuration dialog must have the Subclock option set to "User", rather than "32KHz".

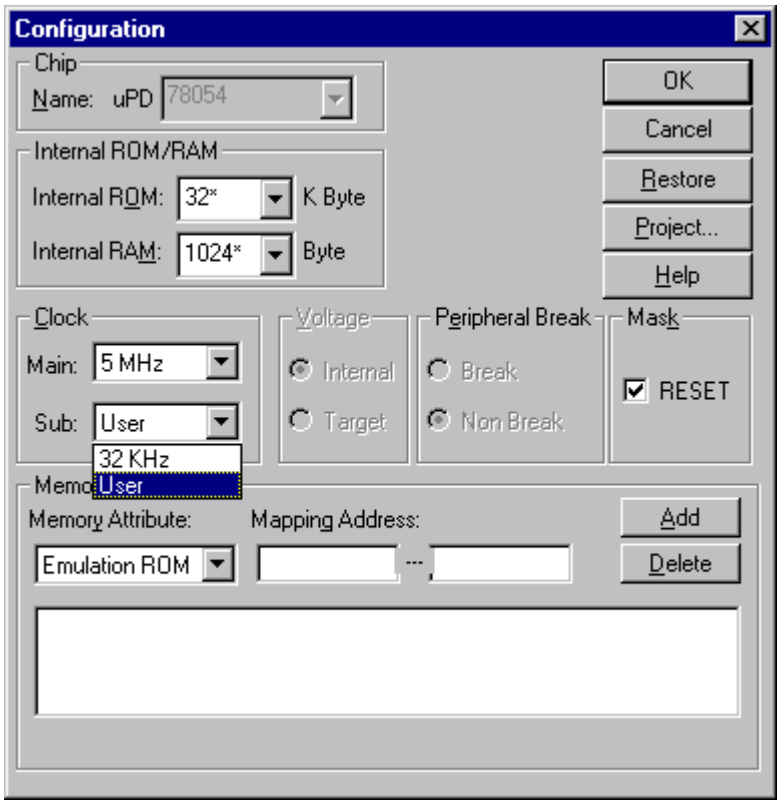


Figure 2.5-1 ID78K0-LCE Configuration Dialog Box

When the "32 KHz" option is selected in the Configuration dialog, the on-board 32 KHz clock source is connected to P07/XT1. Reading port P0 in this configuration will result in an indeterminate value for bit 7.

2.6. Jumper Settings for Analog Voltage Inputs

The target devices emulated by the LCE-780308-EM have analog voltage inputs to A/D converters, ANI0 to ANI7. In addition, the uPD78054 and uPD780058 subseries also have analog outputs from D/A converters, ANO0 and ANO1. These analog inputs and outputs require separate power (AVDD), ground (AVSS) and reference voltage (AVREF0 and AVREF1) inputs.

Normally these analog voltage inputs are connected in the target system, with AVSS connected to VSS and AVDD connected to VDD, and with AVREF0 and AVREF1 connected to a voltage references, which may also be VDD.

The jumpers on the LCE-780308-EM allow these analog voltage inputs to be connected to on-board voltage sources, in case these inputs are unconnected in the target system. The diagram below shows the pin numbering for these jumpers.

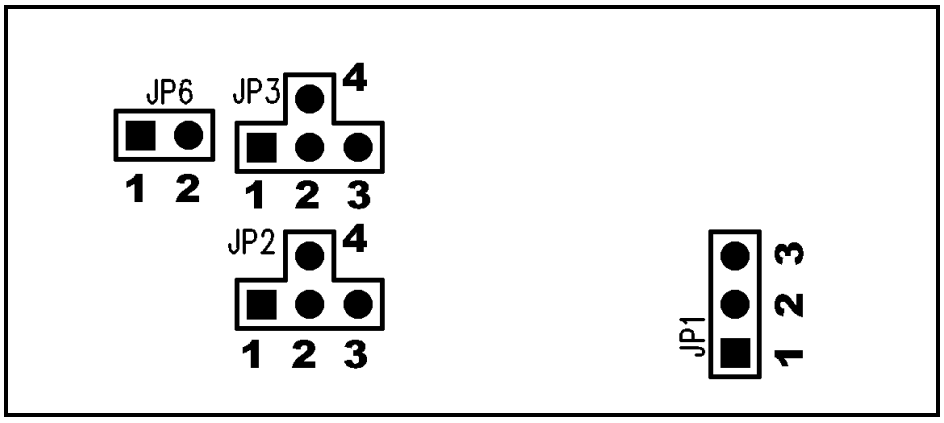


Figure 2.6-1 Analog Jumper Pin Numbering

2.6.1. JP1 AVDD Jumper Options

JP1 is a two-position jumper for AVDD. It allows AVDD on the peripheral emulator to be connected either to the AVDD input from the probe (default), or to VDD on the LCE-780308-EM. AVDD is used only for the uPD78054 and uPD780058 subseries; for the uPD78064 and uPD780308 subseries, AVDD should be connected to VDD.

Table 2-1 JP1 Settings for AVDD

JP1 Setting	AVDD Connection
JP1-2 to JP1-1	VDD on LCE-780308-EM
JP1-2 to JP1-3 *	AVDD on probe

* factory setting

2.6.2. JP2 AVREF0 Jumper Options

JP2 is a three-position jumper, arranged in a T-shape, for AVREF0. It allows AVREF0 on the peripheral emulator to be connected to AVREF0 on the probe (default), to ground, or to the AVDD pin on the peripheral emulator (which may be AVDD or VDD, as selected with JP1).

For the uPD78064 and uPD780308 subseries, AVREF0 is equivalent to the AVREF pin. If it is desired to connect AVREF to VDD for these devices, connect JP1 so that AVDD is connected to VDD.

Table 2.6-2 JP2 Settings for AVREF0

JP2 Setting	AVREF0 Connection
JP2-2 to JP2-1	AVDD as selected by JP1
JP2-2 to JP2-3	GND
JP2-2 to JP2-4 *	AVREF0 on probe

* factory setting

2.6.3. JP3 AVREF1 Jumper Options

JP3 is a three-position jumper, arranged in a T-shape, for AVREF1. It allows AVREF1 on the peripheral emulator to be connected to AVREF1 on the probe (default), to ground, or to the AVDD pin on the peripheral emulator (which may be AVDD or VDD, as selected with JP1). AVDD is used only for the uPD78054 and uPD780058 subseries; for the uPD78064 or uPD780308 subseries, AVREF1 should be jumpered to either GND or VDD (selected for AVDD with JP1).

Table 2.6-3 JP2 Settings for AVREF1

JP3 Setting	AVREF1 Connection
JP3-2 to JP3-1	AVDD as selected by JP1
JP3-2 to JP3-3	GND
JP3-2 to JP3-4 *	AVREF1 on probe

* factory setting

2.6.4. JP6 AVSS Jumper Options

JP6 is a two-pin jumper for AVSS. AVSS on the peripheral emulator is always connected to AVSS on the probe. When JP6 is inserted (default), AVSS is connected to ground, providing a closer ground reference for AVSS. For normal design, AVSS would always be connected to the ground, or VSS, pins of the target device.

Removing JP6 will disconnect AVSS from ground on the LCE-780308. In this case, AVSS in the target system should be connected to target ground.

Table 2.6-4 JP6 Settings for AVSS

JP6 Setting	AVSS Connection
Open	AVSS on probe
JP6-1 to JP6-2 *	GND on LCE-780308-EM and AVSS on probe

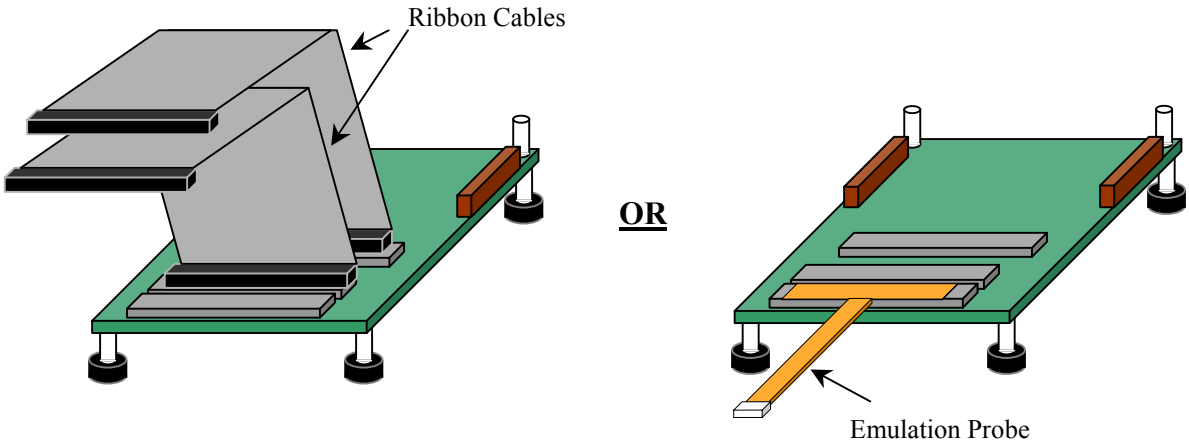
* factory setting

CHAPTER 3 INSTALLATION

This chapter explains how to connect the LCE-780308-EM to the LCE-78K0 and the user target system, and start operation of the LCE-K0 system.

3.1. Connect Probe Cables to LCE-780308-EM

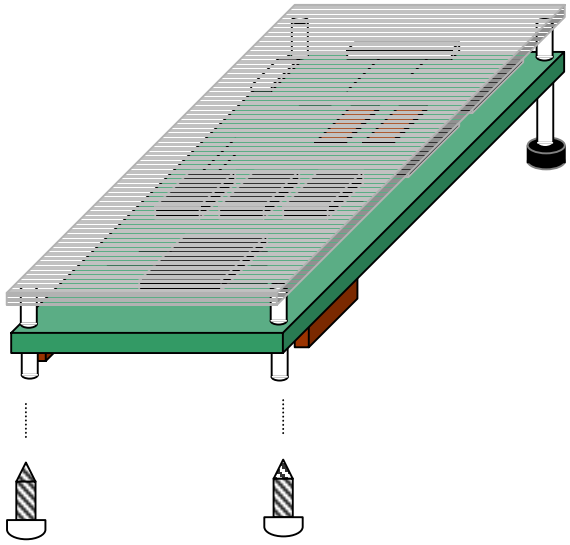
Connect the probe or the ribbon cables to the respective connectors on the LCE-780308-EM.



3.2. Connect LCE-780308-EM to LCE-78K0

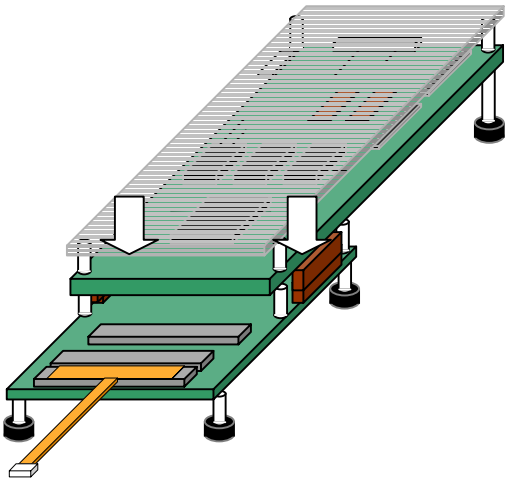
Turn off the power from the LCE-78K0 motherboard. Remove the AC power adapter from the J1 power input on the LCE-78K0 motherboard.

At the end of the LCE-78K0 with the J3 and J4 connectors, remove the two screws at the bottom of the stand-offs as shown.



With the LCE-780xxx-EM daughter board on a stable surface, connect the motherboard to the daughter board by gently applying pressure on the mating connectors. Avoid applying pressure on the plastic cover. You should feel and hear the connectors on the motherboard and daughter board snap together.

Apply pressure on the motherboard



For a secure connection, replace the screws, threading them up through the daughter board into the spacers on the motherboard.

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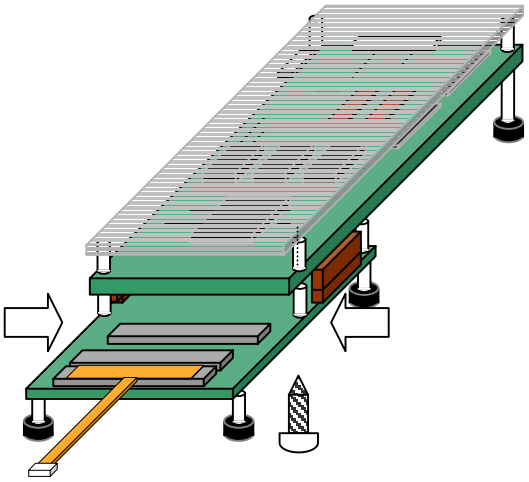


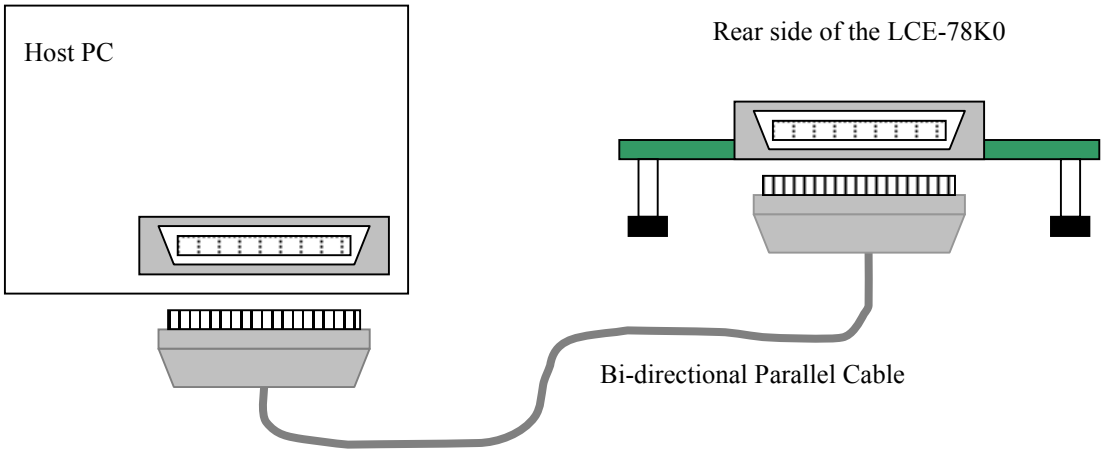
3.3. Connect Probe Cables to User Target

Make sure that power for the user target is off. Connect the other end of the probe or ribbon cable to the user target. Refer to Chapter 4 for pin assignments for both connectors.

Reconnect the AC power adapter to the LCE-78K0.

3.4. Connect LCE-K0 System to Host Computer

Connect the LCE-K0 system to the host computer with a 25-pin male-to-male parallel cable included with the motherboard.



3.5. Power-On Sequence

When applying power to the systems connected above, follow the sequence below.

1) Turn on the host computer system.

2) Turn the power switch on the LCE-78K0 motherboard to the ON position. This will cause the green LED to turn on indicating power is being supplied to the system.

3) Turn on power to the user target system.

4) Run the ID78K0-LCE debugger on the host PC.

3.6. Power-Off Sequence and Disconnect

When turning power off and disconnecting, follow the reverse sequence:

1) Turn power off to the user target system.

2) Turn the power switch on the LCE-78K0 motherboard off.

3) Disconnect the LCE-K0 system from the host PC.

4) Disconnect the AC adapter from the LCE-K0 system.

5) Disconnect the LCE-K0 system from the user target.

CHAPTER 4 CONNECTOR PIN ASSIGNMENTS

4.1. J3-J4 Probe 100 Ribbon Cable Pin Assignments

J3 Pin	Target Pin (100GC)	Target Pin (100GF)	Target Signal	J4 Pin	Target Pin (100GC)	Target Pin (100GF)	Target Signal
1	80	8	X1	1	85	13	P00
2	82	9	XT1/P07	2	86	14	P01
3	23	51	COM0	3	87	15	P02
4	84	12	RESET	4	88	16	P03
5	24	52	COM1	5	89	17	P04
6	9	37	AVREF	6	90	18	P05
7	71	99	P80/S39	7			**Note 1**
8	70	98	P81/S38	8			**Note 1**
9	69	97	P82/S37	9	8	36	VDD0 **Note 4**
10	68	96	P83/S36	10	82	10	VDD1 **Note 4**
11	67	95	P84/S35	11	91	19	P110
12	66	94	P85/S34	12	92	20	P111
13	65	93	P86/S33	13	93	21	P112
14	64	92	P87/S32	14	94	22	P113
15	25	53	COM2	15	95	23	P114
16	26	54	COM3	16	96	24	P115
17	32	60	S0	17	97	25	P116
18	33	61	S1	18	98	26	P117
19	34	62	S2	19	15	43	P30
20	35	63	S3	20	16	44	P31
21	36	64	S4	21	17	45	P32
22	37	65	S5	22	18	46	P33
23	38	66	S6	23	19	47	P34
24	39	67	S7	24	20	48	P35
25	40	68	S8	25	21	49	P36
26	41	69	S9	26	22	50	P37
27	42	70	S10	27	72	100	P25
28	43	71	S11	28	74	2	P27
29	44	72	S12	29	73	1	P26
30	45	73	S13	30	75	3	P70
31	46	74	S14	31	76	4	P71
32	47	75	S15	32	77	5	P72
33	48	76	S16	33	63	91	P90/S31
34	49	77	S17	34	62	90	P91/S30
35	50	78	S18	35	61	89	P92/S29
36	51	79	S19	36	60	88	P93/S28
37	52	80	S20	37	59	87	P94/S27
38	53	81	S21	38	58	86	P95/S26
39	54	82	S22	39	57	85	P96/S25
40	55	83	S23	40	56	84	P97/S24
41	13	41	P102	41	100	28	P10
42	11	39	P101	42	1	29	P11
43	10	38	P100	43	2	30	P12
44	14	42	P103	44	3	31	P13
45	28	56	VLC0	45	4	32	P14
46	29	57	VLC1	46	5	33	P15

J3 Pin	Target Pin (100GC)	Target Pin (100GF)	Target Signal	J4 Pin	Target Pin (100GC)	Target Pin (100GF)	Target Signal
47	30	58	VLC2	47	6	34	P16
48	27	55	BIAS	48	7	35	P17
49	99	27	AVSS	49	31	59	VSS0 **Note 2**
50	78	6	IC **Note 2**	50	12	40	VSS1 **Note 2**

Note 1: P4 pins 7 and 8 carry signals not used for 100-pin devices; do not connect to target
Note 2: VSS0, VSS1 and IC on the target pins are connected to GND on the LCE-780308-EM
Note 3: X2 and XT2 on the target are not connected on the LCE-780308-EM
Note 4: VDD0 and VDD1 on the target are both connected to UVDD on the LCE-780308-EM; this signal is used for sensing target voltage, but does not supply power to the target.

4.2. J4-J5 Probe 80 Ribbon Cable Pin Assignments

J4 Pin	Target Pin (GC/GK)	Target Signal	J5 Pin	Target Pin (GC/GK)	Target Signal
1	61	P00	1	70	X1
2	62	P01	2	73	XT1/P07
3	63	P02	3	4	AVSS
4	64	P03	4	60	RESET
5	65	P04	5	75	AVREF0
6	66	P05	6	7	AVREF1
7	67	P06	7	11	P20
8	74	AVDD	8	12	P21
9	68 *	VDD **Note 4**	9	13	P22
10	68 *	VDD **Note 4**	10		n.c.
11		**Note 1**	11		n.c.
12		**Note 1**	12		n.c.
13		**Note 1**	13	19	P40/AD0
14	14	P23	14	20	P41/AD1
15	15	P24	15	21	P42/AD2
16		**Note 1**	16	22	P43/AD3
17		**Note 1**	17	23	P44/AD4
18		**Note 1**	18	24	P45/AD5
19	44	P30	19	25	P46/AD6
20	45	P31	20	26	P47/AD7
21	46	P32	21	36	P60
22	47	P33	22	37	P61
23	48	P34	23	38	P62
24	49	P35	24	39	P63
25	50	P36	25	40	P64/RD
26	51	P37	26	41	P65/WR
27	16	P25	27	42	P66/WAIT
28	18	P27	28	43	P67/ASTB
29	17	P26	29		n.c.
30	8	P70	30		n.c.
31	9	P71	31	52	P120
32	10	P72	32	53	P121
33		**Note 1**	33	54	P122
34		**Note 1**	34	55	P123
35		**Note 1**	35	56	P124
36		**Note 1**	36	57	P125
37		**Note 1**	37	58	P126
38		**Note 1**	38	59	P127
39		**Note 1**	39	5	P130/ANO0
40		**Note 1**	40	6	P131/ANO1
41	76	P10/ANI0	41	27	P50/A8
42	77	P11/ANI1	42	28	P51/A9
43	78	P12/ANI2	43	29	P52/A10
44	79	P13/ANI3	44	30	P53/A11
45	80	P14/ANI4	45	31	P54/A12
46	1	P15/ANI5	46	32	P55/A13

J4 Pin	Target Pin (GC/GK)	Target Signal	J5 Pin	Target Pin (GC/GK)	Target Signal
47	2	P16/ANI6	47	34	P56/A14
48	3	P17/ANI7	48	35	P57/A15
49	33	VSS **Note 2**	49		GND **Note 6**
50	71	IC **Note 2**	50		GND **Note 6**

Note 1: P4 pins marked "**Note 1**" carry signals not used for 80-pin devices; do not connect to target
Note 2: VSS and IC on the target pins are connected to GND on the LCE-780308-EM
Note 3: X2 and XT2 on the target are not connected on the LCE-780308-EM
Note 4: VDD on the target is connected to UVDD on the LCE-780308-EM on both P4 pin 9 and P4 pin 10; this signal is used for sensing target voltage, but does not supply power to the target.
Note 5: J5 pins marked "n.c." are not connected
Note 6: J5 pins marked "GND" are connected to GND on the LCE-780308-EM

4.3. J1 Probe 100 Pin Assignments, NP-100GC

Target Pin (100GC)	J1 Pin Number	Target Pin (100GC)	J1 Pin Number
1	118	51	4
2	117	52	3
3	114	53	8
4	113	54	7
5	108	55	14
6	107	56	13
7	104	57	18
8	103	58	17
9	100	59	22
10	99	60	21
11	94	61	28
12	93	62	27
13	30	63	92
14	29	64	91
15	24	65	98
16	23	66	97
17	20	67	102
18	19	68	101
19	16	69	106
20	15	70	105
21	10	71	112
22	9	72	111
23	6	73	116
24	5	74	115
25	33	75	87
26	34	76	88
27	37	77	83
28	38	78	84
29	43	79	77
30	44	80	78
31	47	81	73
32	48	82	74
33	51	83	69
34	52	84	70
35	57	85	63
36	58	86	64
37	59	87	61
38	60	88	62
39	55	89	65
40	56	90	66
41	49	91	71
42	50	92	72
43	45	93	75
44	46	94	76
45	41	95	79

Target Pin (100GC)	J1 Pin Number	Target Pin (100GC)	J1 Pin Number
46	42	96	80
47	35	97	85
48	36	98	86
49	31	99	89
50	32	100	90

4.4. J1 Probe 100 Pin Assignments, NP-100GF

Target Pin (100GF)	J1 Pin Number	Target Pin (100GF)	J1 Pin Number
1	116	51	6
2	115	52	5
3	87	53	33
4	88	54	34
5	83	55	37
6	84	56	38
7	77	57	43
8	78	58	44
9	73	59	47
10	74	60	48
11	69	61	51
12	70	62	52
13	63	63	57
14	64	64	58
15	61	65	59
16	62	66	60
17	65	67	55
18	66	68	56
19	71	69	49
20	72	70	50
21	75	71	45
22	76	72	46
23	79	73	41
24	80	74	42
25	85	75	35
26	86	76	36
27	89	77	31
28	90	78	32
29	118	79	4
30	117	80	3
31	114	81	8
32	113	82	7
33	108	83	14
34	107	84	13
35	104	85	18
36	103	86	17
37	100	87	22
38	99	88	21
39	94	89	28
40	93	90	27
41	30	91	92
42	29	92	91
43	24	93	98
44	23	94	97

Target Pin (100GF)	J1 Pin Number	Target Pin (100GF)	J1 Pin Number
45	20	95	102
46	19	96	101
47	16	97	106
48	15	98	105
49	10	99	112
50	9	100	111

4.5. J2 Probe 80 Pin Assignments, NP-80GC and NP-80GK

Target Pin Number	J2 Pin Number	Target Pin Number	J2 Pin Number
1	114	41	8
2	113	42	7
3	108	43	14
4	107	44	13
5	104	45	18
6	103	46	17
7	100	47	22
8	99	48	21
9	94	49	28
10	93	50	27
11	30	51	92
12	29	52	91
13	24	53	98
14	23	54	97
15	20	55	102
16	19	56	101
17	16	57	106
18	15	58	105
19	10	59	112
20	9	60	111
21	37	61	83
22	43	62	77
23	44	63	78
24	47	64	73
25	48	65	74
26	51	66	69
27	52	67	70
28	57	68	63
29	58	69	64
30	59	70	61
31	60	71	62
32	55	72	65
33	56	73	66
34	49	74	71
35	50	75	72
36	45	76	75
37	46	77	76
38	41	78	79
39	42	79	80
40	35	80	85