# AVR<sup>®</sup> JTAGICE mkli

**AV***R*<sup>°</sup>

# **DEBUG AVR APPLICATIONS USING** JTAG OR DEBUGWIRE INTERFACE

The AVR® JTAGICE mkll from Atmel® is a powerful development tool for On-chip Debugging of all AVR 8-bit RISC microcontrollers with IEEE 1149.1 compliant JTAG interface or debugWIRE Interface. DebugWIRE enables on chip debug of AVR microcontrollers in small pin count packages, using only a single wire for the

debug interface. The JTAGICE mkII and the AVR Studio® user interface give the user complete control of the internal resources of the microcontroller, helping to reduce development time by making debugging easier. The JTAGICE mkll performs Real Time emulation of the microcontroller while it is running in a target system. The JTAGICE mkll provides emulation capability at a fraction of the cost of traditional emulators.



- AVR Studio Operated
- Full Emulation of All Analog and Digital All Operations and Breakpoints are Functions
- Full JTAG Programming Support
- Supports Multiple Devices in a JTAG Scan Chain
- USB 1.1 or RS-232 Interface to PC
- Full Support for Assembly and High Supply Voltage 9V 12V, or Powered Level Languages

- Program and Data Breakpoints
- **Real Time**
- Adapter for Direct Connection to **STK500**
- Upgrades are done from AVR Studio
- Target Voltage 1.8 5.5V
- from USB port

Debug

System

MICROCONTROLLERS

# JTAGICE MKII AVR ON-CHIP DEBUG SYSTEM

#### **Corporate Headquarters**

2325 Orchard Parkway San Jose, CA 95131 USA TEL: (1)(408) 441-0311 FAX: (1)(408) 487-2600

### Europe

Atmel Sarl Route des Arsenaux 41 Case Postale 80 CH-1705 Fribourg Switzerland TEL: (41) 26-426-5555 FAX: (41) 26-426-5500

# Asia

Room 1219 Chinachem Golden Plaza 77 Mody Road Tsimshatsui East Kowloon Hong Kong TEL: (852) 2721-9778 FAX: (852) 2722-1369

#### Japan

9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 Japan TEL: (81) 3-3523-3551 FAX: (81) 3-3523-7581

Web Site

http://www.atmel.com

The JTAGICE mkll allows access to all the powerful features of the AVR microcontroller. All AVR resources can be monitored: Flash memory, EEPROM memory, SRAM memory, Register File, Program Counter, Fuse and Lock Bits, and all I/O modules. The JTAGICE mkll also offers extensive On-chip Debug support for break conditions, including break on change of Program memory flow, Program memory Break Points on single address or address range, and Data memory Break Points on single address or address range.

The debugWIRE uses the Reset line for electrical connection; hence the system designer does not have to sacrifice I/O capabilities to take full advantage of the On-Chip-Debug system.

The JTAGICE mkll will automatically be upgraded by future AVR Studio releases to support future devices with JTAG and debugWIRE support as they are released.

The JTAGICE mkll interface is integrated in AVR Studio, Atmel's front-end tool for development on the AVR architecture. All phases of the AVR development can be done in this Integrated Development Environment.

# Supported Devices

JTAG	
ATmega16	ATmega6490
ATmega162	ATmega128
ATmega169	ATmega1281
ATmega32	ATmega1280
ATmega329	ATmega128CAN11
ATmega3290	ATmega256
ATmega64	ATmega2560
ATmega649	

ATtiny13 ATtiny2313 ATtiny25 ATtiny45 ATmega48 ATmega88 ATmega168

Note: Low voltage devices are also supported.

# Ordering Information

The JTAGICE is available from Atmel franchised distributors.

## The ordering code is **ATJTAGICE2**

The latest version of AVR Studio is available free of charge from Atmel web site: www.atmel.com The JTAGICE will automatically be upgraded by future AVR Studio releases to support future devices with JTAG support as they are released.



Atmel Corporation 2004. All rights reserved. Atmel<sup>®</sup> and combinations thereof, AVR<sup>®</sup>, AVR Studio<sup>®</sup>, are registered trademarks of Atmel. Other terms and product names may be trademarks of others.

2489D-AVR-02/04/0M