XC-3 Hardware Manual

Version 1.3

XMOS™

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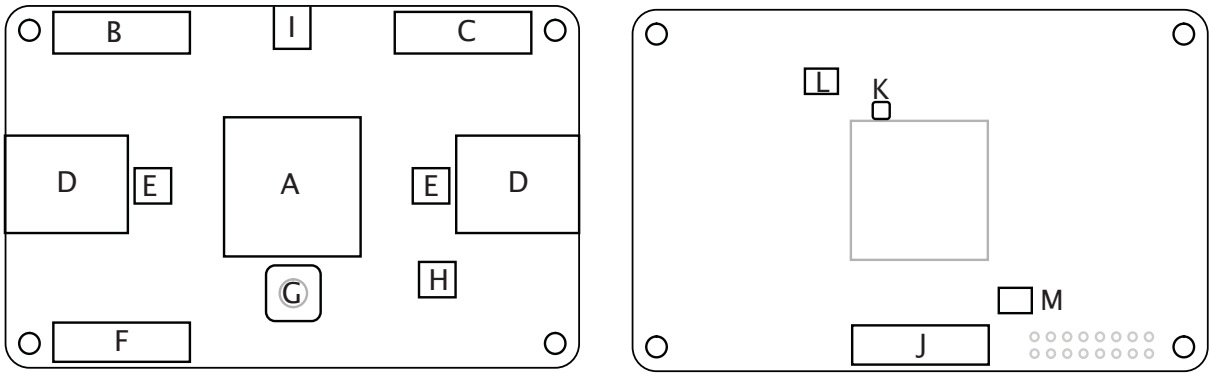
1 Introduction

The XC-3 is an Event-Driven Processor development board that can be used as a LED tile controller. It comprises a single XS1-G4 device, two LED module connectors, two 10/100-BASE-T Ethernet transceiver units, 4Mbits SPI flash memory, one press-button. A GPIO header is provided for connecting additional components, and an XSYS connector can be used to interface the card with a PC. The diagram below shows the layout of these components on the card:



A XS1-G4 Device

B LED In Connector

C LED Out Connector

D RJ45 Connector

E 10/100M Ethernet Transceiver

F I/O Expansion Header

G Reset Button

H SPI Flash Memory

I Power Connector

J XSYS Connector

K Power Regulator

L 20MHz Crystal Oscillator (XCore™)

M 25MHz Crystal Oscillator (Transceiver)

The XC-3 Development Kit also includes a power supply and XTAG connector for booting the device from a PC. The card is fitted with four plastic feet, which can be removed to provide access to mounting holes for product integration.

The following sections in this document provide a detailed description of these components.

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2 XS1-G4 Device [A]

The XC-3 provides a single four-core XS1-G4 device in a 144BGA package. Each XCore is programmable and comprises an event-driven multi-threaded processor with tightly integrated general purpose I/O and 64 KBytes of on-chip RAM. The I/O pins for XCore0 and XCore2 are brought out of the package and connected to the card's components as follows:

Processor 0

- Two LED module connectors
- One SPI interface to flash memory
- One 16-way I/O expansion header

Processor 2

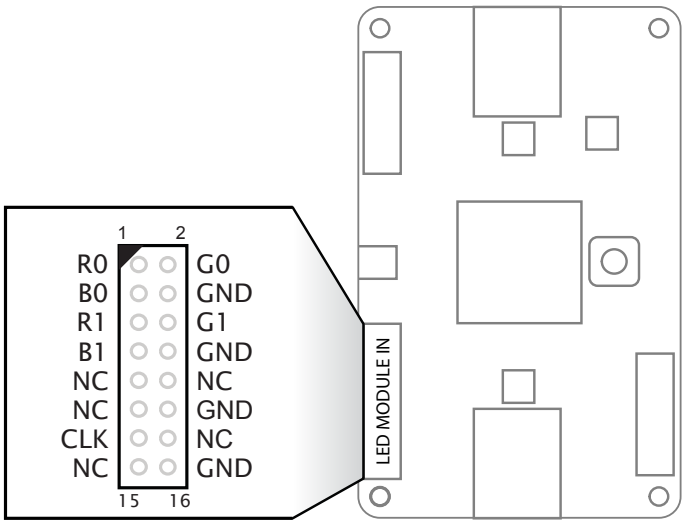
- Two 10/100-BASE-T Ethernet Transceivers

The XSYS Connector and Reset Button are tied to the global system I/O pins.

The processors have ports that are directly connected to the I/O pins.

3 LED Module In [B]

The I/O pins of processor 0 have been brought out to a LED Module Input connector that can be used to connect to a 16-way 2mm IDC connector.



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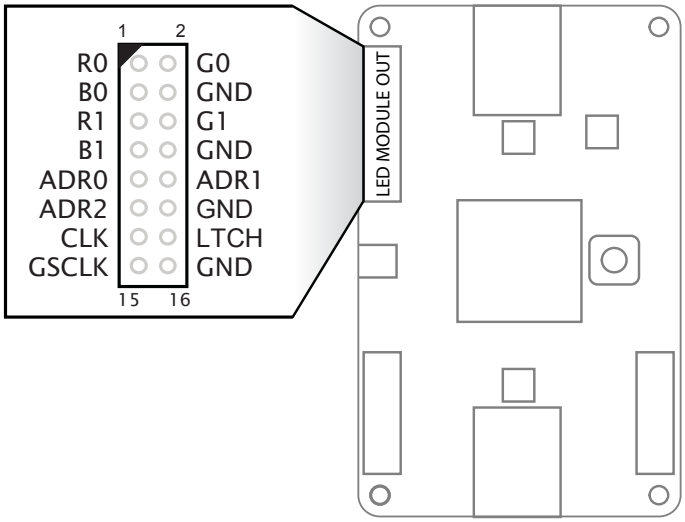
The connector provides a bank of seven I/O pins, which are mapped to the ports as described in the table below:

Pin	Port		Processor
	1b	8b	0
X0D12	P1E0		PORT_LED_IN_CLK
X0D14		P8B0	PORT_LED_IN [R0]
X0D15		P8B1	PORT_LED_IN [G0]
X0D16		P8B2	PORT_LED_IN [B0]
X0D17		P8B3	PORT_LED_IN [R1]
X0D18		P8B4	PORT_LED_IN [G1]
X0D19		P8B5	PORT_LED_IN [B1]

4 LED Module Out [C]

The I/O pins of processor 0 have been brought out to a LED Module Out connector that can be used to connect to a 16-way 2mm IDC connector.



The connector provides a bank of 12 I/O pins, which are mapped to the ports as described in the table on the next page:

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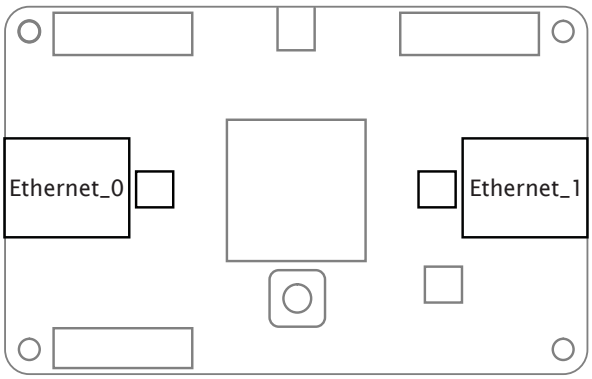
Pin	Port		Processor
	1b	4b	0
X0D2		P4A0	PORT_LED_OUT_ADDR [0]
X0D3		P4A1	PORT_LED_OUT_ADDR [1]
X0D8		P4A2	PORT_LED_OUT_ADDR [2]
X0D13	P1F0		PORT_LED_OUT_R0
X0D22	P1G0		PORT_LED_OUT_G0
X0D23	P1H0		PORT_LED_OUT_B0
X0D24	P1I0		PORT_LED_OUT_R1
X0D25	P1J0		PORT_LED_OUT_G1
X0D34	P1K0		PORT_LED_OUT_B1
X0D35	P1L0		PORT_LED_OUT_CLK
X0D36	P1M0		PORT_LED_OUT_LATCH
X0D37	P1N0		LED_OUT_OE

5 RJ45 [D] and Ethernet Transceiver [E]

The RJ45 connectors are wired to the 10/100-BASE-T Ethernet Transceivers. The MII and MAC level protocols are implemented in software.



The I/O pins on the ethernet PHY are mapped to the ports as described in the table on the following page:

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Pin	Port		Processor
	1b	4b	0
X2D0	P1A0		PORT_ETH_RXCLK_0
X2D1	P1B0		PORT_ETH_RXER_0
X2D10	P1C0		PORT_ETH_TXCLK_0
X2D11	P1D0		PORT_ETH_RXDV_0
X2D12	P1E0		PORT_ETH_TXEN_0
X2D14		P4C0	PORT_ETH_RXD_0 [0:1]
X2D15		P4C1	
X2D16		P4D0	PORT_ETH_TXD_0
X2D17		P4D1	
X2D18		P4D2	
X2D19		P4D3	
X2D20		P4C2	PORT_ETH_RXD_0 [2:3]
X2D21		P4C3	
X2D22	P1G0		PORT_ETH_MDIO_0
X2D23	P1H0		PORT_ETH_RST_N
X2D24	P1I0		PORT_ETH_MDC_0
X2D25	P1J0		PORT_ETH_RXCLK_1
X2D26		P4E0	PORT_ETH_RXD_1 [0:1]
X2D27		P4E1	
X2D28		P4F0	PORT_ETH_TXD_1
X2D29		P4F1	
X2D30		P4F2	
X2D31		P4F3	
X2D32		P4E2	PORT_ETH_RXD_1 [2:3]
X2D33		P4E3	
X2D34	P1K0		PORT_ETH_RXDV_1
X2D35	P1L0		PORT_ETH_RXER_1
X2D36	P1M0		PORT_ETH_TXCLK_1
X2D37	P1N0		PORT_ETH_TXEN_1
X2D38	P1O0		PORT_ETH_MDC_1
X2D39	P1P0		PORT_ETH_MDIO_1

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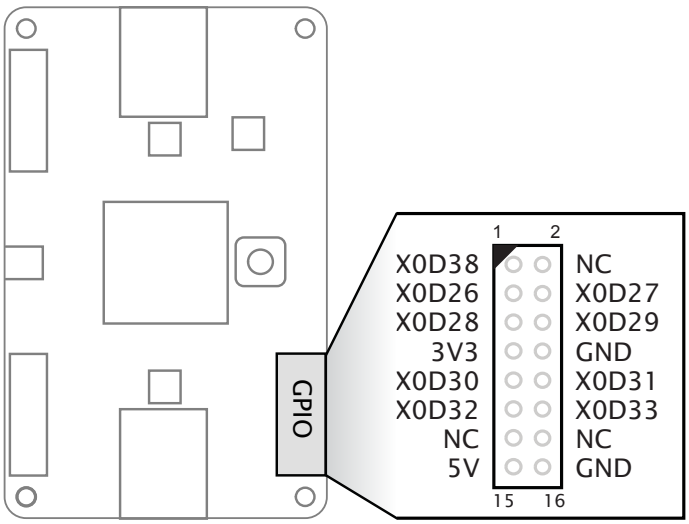
6 I/O Expansion Header [F]

The I/O pins of processor 0 are brought out to a general purpose I/O expansion area on one side of the card. The area has 0.1" pitch through-plated holes and is suitable for use with IDC headers. To provide maximum flexibility, no headers are fitted, allowing the most suitable type to be selected depending on the design. The routing of the I/O and power pins in the expansion header is shown below:



The expansion header provides a bank of nine I/O pins, which are mapped to the ports as described in the table below:

Pin	Port			Processor
	1b	4b	8b	0
X0D26		P4E0	P8C0	GPIO
X0D27		P4E1	P8C1	
X0D28		P4F0	P8C2	
X0D29		P4F1	P8C3	
X0D30		P4F2	P8C4	
X0D31		P4F3	P8C5	
X0D32		P4E2	P8C6	
X0D33		P4E3	P8C7	
X0D38	P1O0			PORT_GPIO_CLK

The pins from the bank can be configured as either two 4-bit ports or a single 8-bit port.

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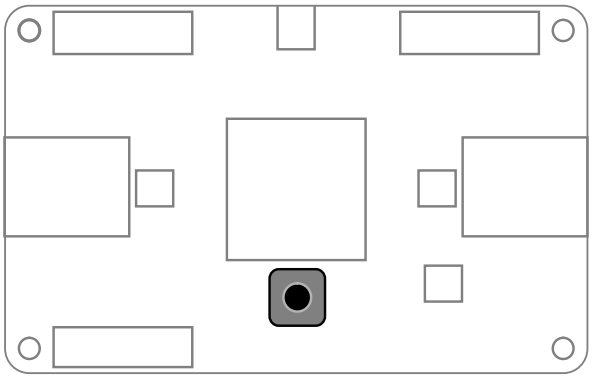
7 Push-Button Switch [G]

The XC-3 provides a hardware reset button which is tied to the global system I/O pins. The layout of the button is shown below:



8 Power Connector [I] and Regulator [K]

The XC-3 requires connection from an external 5V power supply. The voltage is converted by the on-board regulator to the 1V and 3V3 supplies used by the components.

9 XSYS Connector [J]

The XC-3 includes an XSYS connector, which can be used to boot and debug code on all of the XS1-G4's processors. The XSYS connector is tied to global system I/O pins that provide JTAG control, system reset, processor debug, bidirectional UART and one XMOS Link. The routing of these I/O pins along with the power pins is shown on the following page:

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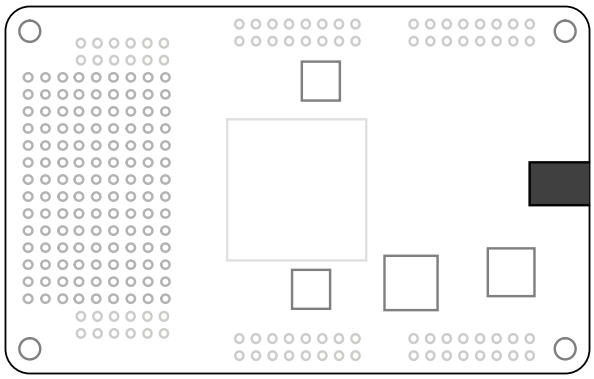

The XMOS XTAG connector converts between XSYS and USB 2.0, allowing the XC-3 to be connected to most PCs. On power on, the XS1-G4 boots from the on-board flash memory. The XS1-G4 can then be put into JTAG mode by the PC, which then boots another program.

No UART hardware is provided. Instead, two UART pins are mapped to ports, as shown in the table below:

Pin	Port		Processor
	1b	4b	0
X0D4		P4B0	PORT_UART_TX
X0D39	P1P0		PORT_UART_RX

If a UART is required, it can be implemented in software by sampling and driving these ports at the required rate. The XTAG performs a UART-to-USB conversion on these pins, presenting a virtual COM port to the PC that can be interfaced via a terminal emulator.

10 SPI Flash Memory [H]

The XC-3 provides 4Mbit of Serial Peripheral Interface (SPI) flash memory, which is interfaced by the four 1-bit connections described in the table below:

Pin	Port	Processor
	1b	0
X0D0	P1A0	PORT_SPI_MISO
X0D1	P1B0	PORT_SPI_SS
X0D10	P1C0	PORT_SPI_CLK
X0D11	P1D0	PORT_SPI_MOSI

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The XMOS Development Tools include the XFLASH utility for programming compiled programs into the flash memory. XC-3 designs may also access the flash memory at run-time by interfacing with the above ports.

11 Crystal Oscillator [L and M]

The XS1-G4 is clocked at 20MHz by a crystal oscillator on the card. Each processor is clocked at 400MHz, the I/O ports at 100MHz, by an on-chip phase-locked loop (PLL).

The two Ethernet Transceivers are clocked at 25MHz by a crystal oscillator on the card.

12 Dimensions

The XC-3 dimensions are 86 x 54mm. The mounting holes are 3mm in diameter.

13 I/O Port-to-Pin Mapping

The diagram on the next page shows how the XC-3 components are connected to the XS1-G4:

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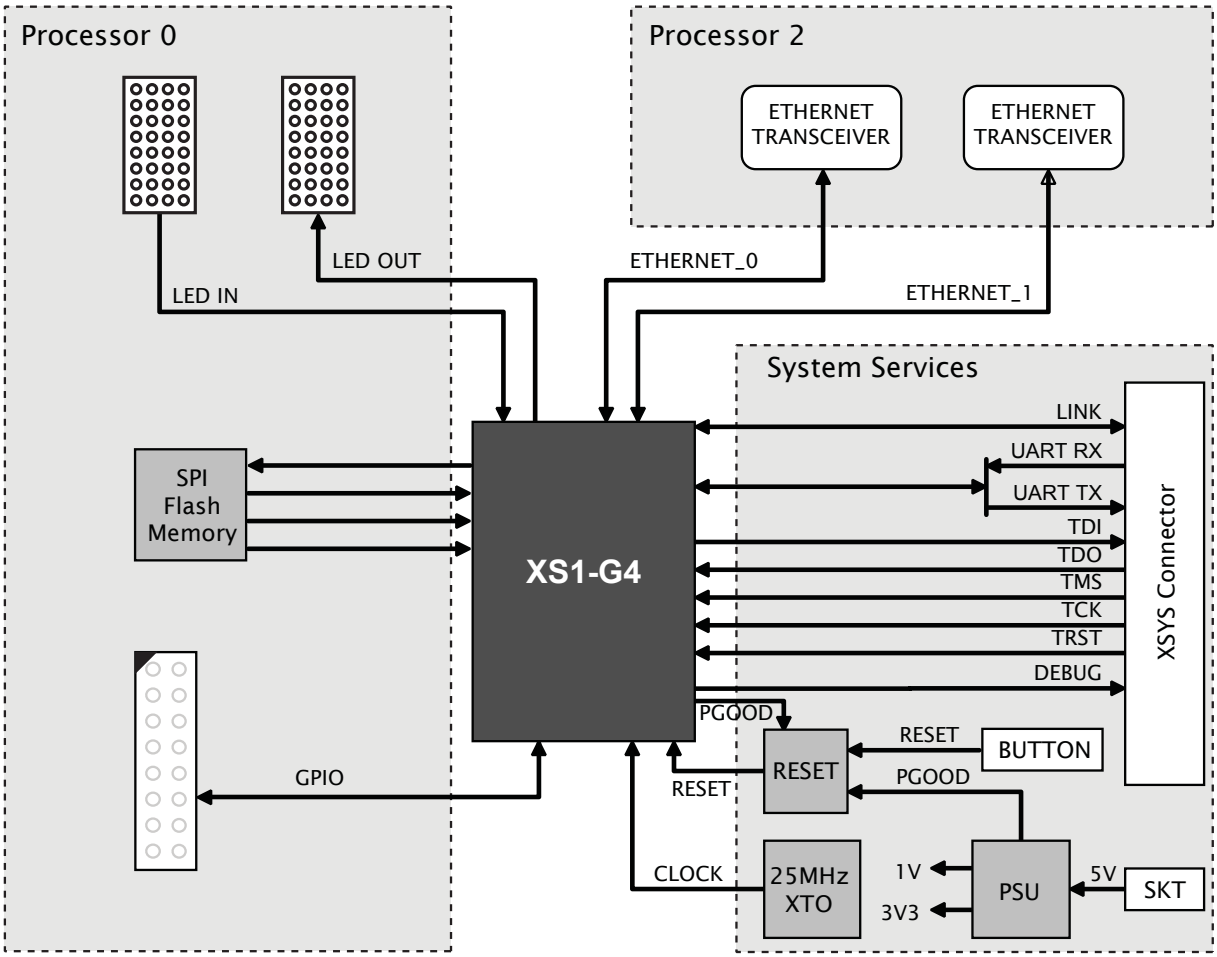

The table on the following page provides a full description of the port-to-pin mappings described throughout this document:

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Pin	Port				Processor	
	1b	4b	8b	16b	0	2
X*n*D0	P1A0				PORT_SPI_MISO	PORT_ETH_RXCLK_0
X*n*D1	P1B0				PORT_SPI_SS	PORT_ETH_RXER_0
X*n*D2		P4A0	P8A0	P16A0	PORT_LED_OUT_ADDR [0:1]	
X*n*D3		P4A1	P8A1	P16A1		
X*n*D4		P4B0	P8A2	P16A2	PORT_UART_TX	
X*n*D5		P4B1	P8A3	P16A3		
X*n*D6		P4B2	P8A4	P16A4		
X*n*D7		P4B3	P8A5	P16A5		
X*n*D8		P4A2	P8A6	P16A6	PORT_LED_OUT_ADDR [2]	
X*n*D9		P4A3	P8A7	P16A7		
X*n*D10	P1C0				PORT_SPI_CLK	PORT_ETH_TXCLK_0
X*n*D11	P1D0				PORT_SPI_MOSI	PORT_ETH_RXDV_0
X*n*D12	P1E0				PORT_LED_IN_CLK	PORT_ETH_TXEN_0
X*n*D13	P1F0				PORT_LED_OUT_R0	
X*n*D14		P4C0	P8B0	P16A8	PORT_LED_IN_R0	PORT_ETH_RXD_0 [0:1]
X*n*D15		P4C1	P8B1	P16A9	PORT_LED_IN_G0	
X*n*D16		P4D0	P8B2	P16A10	PORT_LED_IN_B0	PORT_ETH_TXD_0
X*n*D17		P4D1	P8B3	P16A11	PORT_LED_IN_R1	
X*n*D18		P4D2	P8B4	P16A12	PORT_LED_IN_G1	
X*n*D19		P4D3	P8B5	P16A13	PORT_LED_IN_B1	
X*n*D20		P4C2	P8B6	P16A14		PORT_ETH_RXD_0 [2:3]
X*n*D21		P4C3	P8B7	P16A15		
X*n*D22	P1G0				PORT_LED_OUT_G0	PORT_ETH_MDIO_0
X*n*D23	P1H0				PORT_LED_OUT_B0	PORT_ETH_RST_N
X*n*D24	P1I0				PORT_LED_OUT_R1	PORT_ETH_MDC_0
X*n*D25	P1J0				PORT_LED_OUT_G1	PORT_ETH_RXCLK_1
X*n*D26		P4E0	P8C0	P16B0	GPIO	PORT_ETH_RXD_1 [0:1]
X*n*D27		P4E1	P8C1	P16B1		
X*n*D28		P4F0	P8C2	P16B2		PORT_ETH_TXD_1 [0:3]
X*n*D29		P4F1	P8C3	P16B3		
X*n*D30		P4F2	P8C4	P16B4		
X*n*D31		P4F3	P8C5	P16B5		
X*n*D32		P4E2	P8C6	P16B6		PORT_ETH_RXD_1 [2:3]
X*n*D33		P4E3	P8C7	P16B7		
X*n*D34	P1K0				PORT_LED_OUT_B1	PORT_ETH_RXDV_1
X*n*D35	P1L0				PORT_LED_OUT_CLK	PORT_ETH_RXER_1
X*n*D36	P1M0		P8D0	P16B8	PORT_LED_OUT_LATCH	PORT_ETH_TXCLK_1
X*n*D37	P1N0		P8D1	P16B9	PORT_LED_OUT_OE	PORT_ETH_TXEN_1
X*n*D38	P1O0		P8D2	P16B10	PORT_GPIO_CLK	PORT_ETH_MDC_1
X*n*D39	P1P0		P8D3	P16B11	PORT_UART_RX	PORT_ETH_MDIO_1
X*n*D40			P8D4	P16B12		
X*n*D41			P8D5	P16B13		
X*n*D42			P8D6	P16B14		
X*n*D43			P8D7	P16B15		

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14 XC-3 XN File

The XCore ports linked to the hardware features on the XC-3 are mapped to generic port identifiers as part of a platform specific XN file.

The following table lists the defined identifiers for processors 0 and 2:

Processor	Port Location	Generic Identifier
0	XS1_PORT_1A	PORT_SPI_MISO
	XS1_PORT_1B	PORT_SPI_SS
	XS1_PORT_1C	PORT_SPI_CLK
	XS1_PORT_1D	PORT_SPI_MOSI
	XS1_PORT_1E	PORT_LED_IN_CLK
	XS1_PORT_1F	PORT_LED_OUT_R0
	XS1_PORT_1G	PORT_LED_OUT_G0
	XS1_PORT_1H	PORT_LED_OUT_B0
	XS1_PORT_1I	PORT_LED_OUT_R1
	XS1_PORT_1J	PORT_LED_OUT_G1
	XS1_PORT_1K	PORT_LED_OUT_B1
	XS1_PORT_1L	PORT_LED_OUT_CLK
	XS1_PORT_1M	PORT_LED_OUT_LATCH
	XS1_PORT_1N	PORT_LED_OUT_OE
	XS1_PORT_1O	PORT_GPIO_CLK
	XS1_PORT_1P	PORT_UART_RX
	XS1_PORT_4A	PORT_LED_OUT_ADDR
	XS1_PORT_4B	PORT_UART_TX
	XS1_PORT_8B	PORT_LED_IN
2	XS1_PORT_1A	PORT_ETH_RXCLK_0
	XS1_PORT_1B	PORT_ETH_RXER_0
	XS1_PORT_1C	PORT_ETH_TXCLK_0
	XS1_PORT_1D	PORT_ETH_RXDV_0
	XS1_PORT_1E	PORT_ETH_TXEN_0
	XS1_PORT_1G	PORT_ETH_MDIO_0
	XS1_PORT_1G	PORT_ETH_RST_N
	XS1_PORT_1I	PORT_ETH_MDC_0
	XS1_PORT_1J	PORT_ETH_RXCLK_1
	XS1_PORT_1K	PORT_ETH_RXDV_1
	XS1_PORT_1L	PORT_ETH_RXER_1
	XS1_PORT_1M	PORT_ETH_TXCLK_1
	XS1_PORT_1N	PORT_ETH_TXEN_1
	XS1_PORT_1O	PORT_ETH_MDC_1
	XS1_PORT_1P	PORT_ETH_MDIO_1
	XS1_PORT_4C	PORT_ETH_RXD_0
	XS1_PORT_4D	PORT_ETH_TXD_0
	XS1_PORT_4E	PORT_ETH_RXD_1
	XS1_PORT_4F	PORT_ETH_TXD_1

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15 Related Documents

The following documents provide more information on designing with the XC-3:

- *XCore XS1 Architecture Tutorial* [1]: provides an overview of the XS1 instruction set architecture.

The most up-to-date information on the XC-3, including board schematics and product datasheets, is available from:

- `http://www.xmos.com/xc3/`

Bibliography

[1] David May and Henk Muller. XCore XS1 Architecture Tutorial. Website, 2009. http://www.xmos.com/published/xs1tut.

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