
EDK3069

USER MANUAL

FOR H8/3069

ON-CHIP FLASH MICROCONTROLLER

Preface

Cautions

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2. START-UP INSTRUCTIONS

2.1. INSTALLING THE EVALUATION DEVELOPMENT KIT (EDK)

Please refer to the quick start guide provided for initial installation of the EDK.

A copy of the quick start guide and other information relating to this EDK at:

<http://www.hmse.com/products/support.htm>

Installing the EDK requires power and serial connection to a host computer.

2.2. SERIAL CONNECTION

The serial communications cable for connecting the EDK to a host computer is supplied. The serial cable has 1:1 connectivity.

Figure 2-1 shows how to connect the EDK to a PC or notebook computer equipped with a nine pin D connector.

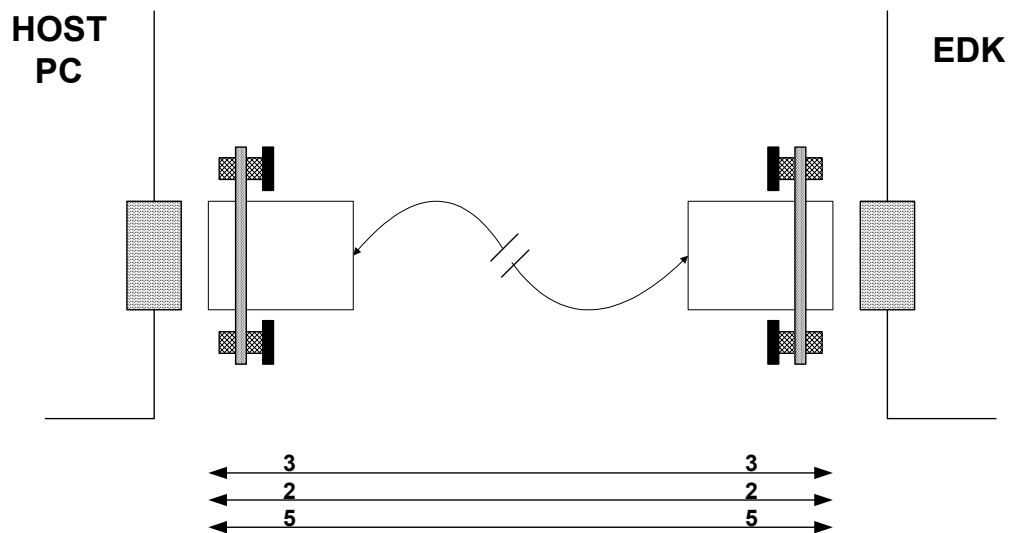


FIGURE 2-1: SERIAL CONNECTION TO PC/NOTEBOOK WITH DB-9 CONNECTOR (SUPPLIED)

2.3. POWER SUPPLY

The EDK hardware requires a power supply of +5V. Since total power consumption can vary widely due to external connections, port states, and memory configuration, use a power supply capable of providing at least 500mA at +5V DC \pm 5%.

The design is specified for evaluation of the microcontroller and so does not include circuitry for supply filtering/noise reduction, under voltage protection, over current protection or reversed polarity protection. Caution should be used when selecting and using a power supply.

The power connector on the EDK is a 2.5mm Barrel connector. The center pin is the positive connection.



FIGURE 2-2: POWER SUPPLY CONNECTION

Caution: Existing customers using E6000 products note that the polarity of this board is opposite to that for the E6000. Use of the E6000 power supply with this board will damage both board and power supply.

3. EDK BOARD LAYOUT

The diagram shows a general layout of the EDK board.

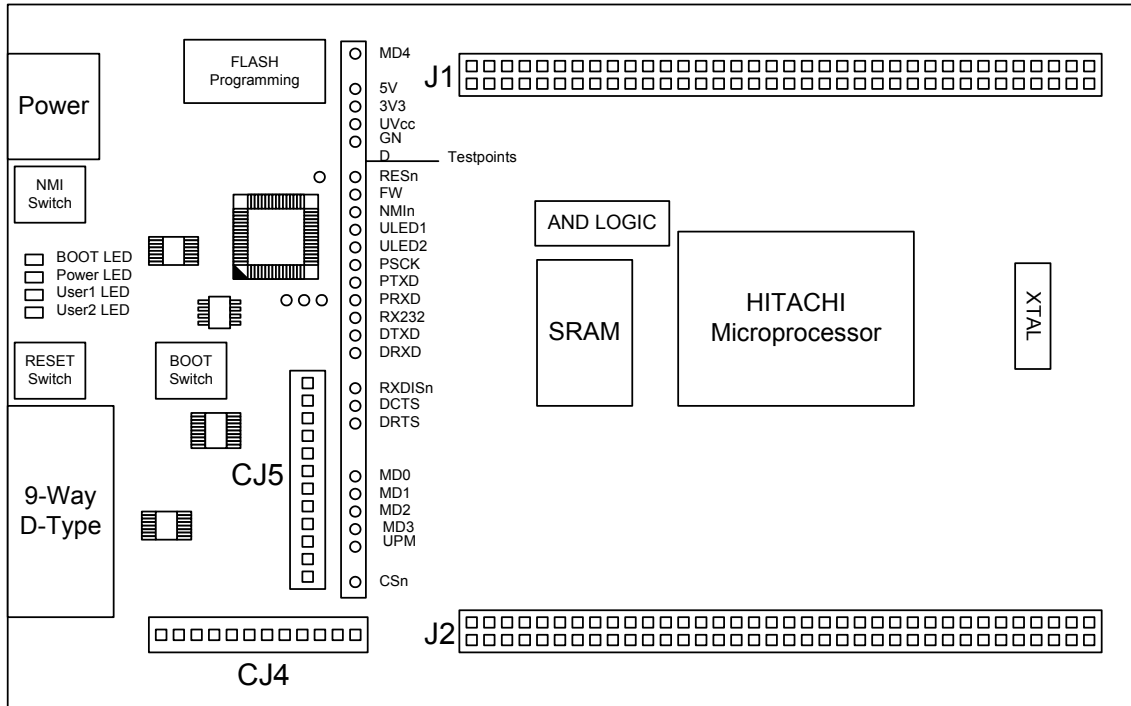


FIGURE 3-1: EDK BOARD LAYOUT

3.1. EDK BLOCK DIAGRAM

The diagram shows the connectivity of the components on the EDK board.

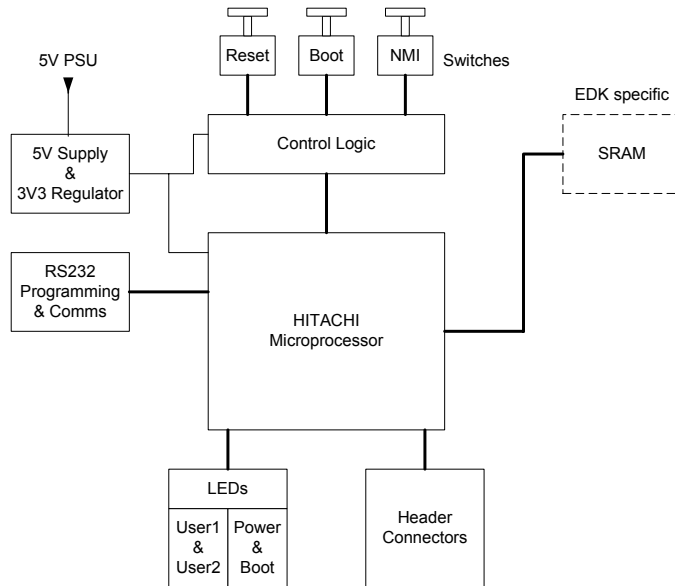


FIGURE 3-2: EDK BLOCK DIAGRAM

4. EDK OPERATION

4.1. USER INTERFACE

The EDK provides three buttons for influencing the operation of the board. The purpose of each button is clearly marked next to it. Refer to the board layout for positions (Section 3)

1. Reset Switch

This button provides the microcontroller with a timed reset pulse of at least 250mS.

2. Boot Switch

This button toggles the operating mode of the microcontroller. A complete description of this function is given in section 5.6.

3. NMI Switch

This button provides a de-bounced signal to the microcontroller for each operation of the button. There is no minimum or maximum activation time for this button.

4.2. SERIAL INTERFACE

The serial interface on the EDK board has several functions. The serial port on the microcontroller directly supports three wire serial interfaces. Options are provided on the board for the user to write handshaking routines using standard port pins. Other board option links allow users to control the entry and exit from boot mode using the same handshaking signals. Refer to section 5 for details on setting serial interface options.

4.2.1. CONNECTOR PIN DEFINITIONS

The EDK RS232 interface conforms to Data Communication Equipment (DCE) format allowing the use of 1-1 cables when connected to Data Terminal Equipment (DTE) such as an IBM PC. The cable used to connect to the EDK will affect the available board options. A fully wired cable can allow handshaking between the microcontroller and the host PC, subject to setting the board options and the availability of suitable host software. Handshaking is not supported as standard on the microcontroller so for normal use a minimal three-wire cable can be used. The minimum connections are unshaded in the following table.

| EDK DB9 Connector Pin | Signal | Host DB9 Connector Pin |
|-----------------------|--------------------|------------------------|
| 1 | No Connection | 1 |
| 2 | EDK Tx Host Rx | 2 |
| 3 | EDK Rx Host Tx | 3 |
| 4 | No Connection | 4 |
| 5 | Ground | 5 |
| 6 | No Connection | 6 |
| 7 | * EDK CTS Host RTS | 7 |
| 8 | * EDK RTS Host CTS | 8 |
| 9 | No Connection | 9 |

TABLE 4-1: RS232 INTERFACE CONNECTIONS

* These are not connected on the EDK by default. See section 5.4 for more details.

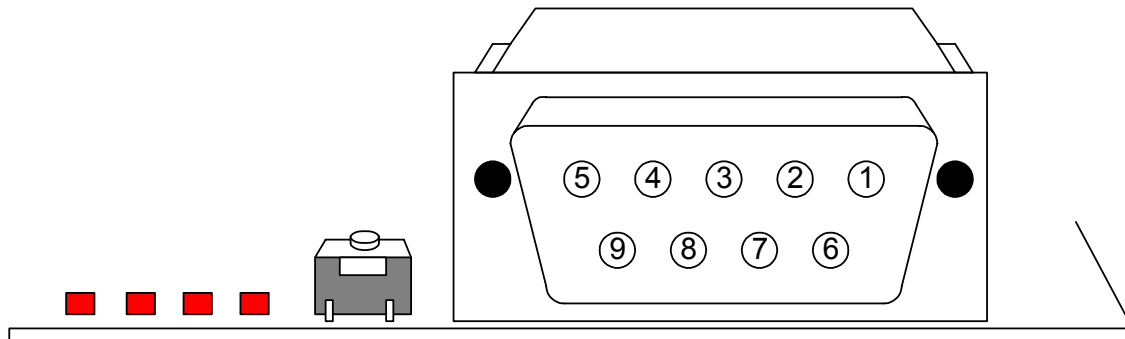


FIGURE 4-1: EDK SERIAL PORT PIN NUMBERING

4.2.2. CRYSTAL CHOICE

The operating crystal frequency has been chosen to support the fastest operation with the fastest serial operating speeds. The value of the crystal is 22.1184MHz.

The following table shows the baud rates and Baud Rate Register (BRR) setting required for each communication rate using the above default operating speed. It also confirms the resultant baud rate and the bit error rate that can be expected.

| Baud Rate Register Settings for Serial Communication Rates | | | | | | | | | | | | |
|--|-------------|-------------|---------|-------------|-------------|---------|-------------|-------------|---------|-------------|-------------|---------|
| SMR Setting: | 0 | | | 1 | | | 2 | | | 3 | | |
| Comm. Baud | BRR setting | Actual Rate | ERR (%) | BRR setting | Actual Rate | ERR (%) | BRR setting | Actual Rate | ERR (%) | BRR setting | Actual Rate | ERR (%) |
| 110 | invalid | invalid | invalid | invalid | invalid | invalid | invalid | invalid | invalid | 97 | 110.20 | 0.19 |
| 300 | invalid | invalid | invalid | invalid | invalid | invalid | 143 | 300 | 0.00 | 35 | 300 | 0.00 |
| 1200 | invalid | invalid | invalid | 143 | 1200 | 0.00 | 35 | 1200 | 0.00 | 8 | 1200 | 0.00 |
| 2400 | invalid | invalid | invalid | 71 | 2400 | 0.00 | 17 | 2400 | 0.00 | 4 | 2160 | -10.00 |
| 4800 | 143 | 4800 | 0.00 | 35 | 4800 | 0.00 | 8 | 4800 | 0.00 | 1 | 5400 | 12.50 |
| 9600 | 71 | 9600 | 0.00 | 17 | 9600 | 0.00 | 4 | 8640 | -10.00 | 0 | 10800 | 12.50 |
| 19200 | 35 | 19200 | 0.00 | 8 | 19200 | 0.00 | 1 | 21600 | 12.50 | invalid | invalid | invalid |
| 38400 | 17 | 38400 | 0.00 | 4 | 34560 | -10.00 | 0 | 43200 | 12.50 | invalid | invalid | invalid |
| 57600 | 11 | 57600 | 0.00 | 2 | 57600 | 0.00 | invalid | invalid | invalid | invalid | invalid | invalid |
| 115200 | 5 | 115200 | 0.00 | 1 | 86400 | -25.00 | invalid | invalid | invalid | invalid | invalid | invalid |
| 230400* | 2 | 230400 | 0.00 | invalid | invalid | invalid | invalid | invalid | invalid | invalid | invalid | invalid |
| 460800* | 1 | 345600 | -25.00 | invalid | invalid | invalid | invalid | invalid | invalid | invalid | invalid | invalid |

TABLE 4-2 CRYSTAL FREQUENCIES FOR RS232 COMMUNICATION

* Note: The device used to convert the RS232 serial information to logic signals for the microcontroller is limited to 120kBaud. The rates above this level can only be utilised if the user provides direct logic level communications.

The default communication rate for the EDK is indicated by the shaded selection.

The user may replace the HC49/U surface mounted AT cut crystal with another of similar type within the operating frequency of the microcontroller device. Please refer to the hardware manual for the microcontroller for the valid operating range.

Alternatively the user may fit an oscillator module – or provide an external clock source. When providing an oscillator module or external source it is highly recommended that the load capacitors for the AT crystal are removed from the PCB. These are physically placed within the PCB outline of the oscillator module for easy location and to ensure they are removed when using this option.

When changing the crystal frequency the pre-loaded debugging monitor will not function. In this situation the user is responsible for providing code to evaluate the device away from the default operating speed.

4.2.3. REMOVABLE COMPONENT INFORMATION.

This information is provided to allow the replacement of components removed from the board as described in section 4.2.2.

| Component | Cct. Ref | Value | Rating | Manufacturer |
|----------------------|----------|-------|--------------|----------------------|
| Load Resistor (X2) | R15 | 1MΩ | 0805 1% | Welwyn WCR Series |
| Load capacitors (X2) | C11,12 | 10pF | 0603 10% 25V | AVX 0603 3 A 150 KAT |

TABLE 4-3: REMOVABLE COMPONENT INFORMATION

Care must be taken not to damage the tracking around these components. Only use soldering equipment designed for surface mount assembly and rework.

4.3. SRAM

The SRAM device fitted to the board is a 4Mbit device allowing 256 x 16 operation. EDK3069 supports only 16-bit access.

The H8/3069 microcontroller has chip select management built in. There is no external chip selection hardware associated with this device. The SRAM is connected to Chip Select 0 (CS0), which can address the range H'00080000 – H001FFFFF. However, as the SRAM is 4Mbit in size, the highest accessible address is H'000FFFFF.

Provision has been made for disabling the connection between the glue logic and the lower-byte select of the SRAM via jumper link CJ4 (pins 8 - 9).

4.4. MEMORY MAP

Table 4-4 illustrates the EDK memory map for mode 5.

| Section Start Section End | Section Allocation |
|------------------------------|----------------------------|
| H'000000 H'07FFFF | On – Chip ROM |
| H'080000 H'FEDFFF | External Address Space |
| H'FEE000 H'FEE0FF | Internal I/O Registers (1) |
| H'FEE100 H'FFBF1F | External Address Space |
| H'FFBF20 H'FFFF1F | On-Chip RAM |
| H'FFFF20 H'FFFFE9 | Internal I/O Registers (2) |
| H'FFFEEA H'FFFFFF | External Address Space |

TABLE 4-4: MEMORY MAP (DEFAULT MODE 5)

4.5. SRAM ACCESS TIMING

External access timing is defined by several registers, allowing different types of devices to be addressed. The registers for the selection of wait states and signal extensions are given below with recommended values for the EDK.

| Register | Address | Recommended Setting for EDK | Function |
|-----------------|---------------------|-----------------------------|---|
| BCR | H'EE024 | Default | En/disables idle cycle insertion, selects address map, area division unit and burst ROM parameters. |
| ABWCR | H'EE020 | 0x00 | Sets up access as 16-bit for each memory area |
| P1DDR, P2DDR | H'EE000, H'EE001 | 0xFF | Allows ports 1 and 2 to be used as address lines as it sets these ports as outputs. |
| P5DDR | H'EE004 | 0xF7 | Sets bits 2 to 0 on port 5 as output for address lines A16 to A18. |
| P8DDR | H'EE007 | Bit 0 set to 1 | This enables chip select 0 |
| WCRL | H'EE023 | 0x01 | Specifies 1 wait cycle for CS0 space. |

TABLE 4-5: SRAM ACCESS CONTROL REGISTERS

Please refer to the hardware manual for the microcontroller for more information on these register settings.

4.6. LEDs

The EDK has four red LEDs. The function of each LED is clearly marked on the silk screen of the PCB. Please refer to the board layout diagram for position information (Section 3).

When the board is connected to a power source the Power (PWR) led will illuminate. The Boot mode indication LED will illuminate when the microcontroller has been placed into Boot mode. Please see section 5.6 for more details of this function.

There are two LEDs dedicated for user control these are marked USR1 and USR2. Each LED will illuminate when the port pin is in a logical high state.

The user LEDs are connected to the following ports:

| LED Identifier | Port Pin | Microcontroller Pin | Pin Functions on Port Pin |
|----------------|----------|---------------------|---------------------------|
| USR1 | PA2 | Pin 95 | TP0/TCLKA/TEND0n/PA0 |
| USR2 | PA3 | Pin 96 | TP1/TCLKB/TEND1n/PA1 |

TABLE 4-6: LED PORT CONNECTIONS

5. BOARD OPTIONS

The EDK has a number of configuration settings set by jumpers CJ4 (A, B, C, D) CJ5 (A, B, C, D) and zero-ohm links. Common EDK functions can be set using the jumpers as described in sections 5.3 and 5.2. The additional zero-ohm links provide additional features that may be required to interface with other systems.

All the Jumper link settings are three pin options. There are four sets of options on each header.

The headers are numbered from 1 to 12 with pin 1 marked on the PCB by an arrow pointing to the pin. The diagram below shows the numbering of these jumper links and indicates jumpers fitted 1-2 for each three-pin jumper.

5.1. JUMPER LINKS

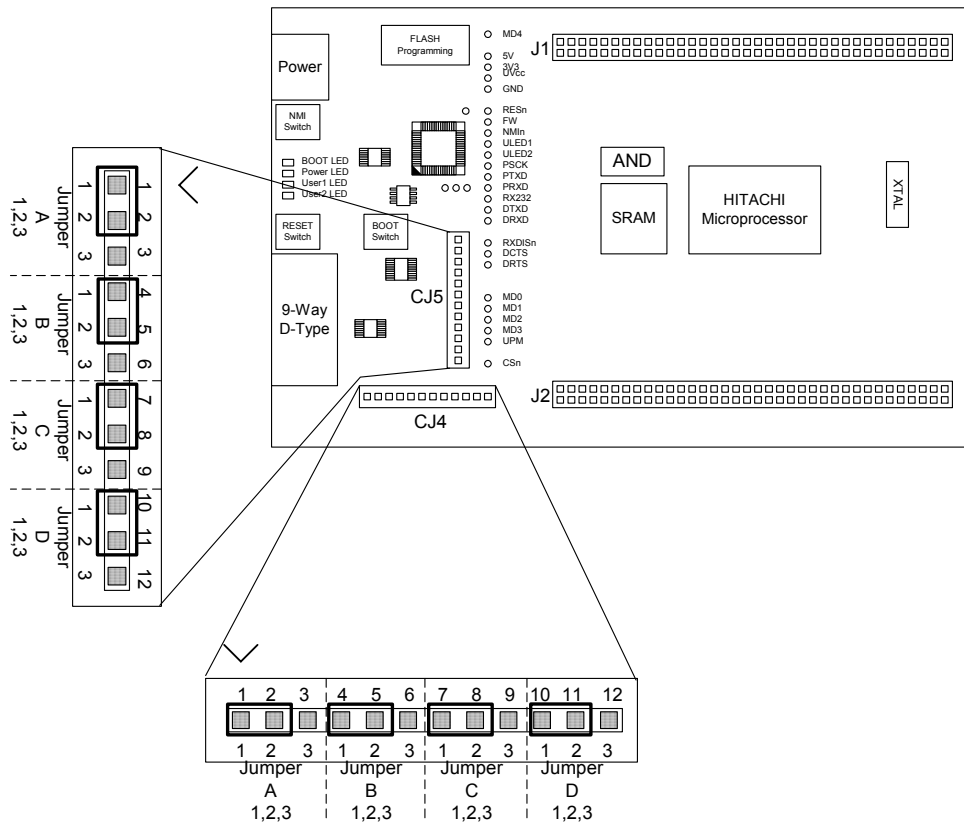


FIGURE 5-1: JUMPER CONFIGURATION

The following tables define each jumper and its settings.

5.2. USER MODE SETTINGS – CJ5

CJ5 is used to set the operating mode of the microcontroller.

These jumpers must be fitted at all times to ensure correct operation of the EDK.

| Jumper | Function | Setting 1-2 | Setting 2-3 |
|-----------------------|-------------------------|---|-------------------------------------|
| CJ 5-A Default 1-2 | User Mode Setting Bit 0 | MD0 pulled High | MD0 pulled Low |
| CJ 5-B Default 2-3 | User Mode Setting Bit 1 | MD1 pulled High | MD1 pulled Low |
| CJ 5-C Default 1-2 | User Mode Setting Bit 2 | MD2 pulled High | MD2 pulled Low |
| CJ 5-D Default 1-2 | User Mode Setting Bit 3 | MD3 pulled High [NOT USED] | MD3 pulled Low [NOT USED] |

TABLE 5-1: USER MODE: JUMPER SETTINGS (DEFAULT SETTINGS IN BOLD)

The default settings indicated in bold text place the microcontroller into Mode 5.

5.3. EDK OPTIONS – CJ4

The EDK options provide access to commonly used features of the EDK range.

These jumpers must be fitted at all times to ensure correct operation of the EDK.

| Jumper | Function | Setting 1-2 | Setting 2-3 |
|-----------------------|---------------------------------|--|--|
| CJ 4-A Default 2-3 | Serial Receive Source | Disables the RS232 receive signal to enable the use of the Flash Programming Header | Enables the RS232 receive signal. The Flash Programming Header* must not be used in this state. |
| CJ 4-B Default 2-3 | User Programming Mode | Disables the Flash write hardware protection. The flash can be overwritten in User Mode. | Enables the Flash write hardware protection. The flash can not be overwritten in User Mode. |
| CJ 4-C Default 2-3 | Chip Select Disable | SRAM is enabled; port 8, pin 4 of the microcontroller is connected to the chip select of the SRAM. | SRAM is disabled. The chip select of the SRAM is a No Connect. |
| CJ 4-D Default 1-2 | Boot / User Boot Mode selection | Microcontroller enters Boot mode on reset | Microcontroller enters User Boot mode on reset |

TABLE 5-2: BOARD OPTION: JUMPER SETTINGS (DEFAULT SETTINGS IN BOLD)

*See section 5.5

The following table lists the connections to each jumper pin.

| Pin | Net Name | Description |
|-----|---------------|--|
| 1 | UVCC | Microcontroller Supply Voltage |
| 2 | RXDISn | Disable Flash Header functions. Pulled low. (Enables RX232) |
| 3 | No Connection | No Connection |
| 4 | UVCC | Microcontroller Supply Voltage |
| 5 | UPM | CPLD Controlled option to set Flash Write (FW). Pulled low. |
| 6 | No Connection | No Connection |
| 7 | P84 | CS0 of microcontroller |
| 8 | CSn | Chip select of SRAM |
| 9 | No Connection | No Connection |
| 10 | UVCC | Pull up to Power supply via 4k7 resistor |
| 11 | BOOT_NMI | NMI signal is used to control entry into either boot or user boot mode on a reset. |
| 12 | Ground | Pull down to ground. |

5.4. SERIAL PORT SELECTION

The programming serial port is connected to the RS232 connector by default. This allows direct programming of the EDK using the supplied software tools. A secondary serial port is available on the microcontroller and can be connected to the RS232 connector by changing some board option links. The additional port option allows the user to write messages or connect to other devices via the serial port while programming support is provided by the Flash programming header.

The following surface mount, zero-ohm link settings are fitted by default and connect the RS232 header to the programming serial port of the microcontroller.

| Zero-ohm Link ID | Default | Function | Microcontroller Port Pin |
|------------------|------------|----------------------------------|--------------------------|
| CR20 | Fitted | Transmit data from EDK | P91 |
| CR23 | Fitted | Receive data to EDK | P93 |
| CR19 | Not Fitted | Alternate Transmit data from EDK | P90 |
| CR22 | Not Fitted | Alternate Receive data to EDK | P92 |

TABLE 5-3: OPTION LINKS – DEFAULT SETTINGS

To enable the use of this alternate port the user must change the settings to those in the following table.

| Zero-ohm Link ID | Default | Function | Microcontroller Port Pin |
|------------------|------------|----------------------------------|--------------------------|
| CR20 | Not Fitted | Transmit data from EDK | P91 |
| CR23 | Not Fitted | Receive data to EDK | P93 |
| CR19 | Fitted | Alternate Transmit data from EDK | P90 |
| CR22 | Fitted | Alternate Receive data to EDK | P92 |

TABLE 5-4: OPTION LINKS – ALTERNATE SERIAL PORT

The user may implement a handshaking protocol on the EDK. This is not supported with the software tools supplied. To support this option two spare port pins have been allocated on the microcontroller. Using these port pins the CTS and RTS lines of the host serial interface can be controlled.

The user may also control the operation of the board via the same handshaking lines. This is not supported with the software tools supplied but may be written by the user. Using the CTS line the user may simulate pressing the boot button, see section:5.6. This will cause the EDK to swap into and out of Boot mode on each low-level activation of CTS. Feedback of the current mode is provided on the RTS line. A high level indicates boot mode and a low level indicates user mode.

The following settings are made by default, and ensure that there are no conflicts on unnecessary microcontroller pins.

| Zero-ohm Link ID | Default | Function | Microcontroller Port Pin |
|------------------|------------|---|--------------------------|
| CR12 | Not Fitted | Mode State out from EDK | N/A (From CPLD*) |
| CR7 | Not Fitted | Change Mode request to EDK | N/A (From CPLD*) |
| CR16 | Not Fitted | Alternate RTS232 – Ready to send – from EDK | P81 |
| CR13 | Not Fitted | Alternate CTS232 – Clear to send – to EDK | P80 |

TABLE 5-5: OPTION LINKS – SERIAL PORT CONTROL

* See section 5.6

Note: These setting pairs are exclusive:
If CR12 and CR7 are fitted; CR16 and CR13 must not be fitted.
If CR16 and CR13 are fitted; CR12 and CR7 must not be fitted.

5.5. FLASH PROGRAMMING HEADER

The Flash Programming header is used with the Hitachi Flash Debug Board (FDB). The FDB is a USB based programming tool for control and programming of Hitachi microcontrollers, available separately from Hitachi. This header provides direct access for the FDB to control the EDK microcontroller.

To utilise this header the user must make the following changes to the board configuration.

1. Disable the RX232 signal from the RS232 transceiver.
Jumper link CJ4-A is provided for this purpose. Please refer to section5.3.
2. Disable User Program Mode using jumper CJ4-B. Please refer to section5.3.

Caution: Do not operate the board with the user mode jumpers removed and the FDB disconnected as the microcontroller mode pins will float to an indeterminate state. This may damage the microcontroller device.

5.6. BOOT AND USER BOOT CONTROL

The timing of specific control signals required for placing the microcontroller device into any mode for reprogramming or running software is performed by a complex programmable logic device (CPLD). This device detects a power up event and provides a timed reset pulse to guarantee the reset of the microcontroller. At the end of the reset pulse the processor will be placed in user mode and any code in the device will execute. The CPLD is not necessary for most user designs, but allows increased flexibility for the EDK designs. Factually, mode transitions including boot mode transitions require the reset and / or the FWE pin to be held active while the appropriate mode settings are presented to the microcontroller. On releasing reset, the microcontroller will then be in the required mode of operation. The value at the mode pins must not however, be altered during the operation of the microcontroller.

During user mode the NMI button can be pressed at any time. This will provide a single de-bounced NMI interrupt to the device.

Pressing the boot button will cause the boot mode controller to reset the device and, during the reset period, present the required mode settings to start the device in either boot or user boot mode. The setting of jumper 4 on CJ4 determines whether the microcontroller enters user boot mode or boot mode (See section 5.3). At the end of the reset period the boot mode settings will have been latched into the device which will then be ready to accept a boot / user boot mode connection via the RS232 interface or the flash programming header. Pressing the boot button during a normal reset will not cause the EDK to enter either boot mode or user boot mode.

The boot mode settings are fixed at mode 1. The required mode settings are made using a tri-state capable buffer.

Note: The boot control device is programmed to support all possible EDK products.
For this reason the reset pulse is over 500ms. Repetitive activation of either the Boot or Reset buttons will restart the reset timer and extend the reset period. Pressing the boot button within the 500mS period of a reset will not cause the board to enter boot mode.

5.6.1. UTILISATION NOTES FOR USER BOOT MODE

A Note on Mats:

The H8/3069 possesses two distinct areas of Flash, User MAT (512KByte) and User Boot MAT (8KByte). The User Boot MAT is a separate area of FLASH from User MAT, intended to hold user boot code.

User Boot Mode:

A custom boot stub could be programmed into User Boot MAT which allows programming and erasing of the User MAT in User Mode, without erasing the contents of the User Boot MAT. Once User Boot Mode is entered, code contained in the User Boot MAT is executed. This differs to Boot mode, as Boot mode erases all User MAT and requires an auto-baud on a fixed SCI port to be performed. The existence of the user boot Mat therefore allows an alternative communications port to be used for further code download to the User MAT. Programming of the user boot mat can, however, only be performed in boot mode.

For entry to User Boot mode on EDK3069, jumper D on jumper block CJ4 must be fitted 11-12, then the boot button depressed once. The Boot LED should light, suggesting a transition to user boot mode.

5.6.2. CPLD CODE

The code is based upon a four state machine providing a guaranteed reset period which can be extended by holding the relevant control input in the active state. When released the timer will extend the reset for approximately 500mS.

The states are split into two functions, one for User mode and one for Boot mode. The first state of each is used to hold the reset line active. When the timer expires then the second state is used to hold the device in the selected mode and wait for an external control signal to either move back into the user reset state or into the boot reset state.

5.6.3. STATE DIAGRAM

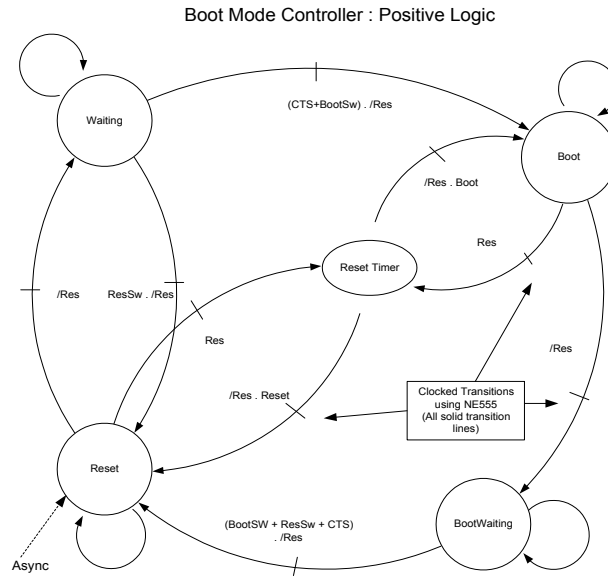


FIGURE 5-2: CPLD STATE DIAGRAM

6. MICROCONTROLLER HEADER CONNECTIONS

The following table lists the connections to each of the headers on the board.

6.1. HEADER J1

| J1 | | | | | | | |
|--------|----------------------------|------------|------------|--------|-----------------------|------------|------------|
| Pin No | Function | EDK Symbol | Device pin | Pin No | Function | EDK Symbol | Device pin |
| 1 | VSS | GND | 11 | 2 | FWE | FW | 10 |
| 3 | PB7/RxD2/TP15 | PB7 | 9 | 4 | PB6/TxD2/TP14 | PB6 | 8 |
| 5 | PB5/SCK2/LCASn/TP13 | PB5 | 7 | 6 | PB4/UCASn/TP12 | PB4 | 6 |
| 7 | PB3/CS4n/DREQ1n/TMIO3/TP11 | PB3 | 5 | 8 | PB2/CS5n/TMO2/TP10 | PB2 | 4 |
| 9 | PB1/CS6n/DREQ0n/TMIO1/TP9 | PB1 | 3 | 10 | PB0/CS7n/TMO0/TP8 | PB0 | 2 |
| 11 | Vcl | NC_J1_11 | 1 | 12 | PA7/TP7/TIOCB2/A20 | PA7 | 100 |
| 13 | PA6/TP6/TIOCA2/A21 | PA6 | 99 | 14 | PA5/TP5/TIOCB1/A22 | PA5 | 98 |
| 15 | PA4/TP4/TIOCA1/A23 | PA4 | 97 | 16 | PA3/TP3/TIOCB0/TCLKD | ULED2 | 96 |
| 17 | PA2/TP2/TIOAC0/TCLKC | ULED1 | 95 | 18 | PA1/TP1/TCLKB/TEND1n | PA1 | 94 |
| 19 | PA0/TP0/TCLKA/TEND0n | PA0 | 93 | 20 | Vss | GND | 92 |
| 21 | P84/CS0n | P84 | 91 | 22 | P83/IRQ3n/CS1n/ADTRGn | P83 | 90 |
| 23 | P82/IRQ2n/CS2n | P82 | 89 | 24 | P81/IRQ1n/CS3n | DRTS | 88 |
| 25 | P80/IRQ0n/RFSHn | DCTS | 87 | 26 | AVss | CON_AVSS | 86 |
| 27 | P77/AN7/DA1 | P77 | 85 | 28 | P76/AN6/DA0 | P76 | 84 |
| 29 | P75/AN5 | P75 | 83 | 30 | P74/AN4 | P74 | 82 |
| 31 | P73/AN3 | P73 | 81 | 32 | P72/AN2 | P72 | 80 |
| 33 | P71/AN1 | P71 | 79 | 34 | P70/AN0 | P70 | 78 |
| 35 | VREF | CON_VREF | 77 | 36 | AVcc | CON_AVCC | 76 |
| 37 | MD2 | MD2 | 75 | 38 | MD1 | MD1 | 74 |
| 39 | MD0 | MD0 | 73 | 40 | P66/LWRn | P66 | 72 |
| 41 | P65/HWRn | P65 | 71 | 42 | P64/RDn | P64 | 70 |
| 43 | P63/Asn | P63 | 69 | 44 | Vcc | UVCC | 68 |
| 45 | XTAL | CON_XTAL | 67 | 46 | EXTAL | CON_EXTAL | 66 |
| 47 | Vss | GND | 65 | 48 | NMI | NMIIn | 64 |
| 49 | RESn | RESn | 63 | 50 | STBYn | STBYn | 62 |

6.2. HEADER J2

| J2 | | | | | | | |
|--------|----------------|------------|------------|--------|----------------|------------|------------|
| Pin No | Function | EDK Symbol | Device pin | Pin No | Function | EDK Symbol | Device pin |
| 1 | P90/TxD0 | P90 | 12 | 2 | P91/TxD1 | PTXD | 13 |
| 3 | P92/RxD0 | P92 | 14 | 4 | P93/RxD1 | PRXD | 15 |
| 5 | P94/IRQ4n/SCK0 | P94 | 16 | 6 | P95/IRQ5n/SCK1 | PSCK | 17 |
| 7 | P40/D0 | P40 | 18 | 8 | P41/D1 | P41 | 19 |
| 9 | P42/D2 | P42 | 20 | 10 | P43/D3 | P43 | 21 |
| 11 | VSS | VSS | 22 | 12 | P44/D4 | P44 | 23 |
| 13 | P45/D5 | P45 | 24 | 14 | P46/D6 | P46 | 25 |
| 15 | P47/D7 | P47 | 26 | 16 | P30/D8 | P30 | 27 |
| 17 | P31/D9 | P31 | 28 | 18 | P32/D10 | P32 | 29 |
| 19 | P33/D11 | P33 | 30 | 20 | P34/D12 | P34 | 31 |
| 21 | P35/D13 | P35 | 32 | 22 | P36/D14 | P36 | 33 |
| 23 | P37/D15 | P37 | 34 | 24 | Vcc | UVCC | 35 |
| 25 | P10/A0 | P10 | 36 | 26 | P11/A1 | P11 | 37 |
| 27 | P12/A2 | P12 | 38 | 28 | P13/A3 | P13 | 39 |
| 29 | P14/A4 | P14 | 40 | 30 | P15/A5 | P15 | 41 |
| 31 | P16/A6 | P16 | 42 | 32 | P17/A7 | P17 | 43 |
| 33 | VSS | VSS | 44 | 34 | P20/A8 | P20 | 45 |
| 35 | P21/A9 | P21 | 46 | 36 | P22/A10 | P22 | 47 |
| 37 | P23/A11 | P23 | 48 | 38 | P24/A12 | P24 | 49 |
| 39 | P25/A13 | P25 | 50 | 40 | P26/A14 | P26 | 51 |
| 41 | P27/A15 | P27 | 52 | 42 | P50/A16 | P50 | 53 |
| 43 | P51/A17 | P51 | 54 | 44 | P52/A18 | P52 | 55 |
| 45 | P53/A19 | P53 | 56 | 46 | Vss | GND | 57 |
| 47 | P60/WAITn | P60 | 58 | 48 | P61/BREQn | P61 | 59 |
| 49 | P62/BACKn | P62 | 60 | 50 | P67/φ | P67 | 61 |

7. CODE DEVELOPMENT

7.1. HMON

7.1.1. MODE SUPPORT

The HMON library is built to support Modes 1, 2, 3, 4, 5 and 7. The Device supports only these modes.

7.1.2. BREAKPOINT SUPPORT

The monitor utilises traps which have vectors located in ROM. User code located in RAM may have multiple breakpoints limited only by the size of the On-Chip RAM.

7.1.2.1. CODE LOCATED IN FLASH / ROM

Double clicking in the breakpoint column in the code sets the breakpoint. Adding a further breakpoint elsewhere in the code removes the previous one.

7.1.2.2. CODE LOCATED IN RAM

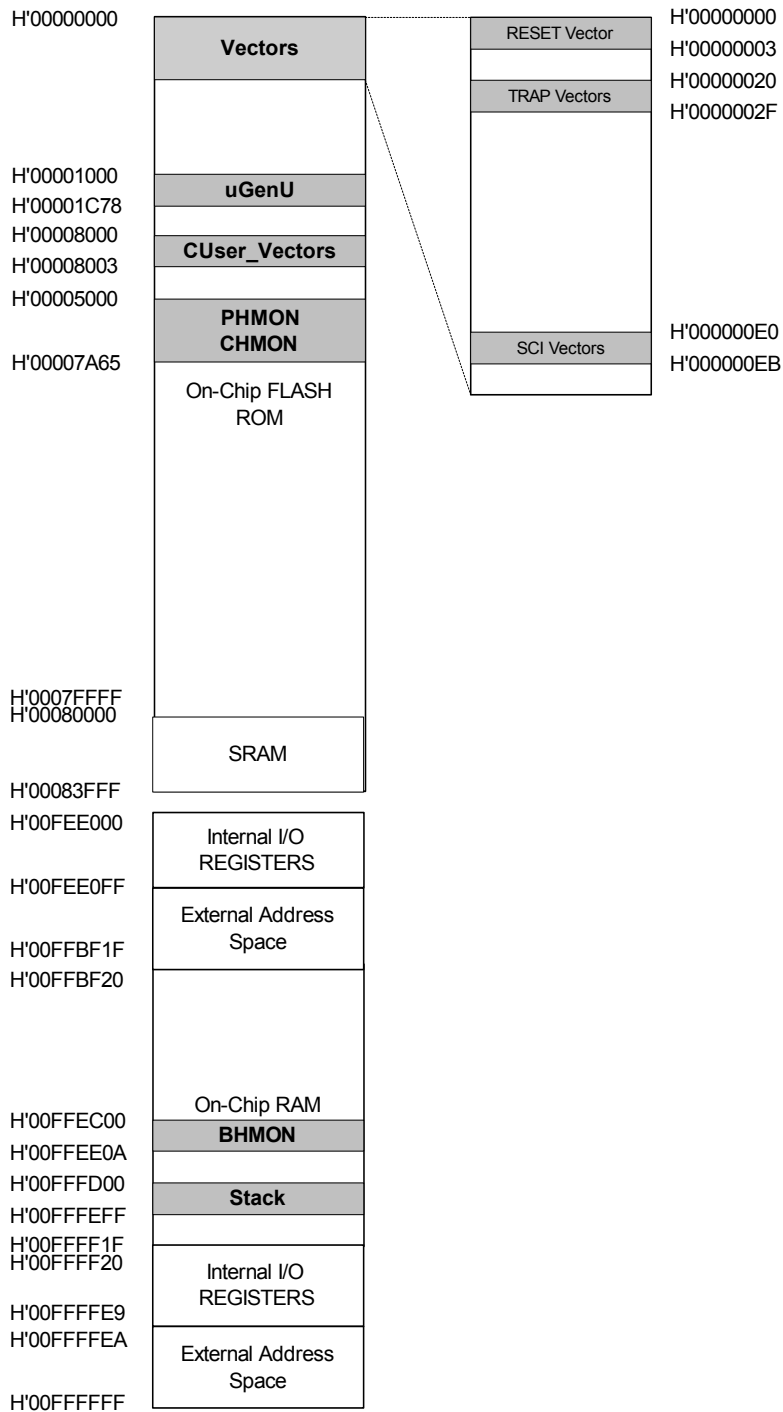
Double clicking in the breakpoint column in the code sets the breakpoint. Breakpoints will remain unless they are double clicked to remove them.

7.1.3. HMON CODE SIZE

HMON is built along with the debug code. Certain elements of the HMON code must remain at a fixed location in memory. The following table details the HMON components and their size and location in memory. For more information, refer to the map file when building code.

| Section | Description | Start Location | Size (H'bytes) |
|---------------|---|----------------|----------------|
| RESET_VECTOR | HMON Reset Vector (Vector 0) Required for Startup of HMON | H' 00000000 | 4 |
| TRAP_VECTORS | Trap Vectors (Vector 8, 9, 10, 11) Required by HMON to create Trap Breakpoints in RAM | H' 00000020 | 10 |
| SCI_VECTORS | HMON Serial Port Vectors (Vector 80, 81, 82, 83) Used by HMON when EDK is configured to connect to the default serial port. | H' 000000E0 | C |
| UGenU | FDT User Mode Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled. | H' 00001000 | C79 |
| PHMON | HMON Code | H' 00005000 | 2928 |
| CHMON | HMON Constant Data | H' 00007928 | 13E |
| BHMON | HMON Uninitialised data | H' 00FFEC00 | 20B |
| CUser_Vectors | Pointer used by HMON to point to the start of user code. This is at a fixed location and must not be moved for the Reset CPU, and Go Reset commands to function. | H' 00008000 | 4 |

7.1.4. MEMORY MAP



7.1.5. BAUD RATE SETTING

HMON has initially set to connect at 115200Baud. Should the user wish to change this, the value for the BRR in HMONserialconfiguser.c will need to be changed and the project re-built. Please refer to the HMON User Manual for further information.

7.1.6. INTERRUPT MASK SECTIONS

HMON has an interrupt priority of 1. The serial port has an interrupt priority of 1. Modules using interrupts should be set to lower than this value so that serial communications and debugging capability is maintained.

7.1.7. LIMITATIONS OF USE FOR HMON

H8/3069 has two interrupt levels for each interrupt, which can be defined as 1 or 0. Whilst the monitor is running, the condition code register is set up such that interrupts with a priority level of less than 1 are not accepted. This does not prevent users code from allowing interrupts of priority level 0 in the condition code register, but these interrupts will only be accepted whilst the user code is running.

7.2. ADDITIONAL INFORMATION

For details on how to use Hitachi Embedded Workshop (HEW), with HMON, refer to the HEW manual available on the CD or from the web site.

For information about the H8/3069 series microcontrollers refer to the *H8/3069 Series Hardware Manual*

For information about the H8/300H assembly language, refer to the *H8/300H Series Programming Manual*

Further information available for this product can be found on the HMSE web site at:

<http://www.hmse.com/products/support.htm>

General information on Hitachi Microcontrollers can be found at the following URLs.

Global: <http://www.hitachisemiconductor.com>

Europe: <http://www.hmse.com>