EDK2676

USER MANUAL

FOR H8S/2676
ON-CHIP FLASH MICROCONTROLLER

Preface

Cautions

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Document Information

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Website: http://www.eu.renesas.com/

1. TABLE OF CONTENTS

2. START-UP INSTRUCTIONS

2.1. INSTALLING THE EVALUATION DEVELOPMENT KIT (EDK)

Please refer to the quick start guide provided for initial installation of the EDK.

A copy of the quick start guide and other information relating to this EDK at:

http://www.eu.renesas.com/tools

Installing the EDK requires power and serial connection to a host computer.

2.2. SERIAL CONNECTION

The serial communications cable for connecting the EDK to a host computer requires 1:1 connectivity.

Figure 2-1 shows how to connect the EDK to a PC or notebook computer equipped with a nine pin D connector.

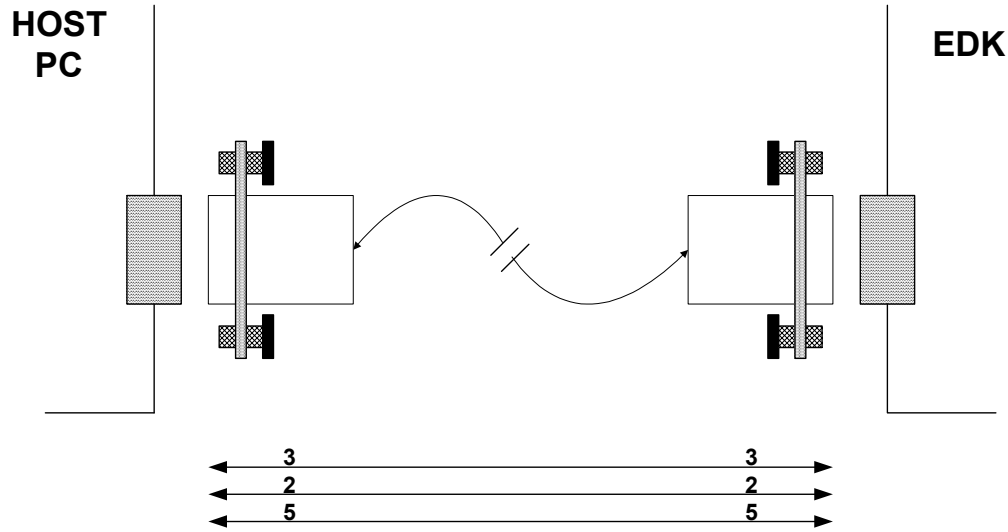


FIGURE 2-1: SERIAL CONNECTION TO PC/NOTEBOOK WITH DB-9 CONNECTOR (SUPPLIED)

2.3. POWER SUPPLY

The EDK hardware requires a power supply of +5V. Since total power consumption can vary widely due to external connections, port states, and memory configuration, use a power supply capable of providing at least 500mA at +5V DC ± 5%.

The design is specified for evaluation of the microcontroller and so does not include circuitry for supply filtering/noise reduction, under voltage protection, over current protection or reversed polarity protection. Caution should be used when selecting and using a power supply.

The power connector on the EDK is a 2.5mm Barrel connector. The center pin is the positive connection.

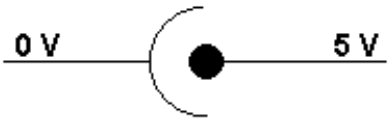


FIGURE 2-2: POWER SUPPLY CONNECTION

Caution: Existing customers using E6000 products note that the polarity of this board is opposite to that for the E6000. Use of the E6000 power supply with this board will damage both board and power supply.

3. EDK BOARD LAYOUT

The diagram shows a general layout of the EDK board.

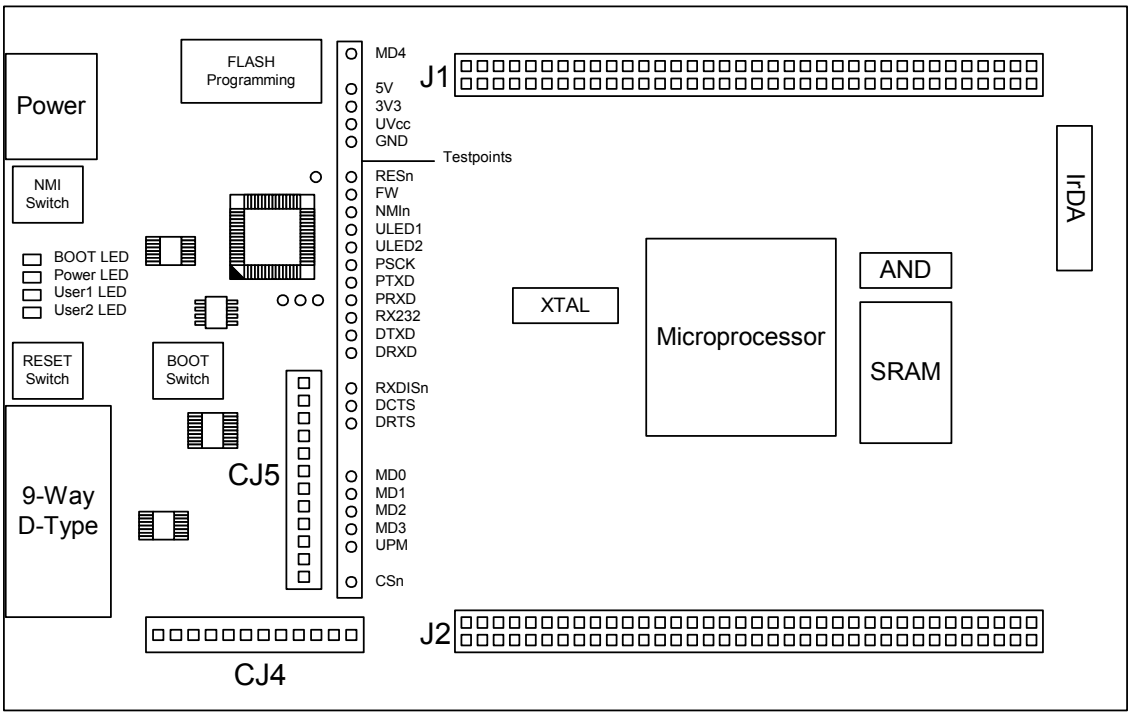


FIGURE 3-1: EDK BOARD LAYOUT

3.1. EDK BLOCK DIAGRAM

The diagram shows the connectivity of the components on the EDK board.

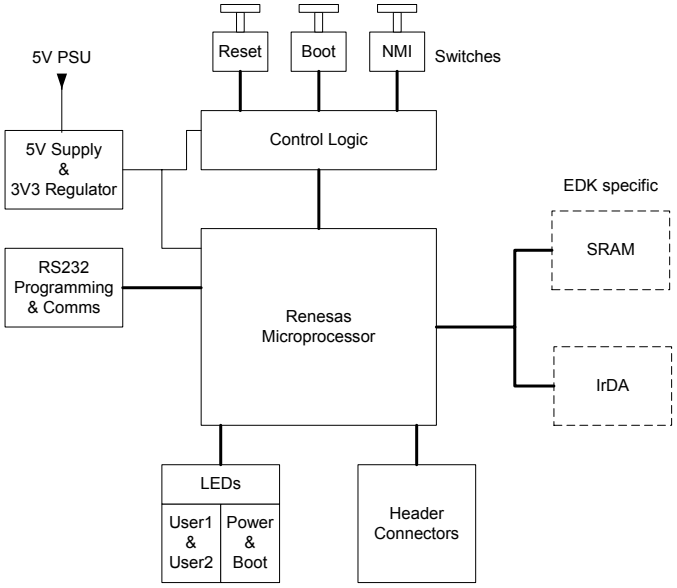


FIGURE 3-2: EDK BLOCK DIAGRAM

4. EDK OPERATION

4.1. USER INTERFACE

The EDK provides three buttons for influencing the operation of the board. The purpose of each button is clearly marked next to it. Refer to the board layout for positions (Section 3)

1. Reset Switch

This button provides the microcontroller with a timed reset pulse of at least 250mS.

2. Boot Switch

This button toggles the operating mode of the microcontroller. A complete description of this function is given in section 5.

3. NMI Switch

This button provides a de-bounced signal to the microcontroller for each operation of the button. There is no minimum or maximum activation time for this button.

4.2. SERIAL INTERFACE

The serial interface on the EDK board has several functions. The serial port on the microcontroller directly supports three wire serial interfaces. Options are provided on the board for the user to write handshaking routines using standard port pins. Other board option links allow users to control the entry and exit from boot mode using the same handshaking signals. Refer to section 5 for details on setting serial interface options.

4.2.1. CONNECTOR PIN DEFINITIONS

The EDK RS232 interface conforms to Data Communication Equipment (DCE) format allowing the use of 1-1 cables when connected to Data Terminal Equipment (DTE) such as an IBM PC. The cable used to connect to the EDK will affect the available board options. A fully wired cable can allow handshaking between the microcontroller and the host PC, subject to setting the board options and the availability of suitable host software. Handshaking is not supported as standard on the microcontroller so for normal use a minimal three-wire cable can be used. The minimum connections are unshaded in the following table.

EDK DB9 Connector Pin	Signal	Host DB9 Connector Pin
1	No Connection	1
2	EDK Tx Host Rx	2
3	EDK Rx Host Tx	3
4	No Connection	4
5	Ground	5
6	No Connection	6
7	* EDK CTS Host RTS	7
8	* EDK RTS Host CTS	8
9	No Connection	9

TABLE 4-1: RS232 INTERFACE CONNECTIONS

* These are not connected on the EDK by default. See section 5.4 for more details.

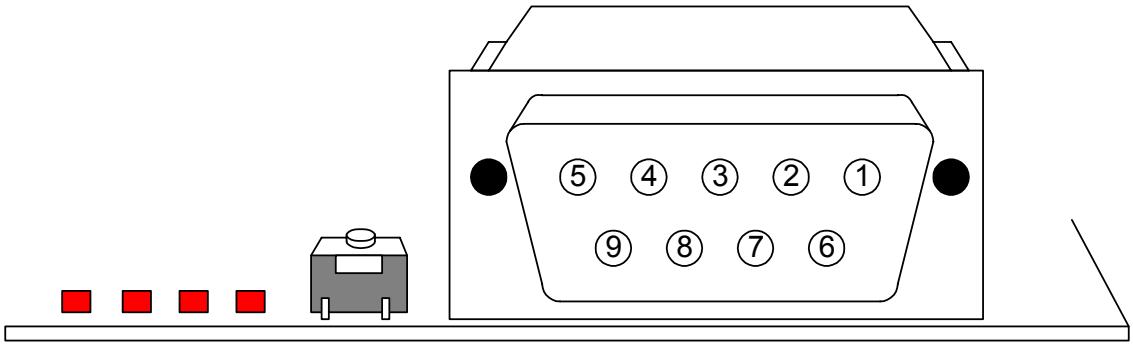


FIGURE 4-1: EDK SERIAL PORT PIN NUMBERING

4.2.2. CRYSTAL CHOICE

The operating crystal frequency has been chosen to support the fastest operation with the fastest serial operating speeds. The value of the crystal is 14.7456MHz. This is multiplied by a factor of two to obtain a default operating frequency of 29.4912MHz.

The following table shows the baud rates and Baud Rate Register (BRR) setting required for each communication rate using the above default operating speed. It also confirms the resultant baud rate and the bit error rate that can be expected.

Baud Rate Register Settings for Serial Communication Rates												
SMR Setting:	**0**			**1**			**2**			**3**		
Comm. Baud	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**
110	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	130	110	-0.07
300	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	191	300	0.00	47	300	0.00
1200	Invalid	Invalid	Invalid	191	1200	0.00	47	1200	0.00	11	1200	0.00
2400	Invalid	Invalid	Invalid	95	2400	0.00	23	2400	0.00	5	2400	0.00
4800	191	4800	0.00	47	4800	0.00	11	4800	0.00	2	4800	0.00
9600	95	9600	0.00	23	9600	0.00	5	9600	0.00	1	7200	-25.00
19200	47	19200	0.00	11	19200	0.00	2	19200	0.00	Invalid	Invalid	Invalid
38400	23	38400	0.00	5	38400	0.00	1	28800	-25.00	Invalid	Invalid	Invalid
57600	15	57600	0.00	3	57600	0.00	0	57600	0.00	Invalid	Invalid	Invalid
115200	7	115200	0.00	1	115200	0.00	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
230400*	3	230400	0.00	0	230400	0.00	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
460800*	1	460800	0.00	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid

TABLE 4-2 CRYSTAL FREQUENCIES FOR RS232 COMMUNICATION

** Note: The device used to convert the RS232 serial information to logic signals for the microcontroller is limited to 120kBaud. The rates above this level can only be utilised if the user provides direct logic level communications.*

The user may replace the HC49/U surface mounted AT cut crystal with another of similar type within the operating frequency of the microcontroller device. Please refer to the hardware manual for the microcontroller for the valid operating range.

Alternatively the user may fit an oscillator module – or provide an external clock source. When providing an oscillator module or external source it is highly recommended that the load capacitors for the AT crystal are removed from the PCB. These are physically placed within the PCB outline of the oscillator module for easy location and to ensure they are removed when using this option.

When changing the crystal frequency the pre-loaded debugging monitor will not function. In this situation the user is responsible for providing code to evaluate the device away from the default operating speed.

4.2.3. REMOVABLE COMPONENT INFORMATION.

This information is provided to allow the replacement of components removed from the board as described in section 4.2.2.

Component	Cct. Ref	Value	Rating	Manufacturer
Load Resistor (X1)	R4*	1MΩ	0805 1%	Welwyn WCR Series
Load capacitors (X1)	C1,C2	22pF	0603 10% 25V	AVX 0603 3 A 220 KAT

TABLE 4-3: REMOVABLE COMPONENT INFORMATION

* Normally not Fitted

Care must be taken not to damage the tracking around these components. Only use soldering equipment designed for surface mount assembly and rework.

4.3. SRAM

The SRAM device fitted to the board is a 4Mbit device allowing 256kx16. 8-bit addressing is not supported by this EDK.

The SRAM is connected to Chip Select 1 (CS1), which can address the range H'00200000 – H'003FFFFF. However, due to size of SRAM, the actual addressable range is H'00200000 – H'0027FFFF.

4.4. MEMORY MAP

Table 4-4 illustrates the EDK memory map for mode 4.

Section End Section Start	Section Allocation
H'00000000	On-Chip ROM
H'0003FFFF	
H'00040000	External Address Space
H'001FFFFF	
H'00200000	External RAM
H'0027FFFF	
H'00280000	External Address Space
H'00FF9FFF	
H'00FFA000	On-Chip RAM / External Address Space
H'00FFBFFF	
H'00FFC000	External Address Space
H'00FFFBFF	
H'00FFFC00	Internal I/O Registers
H'00FFFEFF	
H'00FFFF00	External Address Space
H'00FFFF1F	
H'00FFFF20	Internal I/O Registers
H'00FFFFFF	

TABLE 4-4: MEMORY MAP (DEFAULT MODE 4)

4.5. SRAM ACCESS TIMING

External access timing is defined by several registers, allowing different types of devices to be addressed. Recommended register settings for the selection of wait states and signal extensions specific to this EDK are given below

Register	Address	Recommended Setting for EDK	Function
BCR	H'FECC	0x1C04	16-bit register used for Idle Cycle Settings
DRAMCR	H'FED0	0x00 (Default)	Configures DRAM Interface Settings. This value allows OEn/(CKE) to be used as I/O pin
ABWCR	H'FEC0	0x00	Selects 2 or 3 state access space (3 is selected for this value)
RDNCR	H'FEC6	0x00 (Default)	Selects read strobe (RDn) negation timing
ASTCR	H'FEC1	0xFF (Default)	Selects 2 or 3 state space
WTCRBL	H'FEC5	0x10	Selects number of program wait states for each area
CSACRH	H'FEC8	0x00 (Default)	Selects extension of Chip select signals for each access space
CSACRL	H'FEC9	0x00 (Default)	Selects extension of Chip select signals for each access space
PFCR0	H'FE32	0x02	Port Function Control Register 0 (Selects functions of specific port pins)
PFCR2	H'FE34	0x04	Port Function Control Register 2 (Selects functions of specific port pins)
PADDR	H'FE29	0xFF	Specifies directionality of port A pins
PBDDR	H'FE2A	0xFF	Specifies directionality of port B pins
PCDDR	H'FE2B	0xFE	Specifies directionality of port C pins
PGDDR	H'FE2F	0x02	Specifies directionality of port G pins

TABLE 4-5: SRAM ACCESS CONTROL REGISTERS

Please refer to the hardware manual for the microcontroller for more information on these register settings.

4.6. LEDS

The EDK has four red LEDs. The function of each LED is clearly marked on the silk screen of the PCB. Please refer to the board layout diagram for position information (Section 3).

When the board is connected to a power source the Power (PWR) led will illuminate. The Boot mode indication LED will illuminate when the microcontroller has been placed into Boot mode. Please see section 5 for more details of this function.

There are two LEDs dedicated for user control, these are marked USR1 and USR2. Each LED will illuminate when the port pin is in a logical high state.

The user LEDs are connected to the following ports:

LED Identifier	Port Pin	Microcontroller Pin	Pin Functions on Port Pin
USR1	P26	59	PO6/TIOCA5/EDRAK0n/IRQ14n
USR2	P27	58	PO7/TIOCB5/EDRAK1n/IRQ15n

TABLE 4-6: LED PORT CONNECTIONS

5. BOARD OPTIONS

The EDK has a number of configuration settings set by jumpers CJ4 (A, B, C, D) CJ5 (A, B, C, D) and zero-ohm links. Common EDK functions can be set using the jumpers as described in sections 5.3 and 5.2. The additional zero-ohm links provide additional features that may be required to interface with other systems.

All the Jumper link settings are three pin options. There are four sets of options on each header.

The headers are numbered from 1 to 12 with pin 1 marked on the PCB by an arrow pointing to the pin. The diagram below shows the numbering of these jumper links and indicates jumpers fitted 1-2 for each three-pin jumper.

5.1. JUMPER LINKS

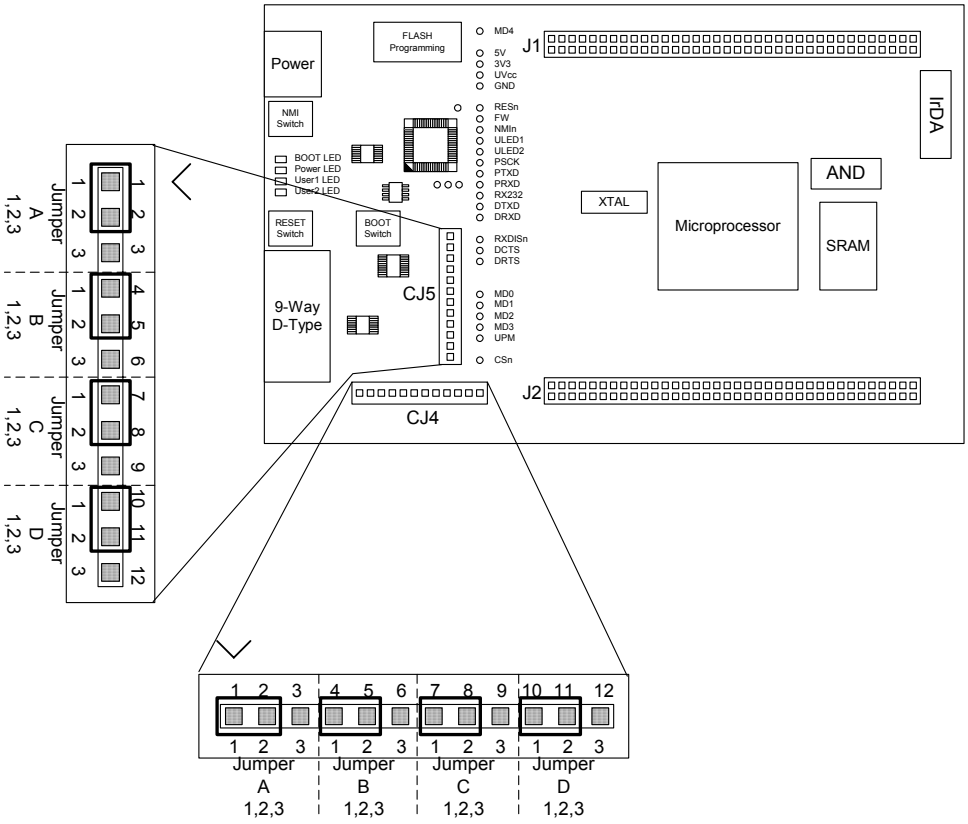


FIGURE 5-1: JUMPER CONFIGURATION

The following tables define each jumper and its settings.

5.2. USER MODE SETTINGS – CJ5

CJ5 is used to set the operating mode of the microcontroller.

These jumpers must be fitted at all times to ensure correct operation of the EDK.

Jumper	Function	Setting 1-2	Setting 2-3
CJ 5-A Default 2-3	User Mode Setting Bit 0	MD0 pulled High	**MD0 pulled Low**
CJ 5-B Default 2-3	User Mode Setting Bit 1	MD1 pulled High	**MD1 pulled Low**
CJ 5-C Default 1-2	User Mode Setting Bit 2	**MD2 pulled High**	MD2 pulled Low
CJ 5-D Default 1-2	User Mode Setting Bit 3	MD3 pulled High	**MD3 pulled Low**

TABLE 5-1: USER MODE: JUMPER SETTINGS (DEFAULT SETTINGS IN BOLD)

The default settings indicated in bold text place the microcontroller into Mode 4.

5.3. EDK OPTIONS – CJ4

The EDK options provide access to commonly used features of the EDK range.

These jumpers must be fitted at all times to ensure correct operation of the EDK.

Jumper	Function	Setting 1-2	Setting 2-3
CJ 4-A Default 2-3	Serial Receive Source	Enables the RS232 receive signal. The Flash Programming Header* must not be used in this state.	**Disables the RS232 receive signal to enable the use of the Flash Programming Header**
CJ 4-B Default 2-3	User Programming Mode	Enables the Flash write hardware protection. The flash cannot be overwritten in User Mode.	**Disables the Flash write hardware protection.The flash can be overwritten in User Mode.**
CJ 4-C Default 1-2	CSn	**SRAM device enabled: Device selected by microcontroller.** **(DEFAULT)**	SRAM device Disabled: Device permanently de-selected.
CJ 4-D	**Not Used**	**Not Used**	**Not Used**

TABLE 5-2: BOARD OPTION: JUMPER SETTINGS (DEFAULT SETTINGS IN BOLD)

*See section 5.5

The following table lists the connections to each jumper pin.

Pin	Net Name	Description
1	UVCC	Microcontroller Supply Voltage
2	RXDISn	Disable Flash Header functions. Pulled low. (Enables RX232)
3	No Connection	No Connection
4	UVCC	Microcontroller Supply Voltage
5	UPM	CPLD Controlled option to set Flash Write (FW). Pulled low.
6	No Connection	No Connection
7	PG0	Chip Select 0 on H8S/2676
8	CSn	Chip Select signal connected to SRAM Chip Select
9	No Connection	No Connection
10	No Connection	No Connection
11	No Connection	No Connection
12	No Connection	No Connection

5.4. SERIAL PORT SELECTION

The programming serial port is connected to the RS232 connector by default. This allows direct programming of the EDK using the supplied software tools. A secondary serial port is available on the microcontroller and can be connected to the RS232 connector by changing some board option links. The additional port option allows the user to write messages or connect to other devices via the serial port while programming support is provided by the Flash programming header.

The following surface mount, zero-ohm link settings are fitted by default and connect the RS232 header to the programming serial port of the microcontroller.

Zero-ohm Link ID	Default	Function	Microcontroller Port Pin
CR20	Fitted	Transmit data from EDK	P31
CR23	Fitted	Receive data to EDK	P33
CR19	Not Fitted	Alternate Transmit data from EDK	P50
CR22	Not Fitted	Alternate Receive data to EDK	P51

TABLE 5-3: OPTION LINKS – DEFAULT SETTINGS

To enable the use of this alternate port the user must change the settings to those in the following table.

Zero-ohm Link ID	Default	Function	Microcontroller Port Pin
CR20	Not Fitted	Transmit data from EDK	P31
CR23	Not Fitted	Receive data to EDK	P33
CR19	Fitted	Alternate Transmit data from EDK	P50
CR22	Fitted	Alternate Receive data to EDK	P51

TABLE 5-4: OPTION LINKS – ALTERNATE SERIAL PORT

The user may implement a handshaking protocol on the EDK. This is not supported with the software tools supplied. To support this option two spare port pins have been allocated on the microcontroller. Using these port pins the CTS and RTS lines of the host serial interface can be controlled.

The user may also control the operation of the board via the same handshaking lines. This is not supported with the software tools supplied but may be written by the user. Using the CTS line the user may simulate pressing the boot button, see section:5.7. This will cause the EDK to swap into and out of Boot mode on each low-level activation of CTS. Feedback of the current mode is provided on the RTS line. A high level indicates boot mode and a low level indicates user mode.

The following settings are made by default, and ensure that there are no conflicts on unnecessary microcontroller pins.

Zero-ohm Link ID	Default	Function	Microcontroller Port Pin
CR12	Not Fitted	Mode State out from EDK	N/A (From CPLD*)
CR7	Not Fitted	Change Mode request to EDK	N/A (From CPLD*)
CR16	Not Fitted	Alternate RTS232 – Ready to send – from EDK	P81
CR13	Not Fitted	Alternate CTS232 – Clear to send – to EDK	P80

TABLE 5-5: OPTION LINKS – SERIAL PORT CONTROL

* See section 5.7

Note: These setting pairs are exclusive:
If CR12 and CR7 are fitted; CR16 and CR13 must not be fitted.
If CR16 and CR13 are fitted; CR12 and CR7 must not be fitted.

5.5. FLASH PROGRAMMING HEADER

The Flash Programming header is used with the Renesas Flash Debug Module (FDM). The FDM is a USB based programming tool for control and programming of Renesas microcontrollers, available separately from Renesas. This header provides direct access for the FDB to control the EDK microcontroller.

To utilise this header the user must make the following changes to the board configuration.

1. Disable the RX232 signal from the RS232 transceiver.
   Jumper link CJ4-A is provided for this purpose. Please refer to section 5.3.
2. Enable User Program Mode using jumper CJ4-B. Please refer to section 5.3.

Caution: Do not operate the board with the user mode jumpers removed and the FDB disconnected, as the microcontroller mode pins will float to an indeterminate state. This may damage the microcontroller device.

5.6. EXTERNAL DEBUG HEADER

This EDK does not include support for an external debugger

5.7. BOOT CONTROL

The method for placing the microcontroller device in to Boot mode for reprogramming has been incorporated into a complex programmable logic device (CPLD). This is not necessary for most user designs but allows a measure of increased flexibility for the EDK designs. Mode transitions including boot mode transitions only require the reset to be held active while the mode settings are presented. On releasing reset the microcontroller will be in the required mode.

The logic design detects a power up event and provides a timed reset pulse to guarantee the reset of the device. At the end of the rest pulse the processor will be placed in user mode and any code in the device will execute.

During user mode the NMI button can be pressed at any time. This will provide a single de-bounced NMI interrupt to the device.

Pressing the boot button will cause the boot mode controller to reset the device and, during the reset period, present the required mode settings to start the device in boot mode. At the end of the reset period the boot mode settings will have been latched into the device, which will then be ready to accept a boot mode connection via the RS232 interface or the flash programming header. Pressing the boot button during a normal reset will not cause the EDK to enter boot mode.

The boot mode settings are fixed at mode 11. The required mode settings are made using a tri-state capable buffer.

Note: The boot control device is programmed to support all possible EDK products.
For this reason the reset pulse is over 500ms. Repetitive activation of either the Boot or Reset buttons will restart the reset timer and extend the reset period. Pressing the boot button within the 500mS period of a reset will not cause the board to enter boot mode.

5.7.1. CPLD CODE

The code is based upon a four state machine providing a guaranteed reset period, which can be extended by holding the relevant control input in the active state. When released the timer will extend the reset for approximately 500mS.

The states are split into two functions, one for User mode and one for Boot mode. The first state of each is used to hold the reset line active. When the timer expires then the second state is used to hold the device in the selected mode and wait for an external control signal to either move back into the user reset state or into the boot reset state.

5.7.2. STATE DIAGRAM

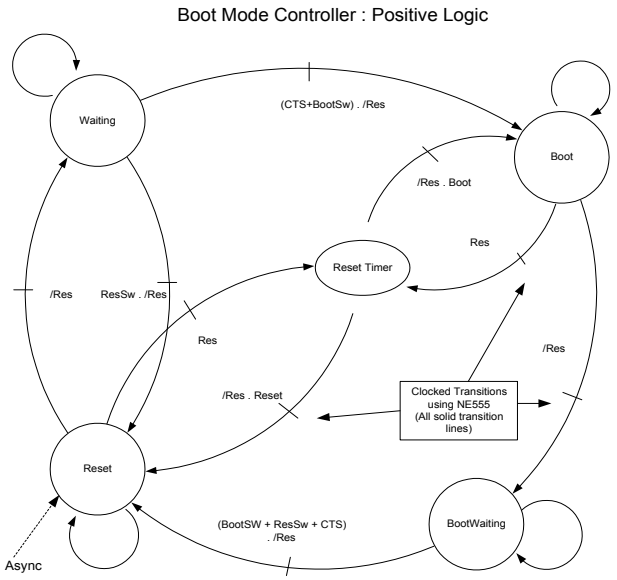


FIGURE 5-2: CPLD STATE DIAGRAM

6. MICROCONTROLLER HEADER CONNECTIONS

The following table lists the connections to each of the headers on the board.

6.1. HEADER J1

J1							
Pin No	**Function**	**EDK Symbol**	**Device pin**	**Pin No**	**Function**	**EDK Symbol**	**Device pin**
1	PF7/φ	PF7	95	2	VCC	UVCC	96
3	RESn	RESn	93	4	PLLVCC	NC_J1_04	94
5	PF6/Asn	PF6	91	6	PLLVSS	NC_J1_06	92
7	PF4/HWRn	PF4	89	8	PF5/RDn	PF5	90
9	PF2/LCASn/IRQ15n	PF2	87	10	PF3/LWRn	PF3	88
11	PF0/WAITn	PF0	85	12	PF1/UCASn/IRQ14n	PF1	86
13	P64/TMO0/DACK0n/IRQ12n	P64	83	14	P65/TM01/DACK1n/IRQ13n	P65	84
15	P62/TMCI0/TEND0n/IRQ10n	P62	81	16	P63/TMCI1/TEND1n/IRQ11n	P63	82
17	PD1/D9	PD1	79	18	PD0/D8	PD0	80
19	PD3/D11	PD3	77	20	PD2/D10	PD2	78
21	PD4/D12	PD4	75	22	VSS	GND	76
23	PD6/D14	PD6	73	24	PD5/D13	PD5	74
25	PE0/D0	PE0	71	26	PD7/D15	PD7	72
27	PE2/D2	PE2	69	28	PE1/D1	PE1	70
29	VCC	UVCC	67	30	PE3/D3	PE3	68
31	PE5/D5	PE5	65	32	PE4/D4	PE4	66
33	PE7/D7	PE7	63	34	PE6/D6	PE6	64
35	P61/TMRI1/DREQ1n/IRQ9n	P61	61	36	FWE	FW	62
37	P27/PO7/TIOCB5/EDRAK1n /IRQ15n	ULED2	59	38	P60/TMRI0/DREQ0n/IRQ8n	P60	60
39	P25/PO5/TIOCB4/IRQ13n	P25	57	40	P26/PO6/TIOCA5/EDRAK0n/IRQ14n	ULED1	58
41	P23/PO3/TIOCD3/IRQ11n	P23	55	42	P24/PO4/TIOCA4/IRQ12n	P24	56
43	P21/PO1/TIOCB3/IRQ9n	P21	53	44	P22/PO2/TIOCC3/IRQ10n	P22	54
45	P17/PO15/TIOCB2/TCLKD /EDRACK3n	P17	51	46	P20/PO0/TIOCA3/IRQ8n	P20	52
47	P15/PO13/TIOCB1/TCLKC	P15	49	48	P16/PO14/TIOCA2/EDRAK2n	P16	50
49	VSS	GND	47	50	P14/PO12/TIOCA1	P14	48
51	P12/PO10/TIOCC0/TCLKA	P12	45	52	P13/PO11/TIOCD0/TCLKB	P13	46
53	P10/P08/TIOCA0	P10	43	54	P11/PO9/TIOCB0	P11	44
55	P74/EDACK0n/ DACK0n	P74	41	56	P75/EDACK1n/DACK1n	P75	42
57	VCC	UVCC	39	58	P73/ETEND1n/TEND1n	P73	40
59	WDTOVFn	WDTOVFn	37	60	NMI	NMIn	38
61	P71/EDREQ1n/DREQ1n	P71	35	62	P72/ETEND0n/TEND0n	P72	36
63	NC	NC_J1_63	33	64	P70/EDREQ0n/DREQ0n	P70	34
65	PA6/A22	PA6	31	66	PA7/A23	PA7	32
67	PA4/A20	PA4	29	68	PA5/A21	PA5	30
69	PA2/A18	PA2	27	70	PA3/A19	PA3	28
71	PA1/A17	PA1	25	72	VSS	GND	26

6.2. HEADER J2

J2							
Pin No	**Function**	**EDK Symbol**	**Device pin**	**Pin No**	**Function**	**EDK Symbol**	**Device pin**
1	EXTAL	CON_EXTAL	97	2	XTAL	CON_XTAL	98
3	VSS	GND	99	4	STBYn	STBYn	100
5	PG0/CS0n	PG0	101	6	PG1/CS1n	PG1	102
7	PG2/CS2n	PG2	103	8	PG3/CS3n	PG3	104
9	PH0/CS4n	PH0	105	10	PH1/CS5n	PH1	106
11	P50/TxD2/IRQ0n	DTXD	107	12	P51/RxD2/IRQ1n	DRXD	108
13	P52/SCK2/IRQ2n	P52	109	14	P53/ADTRGn/IRQ3n	P53	110
15	PH2/CS6n/IRQ6n	PH2	111	16	PH3/CS7n/OEn/IRQ7n	PH3	112
17	PG4/BREQ0n	PG4	113	18	PG5/BACKn	PG5	114
19	PG6/BREQn	PG6	115	20	VCC	UVCC	116
21	P40/AN0	P40	117	22	P41/AN1	P41	118
23	P42/AN2	P42	119	24	P43/AN3	P43	120
25	VREF	VREF	121	26	AVCC	AVCC	122
27	P44/AN4	P44	123	28	P45/AN5	P45	124
29	P46/AN6/DA0	P46	125	30	P47/AN7/DA1	P47	126
31	P54/AN12/IRQ4n	P54	127	32	P55/AN13/IRQ5n	P55	128
33	P56/AN14/DA2/IRQ6n	P56	129	34	P57/AN15/DA3/IRQ7n	P57	130
35	AVSS	AVSS	131	36	NC	NC_J2_36	132
37	P35/SCK1/OEn	PSCK	133	38	P34/SCK0	P34	134
39	P33/RxD1	PRXD	135	40	VSS	GND	136
41	P32/RxD0/IrRxD	P32	137	42	P31/TxD1	PTXD	138
43	P30/TxD0/IrTxD	P30	139	44	P80/EDREQ2n/IRQ0n	DCTS	140
45	P81/EDREQ3n/IRQ1n	DRTS	141	46	P82/ETEND2n/IRQ2n	P82	142
47	MD0	MD0	143	48	MD1	MD1	144
49	MD2	MD2	1	50	P83/ETEND3n/IRQ3n	P83	2
51	P84/EDACK2n/IRQ4n	P84	3	52	P85/EDACK3n/IRQ5n	P85	4
53	VCC	UVCC	5	54	PC0/A0	PC0	6
55	PC1/A1	PC1	7	56	PC2/A2	PC2	8
57	PC3/A3	PC3	9	58	PC4/A4	PC4	10
59	PC5/A5	PC5	11	60	VSS	GND	12
61	PC6/A6	PC6	13	62	PC7/A7	PC7	14
63	PB0/A8	PB0	15	64	PB1/A9	PB1	16
65	PB2/A10	PB2	17	66	PB3/A11	PB3	18
67	VSS	GND	19	68	PB4/A12	PB4	20
69	PB5/A13	PB5	21	70	PB6/A14	PB6	22
71	PB7/A15	PB7	23	72	PA0/A16	PA0	24

7. CODE DEVELOPMENT

7.1. HMON

7.1.1. MODE SUPPORT

The HMON library is built to support Advanced Expanded Mode only.

7.1.2. BREAKPOINT SUPPORT

Code located in RAM may have multiple breakpoints limited only by the size of the On-Chip RAM.

7.1.2.1. CODE LOCATED IN FLASH / ROM

Breakpoints cannot be set in FLASH areas as the device does not have a break controller.

7.1.2.2. CODE LOCATED IN RAM

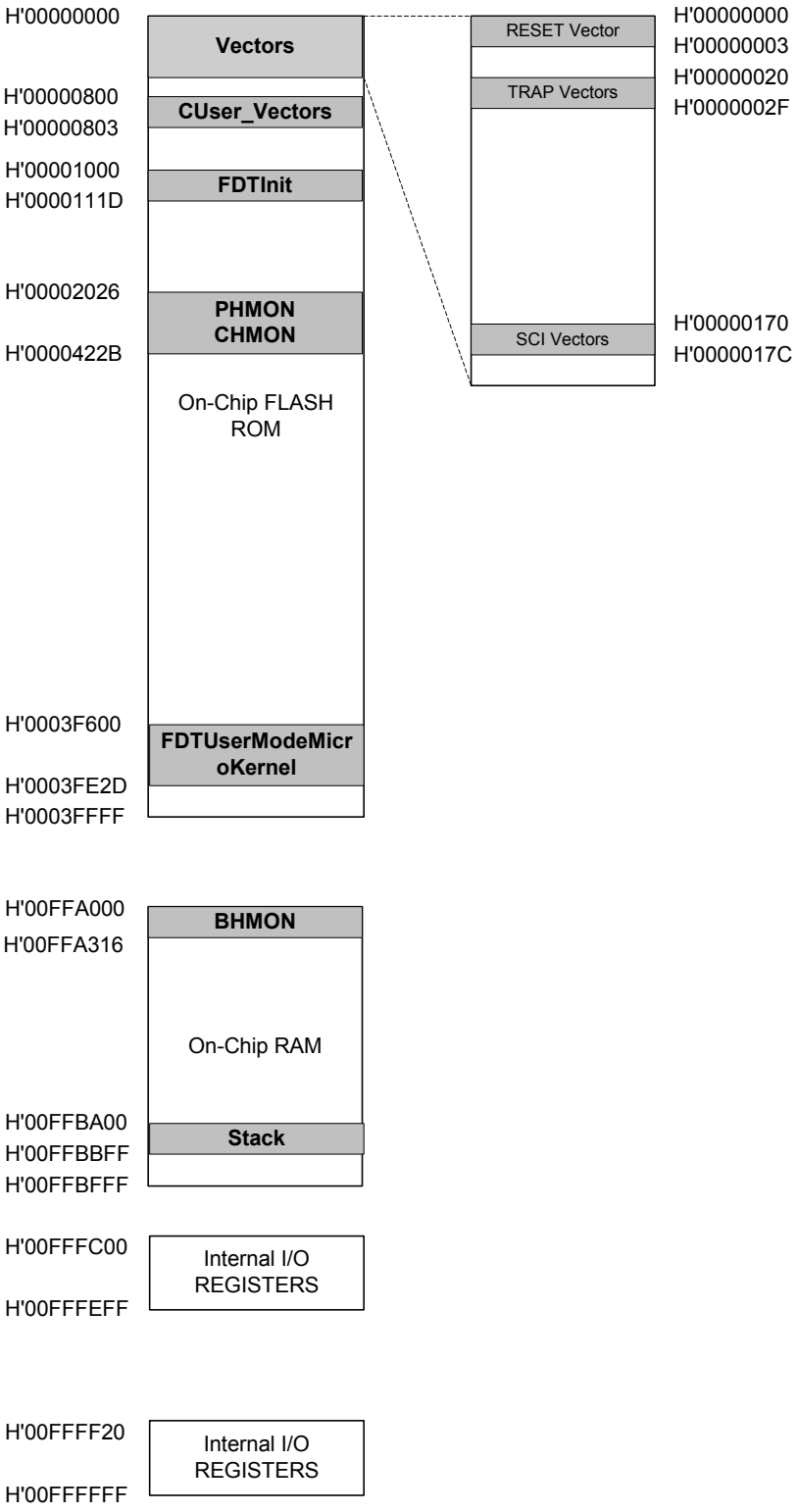
Double clicking in the breakpoint column in the code sets the breakpoint. Breakpoints will remain unless they are double clicked to remove them.

7.1.3. HMON CODE SIZE

HMON is built along with the debug code. Certain elements of the HMON code must remain at a fixed location in memory. The following table details the HMON components and their size and location in memory. For more information, refer to the map file when building code.

Section	Description	Start Location	Size (H'bytes)
RESET_VECTOR	HMON Reset Vector (Vector 0) Required for Startup of HMON	H' 00000000	4
TRAP_VECTORS	Trap Vectors (Vector 8, 9, 10, 11) Required by HMON to create Trap Breakpoints in RAM	H' 00000020	10
SCI_VECTORS	HMON Serial Port Vectors (Vector 80, 81, 82, 83) Used by HMON when EDK is configured to connect to the default serial port.	H' 00000170	C
PHMON	HMON Code	H' 00002026	20C6
CHMON	HMON Constant Data	H' 000040EC	140
BHMON	HMON Uninitialised data	H' 00FFA000	317
FDTInit	FDT User Mode Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 00001000	11E
FDTUserModeMicroKernel	FDT User Mode Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 0003F600	82E
CUser_Vectors	Pointer used by HMON to point to the start of user code.	H' 00000800	4

7.1.4. MEMORY MAP



7.1.5. BAUD RATE SETTING

HMON has initially set to connect at 115200Baud. Should the user wish to change this, the value for the BRR in HMONserialconfiguser.c will need to be changed and the project re-built. Please refer to the HMON User Manual for further information.

7.1.6. INTERRUPT MASK SECTIONS

HMON has an interrupt priority of 6. The serial port has an interrupt priority of 7. Modules using interrupts should be set to lower than this value (6 or below), so that serial communications and debugging capability is maintained.

7.2. ADDITIONAL INFORMATION

For details on how to use High-performance Embedded Workshop (HEW), with HMON, refer to the HEW manual available on the CD or from the web site.

For information about the H8S/2676 series microcontrollers refer to the H8S/2676 *Series Hardware Manual*

For information about the H8S/2676 assembly language, refer to the H8S *Series Programming Manual*

Further information available for this product can be found on the Renesas web site at:

http://www.eu.renesas.com/tools

General information on Renesas Microcontrollers can be found at the following URL.

Global: http://www.renesas.com/