EDK3687

USER MANUAL

FOR H8/3687
ON-CHIP FLASH MICROCONTROLLER

Preface

Cautions

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Document Information

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1. TABLE OF CONTENTS

2. START-UP INSTRUCTIONS

2.1. INSTALLING THE EVALUATION DEVELOPMENT KIT (EDK)

Please refer to the quick start guide provided for initial installation of the EDK.

A copy of the quick start guide and other information relating to this EDK at:

http://www.eu.renesas.com/tools

Installing the EDK requires power and serial connection to a host computer.

2.2. SERIAL CONNECTION

The serial communications cable for connecting the EDK to a host computer requires 1:1 connectivity.

Figure 2-1 shows how to connect the EDK to a PC or notebook computer equipped with a nine pin D connector.

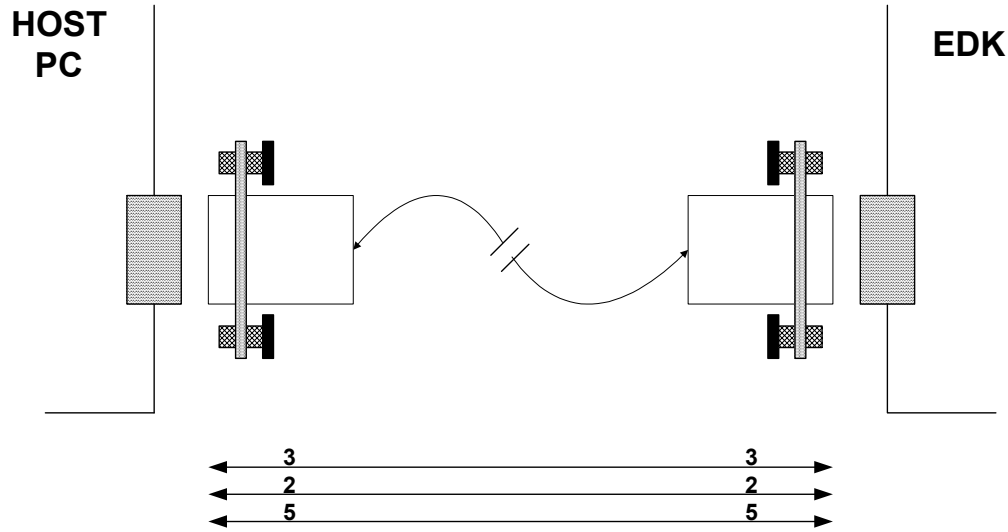


FIGURE 2-1: SERIAL CONNECTION TO PC/NOTEBOOK WITH DB-9 CONNECTOR (SUPPLIED)

2.3. POWER SUPPLY

The EDK hardware requires a power supply of +5V. Since total power consumption can vary widely due to external connections, port states, and memory configuration, use a power supply capable of providing at least 500mA at +5V DC ± 5%.

The design is specified for evaluation of the microcontroller and so does not include circuitry for supply filtering/noise reduction, under voltage protection, over current protection or reversed polarity protection. Caution should be used when selecting and using a power supply.

The power connector on the EDK is a 2.5mm Barrel connector. The center pin is the positive connection.

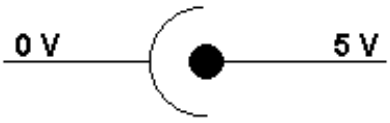


FIGURE 2-2: POWER SUPPLY CONNECTION

Caution: Existing customers using E6000 products note that the polarity of this board is opposite to that for the E6000. Use of the E6000 power supply with this board will damage both board and power supply.

3. EDK BOARD LAYOUT

The diagram shows a general layout of the EDK board.

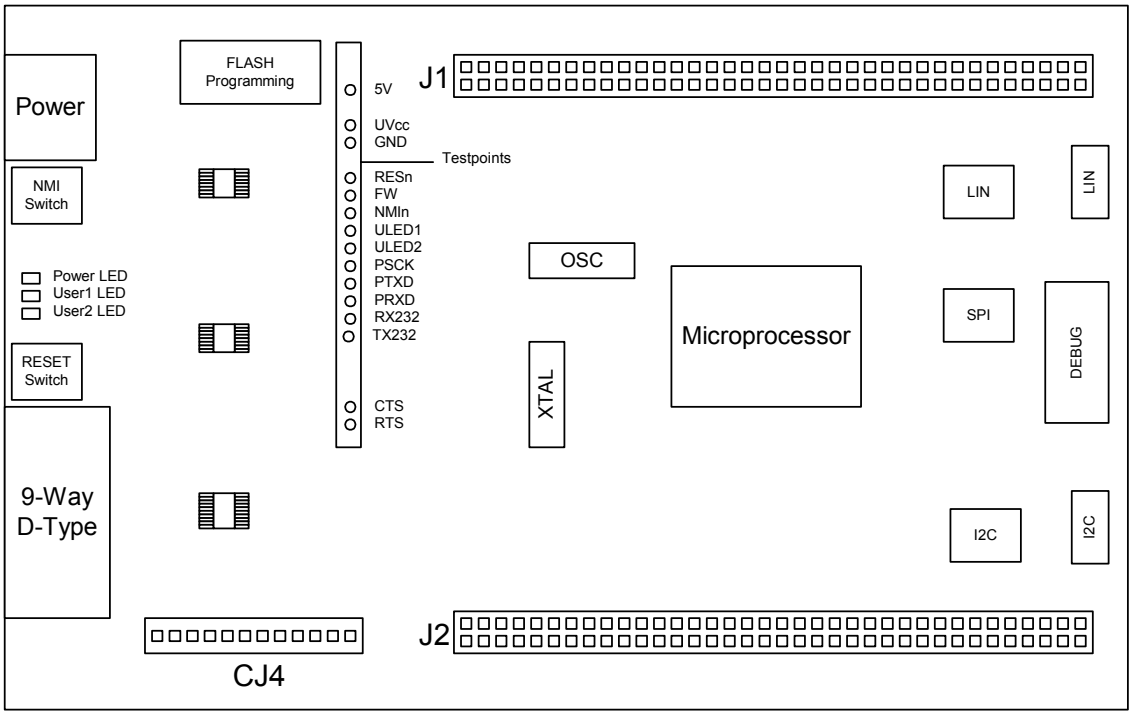


FIGURE 3-1: EDK BOARD LAYOUT

3.1. EDK BLOCK DIAGRAM

The diagram shows the connectivity of the components on the EDK board.

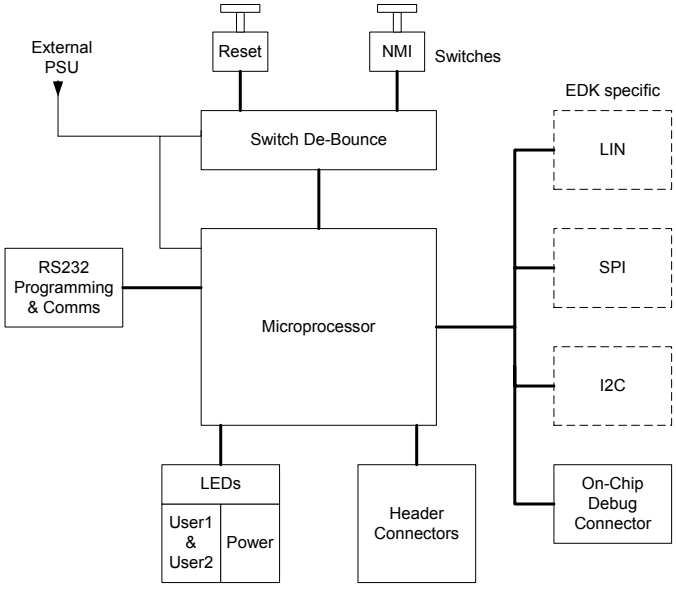


FIGURE 3-2: EDK BLOCK DIAGRAM

4. EDK OPERATION

4.1. USER INTERFACE

The EDK provides two buttons for influencing the operation of the board. The purpose of each button is clearly marked next to it. Refer to the board layout for positions (Section 3)

1. Reset Switch

This button provides the microcontroller with a reset pulse utilizing the built in power on reset control of the device.

2. NMI Switch

This button provides a de-bounced signal to the microcontroller for each operation of the button. There is no maximum activation time for this button.

4.2. SERIAL INTERFACE

The serial port on the microcontroller directly supports three wire serial interfaces. Options are provided on the board for the user to write handshaking routines using standard port pins.

4.2.1. CONNECTOR PIN DEFINITIONS

The EDK RS232 interface conforms to Data Communication Equipment (DCE) format allowing the use of 1-1 cables when connected to Data Terminal Equipment (DTE) such as an IBM PC. The cable used to connect to the EDK will affect the available board options. A fully wired cable can allow handshaking between the microcontroller and the host PC, subject to setting the board options and the availability of suitable host software. Handshaking is not supported as standard on the microcontroller so for normal use a minimal three-wire cable can be used. The minimum connections are unshaded in the following table.

EDK DB9 Connector Pin	Signal	Host DB9 Connector Pin
1	No Connection	1
2	EDK Tx Host Rx	2
3	EDK Rx Host Tx	3
4	No Connection	4
5	Ground	5
6	No Connection	6
7	EDK CTS Host RTS	7
8	EDK RTS Host CTS	8
9	No Connection	9

TABLE 4-1: RS232 INTERFACE CONNECTIONS

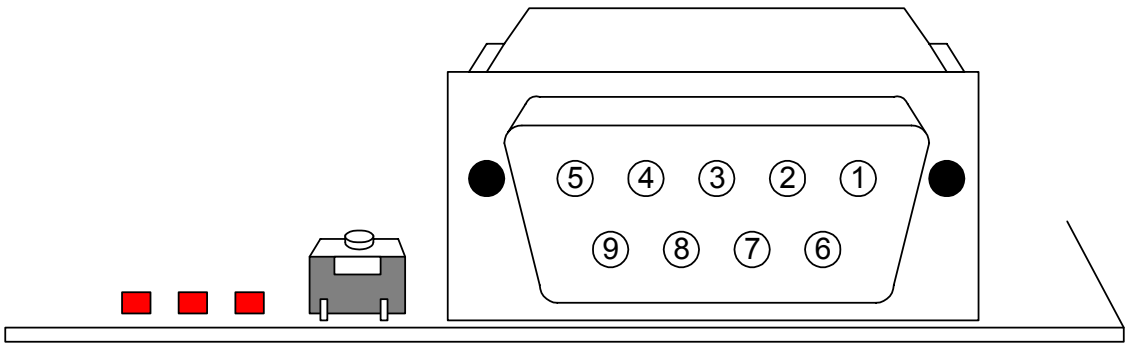


FIGURE 4-1: EDK SERIAL PORT PIN NUMBERING

4.2.2. CRYSTAL CHOICE

The operating crystal frequency has been chosen to support the fastest operation with the fastest serial operating speeds. The value of the crystal is 18.432MHz.

The following table shows the baud rates and Baud Rate Register (BRR) setting required for each communication rate using the above default operating speed. It also confirms the resultant baud rate and the bit error rate that can be expected.

Baud Rate Register Settings for Serial Communication Rates												
SMR Setting:	0			1			2			3		
Comm. Baud	BRR setting	Actual Rate	ERR (%)	BRR setting	Actual Rate	ERR (%)	BRR setting	Actual Rate	ERR (%)	BRR setting	Actual Rate	ERR (%)
110	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	81	110	-0.22
300	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	119	300	0.00	29	300	0.00
1200	Invalid	Invalid	Invalid	119	1200	0.00	29	1200	0.00	7	1125	-6.25
2400	239	2400	0.00	59	2400	0.00	14	2400	0.00	3	2250	-6.25
4800	119	4800	0.00	29	4800	0.00	7	4500	-6.25	1	4500	-6.25
9600	59	9600	0.00	14	9600	0.00	3	9000	-6.25	Invalid	Invalid	Invalid
19200	29	19200	0.00	7	18000	-6.25	1	18000	-6.25	Invalid	Invalid	Invalid
38400	14	38400	0.00	3	36000	-6.25	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
57600	9	57600	0.00	2	48000	-16.67	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
115200	4	115200	0.00	0	144000	25.00	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
230400*	2	192000	-16.67	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
460800*	0	576000	25.00	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid

TABLE 4-2 CRYSTAL FREQUENCIES FOR RS232 COMMUNICATION

** Note: The device used to convert the RS232 serial information to logic signals for the microcontroller is limited to 120kBaud. The rates above this level can only be utilised if the user provides direct logic level communications.*

The user may replace the HC49/U surface mounted AT cut crystal with another of similar type within the operating frequency of the microcontroller device. Please refer to the hardware manual for the microcontroller for the valid operating range.

Alternatively the user may fit an oscillator module – or provide an external clock source. When providing an oscillator module or external source it is highly recommended that the load capacitors for the AT crystal are removed from the PCB. These are physically placed within the PCB outline of the oscillator module for easy location and to ensure they are removed when using this option.

When changing the crystal frequency the pre-loaded debugging monitor will not function. In this situation the user is responsible for providing code to evaluate the device away from the default operating speed.

4.2.3. REMOVABLE COMPONENT INFORMATION.

This information is provided to allow the replacement of components removed from the board as described in section 4.2.2.

Component	Cct. Ref	Value	Rating	Manufacturer
Load Resistor (X2)	R8	1MΩ	0805 1%	Welwyn WCR Series
Load Resistor (X3)	R7	1MΩ	0805 1%	Welwyn WCR Series
Load capacitors (X2)	C2,C3	12pF	0603 10% 25V	AVX 0603 3 A 150 KAT
Load capacitors (X3)	C4,C5	15pF	0603 10% 25V	AVX 0603 3 A 150 KAT

TABLE 4-3: REMOVABLE COMPONENT INFORMATION

Care must be taken not to damage the tracking around these components. Only use soldering equipment designed for surface mount assembly and rework.

4.3. SPI EEPROM

The board has been tested with an Atmel AT25040N-10SA-2.7 SPI EEPROM device (Not supplied).

The device should be connected to P30, P31, P32 and P67 using 0R links on R15, R16, R17 and R21. Alternative connections are available, refer to section 5.3 for more information.

Do not fit the CAN transceiver if the SPI device is fitted while using the settings above.

4.4. I2C EEPROM

The board has been tested with an Atmel AT24C04AN-10SI-2.7 I2C EEPROM device (Not supplied).

The device is configured to connect to dedicated I2C pins on Ports P56 and P57.

4.5. LIN INTERFACE

The board has been tested with an Philips TJA1020TD device (Not supplied).

The device should be connected to P71 and P72 using 0R links on R29 and R31. Alternative connections are available; refer to section 5.3 for more information.

The links R41, R45 and R47 need to be carefully considered before fitting. Damage to the device, board or connected equipment may occur if these links are fitted inappropriately. Please review the specifications for the LIN transceiver and LIN Interface before fitting any of these links.

4.6. LEDS

The EDK has three red LEDs. The function of each LED is clearly marked on the silk screen of the PCB. Please refer to the board layout diagram for position information (Section 3).

When the board is connected to a power source the Power (PWR) led will illuminate.

There are two LEDs dedicated for user control these are marked USR1 and USR2. Each LED will illuminate when the port pin is in a logical low state.

The user LEDs are connected to the following ports:

LED Identifier	Port Pin	Microcontroller Pin	Pin Functions on Port Pin
USR1	P64	37	FTIOA1
USR2	P65	38	FTIOB1

TABLE 4-4: LED PORT CONNECTIONS

5. BOARD OPTIONS

The EDK has a number of configuration settings set by four jumpers CJ4 (A, B, C, D) and zero-ohm links. Common EDK functions can be set using the jumpers as described in sections 5.2. The additional zero-ohm links provide additional features that may be required to interface with other systems.

All the Jumper link settings are three pin options. There are four sets of options on each header.

The headers are numbered from 1 to 12 with pin 1 marked on the PCB by an arrow pointing to the pin. The diagram below shows the numbering of these jumper links and indicates jumpers fitted 1-2 for each three-pin jumper.

5.1. JUMPER LINKS

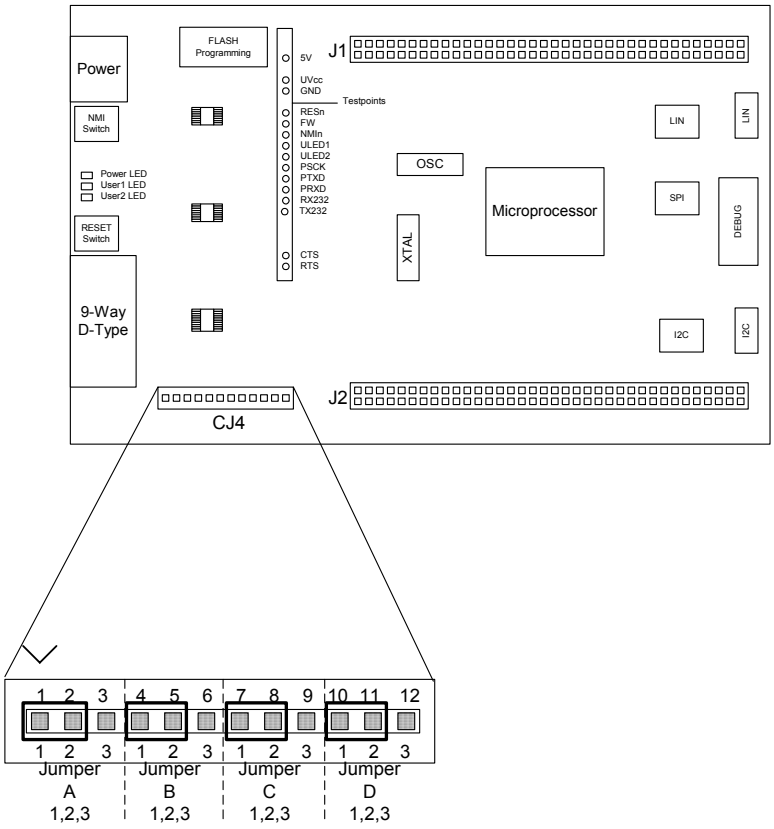


FIGURE 5-1: JUMPER CONFIGURATION

The following tables define each jumper and its settings.

5.2. EDK OPTIONS – CJ4

The EDK options provide access to commonly used features of the EDK range.

These jumpers must be fitted at all times to ensure correct operation of the EDK.

Jumper	Function	Setting 1-2	Setting 2-3
CJ 4-A Default 1-2	Serial Receive Source	**Routes the programming serial port to the 9Way D Connector**	Routes the programming serial port to the LIN Interface
CJ 4-B Default 1-2	Serial Transmit Destination	**Routes the programming serial port to the 9Way D Connector**	Routes the programming serial port to the LIN Interface
CJ 4-C Default 2-3	Serial Receive Source	Enable the Flash Programming header data receive	**Enable the RS232 interface data receive.**
CJ 4-D Default 1-2	BOOT Mode Selection	**User Mode**	BOOT Mode

TABLE 5-1: BOARD OPTION: JUMPER SETTINGS (DEFAULT SETTINGS IN BOLD)

*See section 5.4

The following table lists the connections to each jumper pin.

Pin	Net Name	Description
1	RX232	RS232 received data
2	RX_OPT	Link to below – Data from RS232 or LIN
3	LIN_RX	LIN received data
4	TX232	RS232 transmitter
5	PTXD	Data transmission
6	LIN_TX	LIN transmitter
7	RX_HDR	Flash Programming Header received data
8	PRXD	Data reception
9	RX_OPT	Link to above – Data from RS232 or LIN
10	NC	No Connection
11	NMIn	NMI used for BOOT mode selection
12	GROUND	System Ground

5.3. OPTION LINK SELECTION

The following sections show the option links that apply to each peripheral device. The tables all use the same key of symbols which is given below:

X – Groups of options one set of which must be fitted for correct operation of the EDK.

O – Groups of options which if fitted must be connected in the groups as shown by the table row.

S – Optional selection that will enable or disable specific device functions as listed.

! – Options which when incorrectly fitted may damage the board or attached devices.

5.3.1. RST – RESET FUNCTION

The HD643687GFP device includes a built in reset control circuit.

		CR2	CR3	CR4	CR8	CR9	CR10	
RST	Internal	X		X				Default
	External		X		X	X	X	

TABLE 5-2: OPTION LINKS

The alternate settings can be fitted without damage to the device.

5.3.2. LIN – LIN INTERFACE

The LIN interface is not fitted by default. The transceiver can be connected to two groups of pins. The SCI2 (56,57,58) pins are shared with the CAN transceiver, do not use this selection when the CAN transceiver is fitted.

		SCI2 48,49,50	SCI2 56,57,58	R12	R27	R26	R29	R30	R31	R32	R41	R45	R46	R47	
LIN	SCI	O					O		O						Default
	SCI		O			O		O							
	NWAKE											!		!	
	NSLP			S											
	FTOA0									S					
	IRQ3n				S										
	MASTER												X		
	SLAVE												X		
	POWER										!				

TABLE 5-3: OPTION LINKS

5.3.3. SPI – SERIAL PERIPHERAL INTERFACE

The SPI interface is not directly compatible with the SCI interface on the device. Selection of the connections to the SPI interface should therefore be chosen to allow the operation of other peripherals as required.

			SCI2	SCI2	R	R	R	R	R	R	R	R	R	R	R	R	R
		SSU	48,49,50	56,57,58	15	16	17	18	19	20	21	22	23	24	25	35	37
SPI	SCI	X										O	O	O	O		
	SCI		X		O	O	O										
	SCI			X				O	O	O							
SPI	HOLDn																S
	WPn															S	
	CSn										X						

TABLE 5-4: OPTION LINKS

5.3.4. CAN – CONTROLLER AREA NETWORK

The CAN device, when fitted, is permanently connected to microcontroller pins 56 & 57. Other options share these pins so be sure that the alternate settings are made for the other peripheral options to avoid contentions on the board.

5.4. FLASH PROGRAMMING HEADER

The Flash Programming header is used with the Flash Debugging Module (FDM). The FDM is a USB based programming tool for control and programming of Renesas microcontrollers, available separately from Renesas. This header provides direct access for the FDM to control the EDK microcontroller.

To utilise this header the user must make the following changes to the board configuration.

1. Select the FDM header using CJ4-C as marked on the silk screen. Please refer to section 5.2.

5.5. EXTERNAL DEBUG HEADER

The External debug header may be used with the Renesas E10T Debugger, Renesas LEM Debugger or a third party debugger.

The E10T and LEM are on-chip debug emulators available separately from Renesas.

This header provides direct access for the debugger to control the EDK microcontroller.

5.6. BOOT CONTROL

The EDK provides a jumper selection to place the microcontroller device into boot mode. This jumper link grounds the NMI pin on the device.

Always remove the power from the EDK before moving this jumper to prevent unintended effects in the processor that may prevent the programming function from completing successfully.

6. MICROCONTROLLER HEADER CONNECTIONS

The following table lists the connections to each or the headers on the board.

6.1. HEADER J1

J1							
Pin No	**Function**	**EDK Symbol**	**Device pin**	**Pin No**	**Function**	**EDK Symbol**	**Device pin**
1	TEST	GND	8	2	RESn	RESn	7
3	VCL(No Connection)	NC3	6	4	X1	CON_X1	5
5	X2	CON_X2	4	6	AVCC	CON_AVCC	3
7	PB7/AN7	PB7	2	8	PB6/AN6	PB6	1
9	PB5/AN5	PB5	64	10	PB4/AN4	PB4	63
11	PB0/AN0	PB0	62	12	PB1/AN1	PB1	61
13	PB2/AN2	PB2	60	14	PB3/AN3	PB3	59
15	P30	P30	58	16	P31	P31	57
17	P32	P32	56	18	P33	P33	55
19	P17/IRQ3n/TRGV	P17	54	20	P16/IRQ2n	P16	53
21	P15/IRQ1n/TMIB1	P15	52	22	P14/IRQ0n	CTS	51
23	P72/TXD_2	P72	50	24	P71/RXD_2	P71	49
25	P70/SCK3_2	P70	48	26	P23	P23	47
27	P22/TXD	PTXD	46	28	P21/RXD	PRXD	45
29	P20/SCK3	PSCK	44	30	P87	P87	43
31	P86	P86	42	32	P85	P85	41

6.2. HEADER J2

J2							
Pin No	**Function**	**EDK Symbol**	**Device pin**	**Pin No**	**Function**	**EDK Symbol**	**Device pin**
1	VSS	GND	9	2	OSC2	CON_OSC2	10
3	OSC1	CON_OSC1	11	4	VCC	EVCC [1]	12
5	P50/WKP0n	P50	13	6	P51/WKP1n	P51	14
7	P34	P34	15	8	P35	P35	16
9	P36	P36	17	10	P37	P37	18
11	P52/WKP2n	P52	19	12	P53/WKP3n	P53	20
13	P54/WKP4n	P54	21	14	P55/WKP5n/ADTRGn	P55	22
15	P10/TMOW	P10	23	16	P11/PWM	P11	24
17	P12	P12	25	18	P56/SDA	P56	26
19	P57/SCL	P57	27	20	P74/TMRIV	P74	28
21	P75/TMCIV	P75	29	22	P76/TMOV	P76	30
23	P24	P24	31	24	P63/FTIOD0	P63	32
25	P62/FTIOC0	P62	33	26	P61/FTIOB0	P61	34
27	NMIn	NMIn	35	28	P60/FTIOA0	P60	36
29	P64/FTIOA1	ULED1	37	30	P65/FTIOB1	ULED2	38
31	P66/FTIOC1	RTS	39	32	P67/FTIOD1	P67	40

7. CODE DEVELOPMENT

7.1. HMON

7.1.1. MODE SUPPORT

The HMON library is built to support Normal Mode only.

7.1.2. BREAKPOINT SUPPORT

The monitor utilises the Address Break Controller for code located in ROM, allowing a single breakpoint to be set in the code. Code located in RAM may have multiple breakpoints limited only by the size of the On-Chip RAM.

Due to a limitation of the internal address break controller, a breakpoint set in ROM will execute the instruction at the breakpoint and stop on the subsequent op-code.

7.1.2.1. CODE LOCATED IN FLASH / ROM

Double clicking in the breakpoint column in the code sets the breakpoint. Adding a further breakpoint in the code removes the previous one. A warning message will be displayed in the message window when this occurs.

7.1.2.2. CODE LOCATED IN RAM

Double clicking in the breakpoint column in the code sets the breakpoint. Breakpoints will remain unless they are double clicked to remove them.

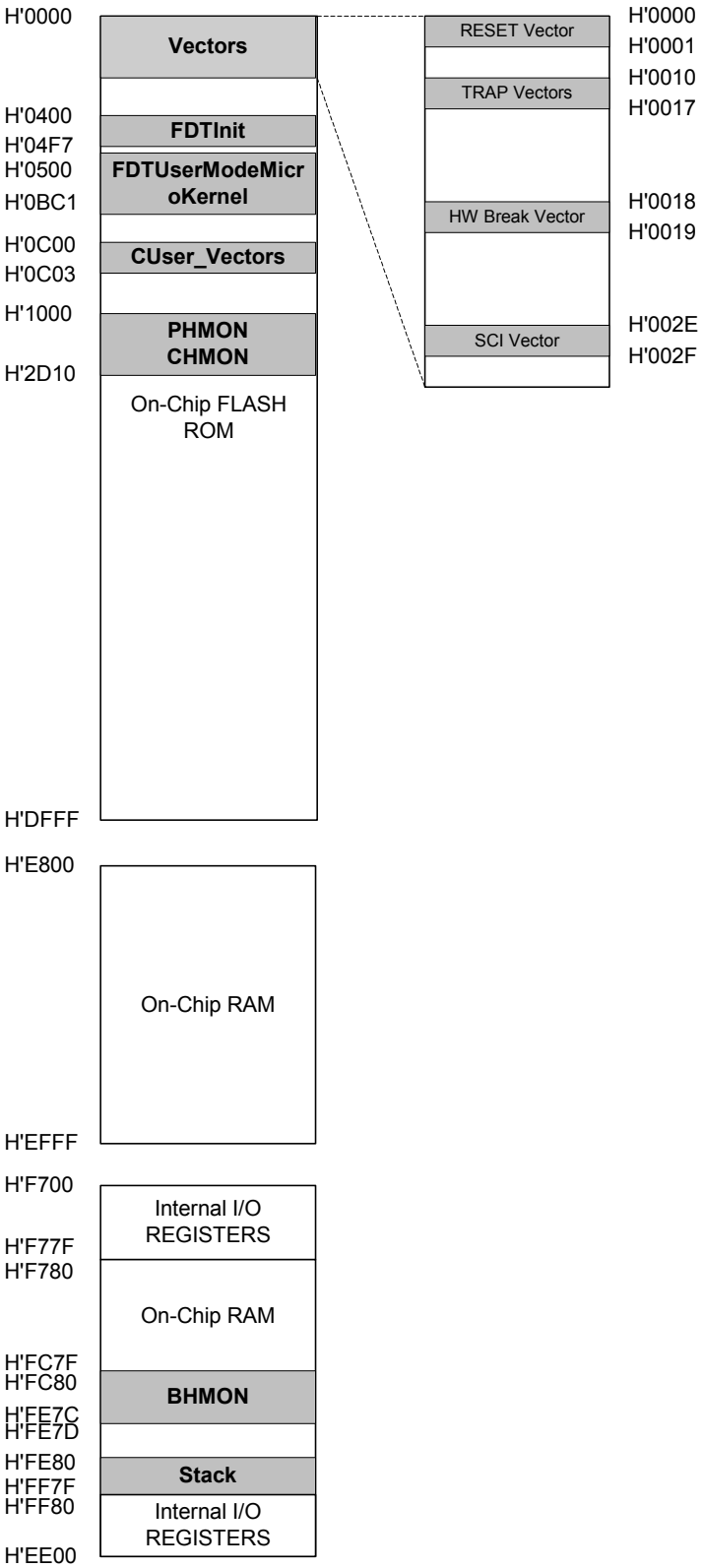
7.1.3. HMON CODE SIZE

HMON is built along with the debug code. Certain elements of the HMON code must remain at a fixed location in memory. The following table details the HMON components and their size and location in memory. For more information, refer to the map file when building code.

Section	Description	Start Location	Size (H'bytes)
RESET_VECTOR	HMON Reset Vector (Vector 0) Required for Startup of HMON	H' 0000	2
TRAP_VECTORS	Trap Vectors (Vector 8, 9, 10, 11) Required by HMON to create Trap Breakpoints in RAM	H' 0010	8
HW_BREAK_VECTORS	HMON Break Controller (Vector 12) Required by HMON to create Breakpoints in ROM	H' 0018	2
SCI_VECTOR	HMON Serial Port Vectors (Vector 23) Used by HMON when EDK is configured to connect to the default serial port.	H' 002E	2
PHMON	HMON Code	H' 1000	2C3D
CHMON	HMON Constant Data	H' 2C3E	2D10
BHMON	HMON Uninitialised data	H' FC80	1FD
FDTInit	FDT User Mode Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 0400	F7
FDTUserModeMicroKernel	FDT User Mode Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 0500	6CC
CUser_Vectors	Pointer used by HMON to point to the start of user code.	H' 0C00	4*

* CUserVectors is a long word location with the upper 16 bits set to zero.

7.1.4. MEMORY MAP



7.1.5. BAUD RATE SETTING

HMON has initially set to connect at 115200Baud. Should the user wish to change this, the value for the BRR in HMONserialconfiguser.c will need to be changed and the project re-built. Please refer to the HMON User Manual for further information.

7.1.6. INTERRUPT MASK SECTIONS

The EDK3687 has fixed interrupt priorities. The serial (SCI3)port interrupt is used by HMON. The Real Time clock, external interrupt and Timer V interrupts have a higher priority than the serial port. If these interrupts are used HMON may not function correctly.

7.2. ADDITIONAL INFORMATION

For details on how to use HEW, with HMON, `refer to the HEW manual available on the CD or from the web site.

For information about the H8/3687 series microcontrollers refer to the H8/3687 *Series Hardware Manual*

For information about the H8/300 assembly language, refer to the H8300 *Series Programming Manual*

Further information available for this product can be found on the Renesas web site at:

http://www.eu.renesas.com/tools

General information on Renesas microcontrollers can be found at the following URLs.

Global: http://www.renesas.com/