79EB351
Evaluation Board Manual

June 2003

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Description of IDT79EB351 Evaluation Board

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Introduction

The IDT79RC32351 is a high performance integrated processor that combines IDT's RISCore32300 CPU core with system logic to control memory, I/O, and various communications devices. It also includes on-chip peripherals such as DMA channels, reset circuitry, interrupts, timers, and UARTs. The RC32351 integrated processor is a complete CPU subsystem for embedded designs.

The IDT79EB351 Evaluation Board provides an RC32351 evaluation tool.This board is highly configurable and contains hardware options for various memory configurations.

Revision History

January 18, 2002: Initial publication.

June 9, 2003: Added Item #3 in Chapter 4.

Overview of Features

The 79EB351 Evaluation Board, illustrated in Figure 1.1, incorporates the following features:

- *RC32351 CPU*
- *EPROM 1 Mbyte*
- *Flash memory up to 8 Mbytes (depending on the word width)*
- *SRAM up to 1 Mbytes*
- *SDRAM SODIMM/DIMM up to XX Mbytes*
- *Ethernet controller 10/100Mbps*
- *ATM interface*
- *USB interface (Rev. 1.1 compliant)*
- *Two on chip serial I/O channels (16550 compatible UART)*
- *External 16550 compatible UART (2 channels)*
- *Real time clock with battery backup*
- *LCD display (2 lines by 16 characters)*

Explanation of Features

79EB351 Evaluation Board is a complete microcomputer system that is targeted as evaluation and software development platform for the RC32351 network processor.

The board requires an ATX compatible power supply and a CRT terminal for operation. The board has an EPROM memory with IDT/sim, a debugging monitor with code downloading capability. Capabilities of IDT/sim include single stepping, breakpoints, memory and register examination and change and symbolic assembler/disassembler. Complete description of IDT/sim is provided in a separate document.

Notes

Block Diagram

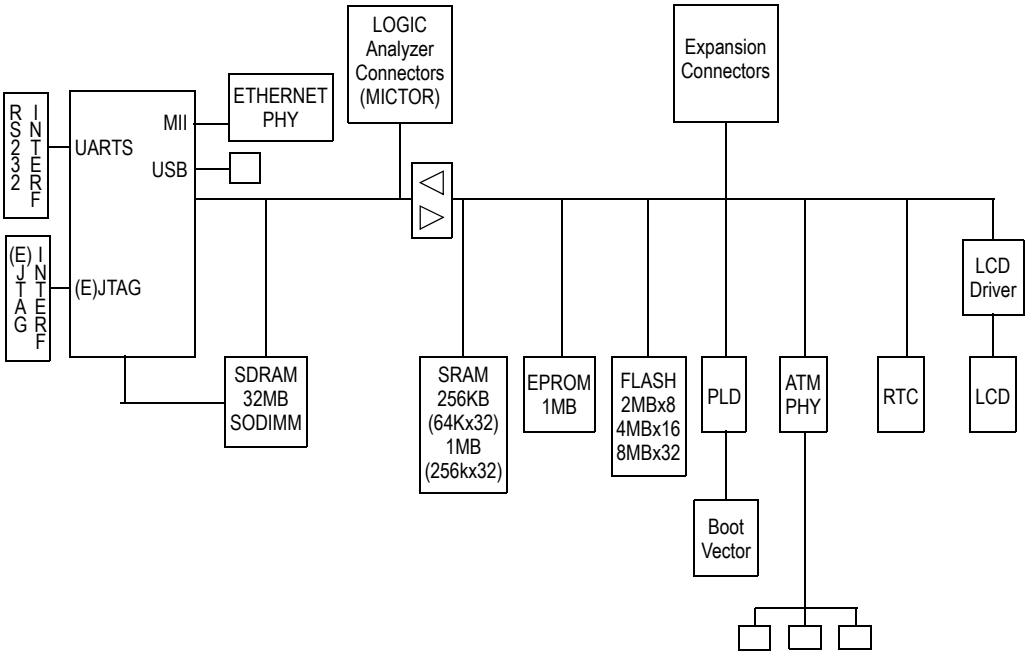


Figure 1.1 79EB351 Evaluation Board Block Diagram

Specification Summary

SDRAM

- *SODIMM (standard)*

EPROM

- *EPROM memory is 1Mx8*

FLASH

- *FLASH memory can be configured to be 8, 16 or 32 bits wide by populating U19, U19 and U18 or U19, U18, U21, U22 sockets. Flash boot width must be set by S4-1 and S4-2 switches. Flash memory used is 2Mx8, so memory capacity if flash is used is 2MB, 4MB or 8MB depending on the width.*

SRAM

- *Standard configuration is 64Kx32, but it is possible to install larger capacity memory chips to get 256Kx32.*

Ethernet

- *10/100 Mbps Ethernet interface with possibility of configuration*

Installation of 79EB351 Evaluation Board

Notes

79EB351 Installation

The primary installation steps are as follows:

1. Connecting a power source
   – *This involves connecting an external power supply to the board.*
2. Connecting a Video display terminal
   – *This involves connecting an RS232C serial cable from a video terminal to the board, through connector J1.*
3. Configuring jumper/switch options
   – *This involves altering CPU reset initialization mode vector, changing memory configuration, etc. The board is shipped with the jumpers set to the default configuration.*
4. Running software
   – *No additional software required.*
5. Booting IDT/SIM
   – *When power to the board is turned on, the board's IDT/SIM program boots and displays the start-up message.*

Getting Started Quickly

The 79EB351 board is shipped ready to run. Before the board is shipped, jumpers and switches are configured to the default settings, and generally they do not require further modification or set up.

Two basic requirements for the board to run are:

- *ATX power supply.*
- *CRT video terminal with an RS 232C port connected to J1.*

The board is designed to be used with ATX power supply which is supplied with the board. If the user wants to use another ATX power supply attention must be paid to the fact that the switch-mode power supply should be specified with the minimum current of 500mA or less on the 3.3V. Some of the (older) power supplies are specified for minimum current of 1A at +5V supply and these will not work with the evaluation board since power consumption for +5V is in the order of 50 mA. The ATX power connector is connected to the connector J21on the Eval Board.

Power Connector (J21)

PIN	SIGNAL	COLOR
1	+3.3V	ORANGE
2	+3.3V	ORANGE
3	COM	BLACK
4	+5VDC	RED
5	COM	BLACK
6	+5VDC	RED
7	COM	BLACK
8	PWR_OK	GRAY
9	+5VSB	PURPLE

Table 2.1 J21 Power Connectors (Part 1 of 2)

Notes

PIN	SIGNAL	COLOR
10	+12VDC	YELLOW
11	+3.3VDC (+3.3V default sense)	ORANGE (BROWN)
12	-12VDC	BLUE
13	COM	BLACK
14	PS_ON#	GREEN
15	COM	BLACK
16	COM	BLACK
17	COM	BLACK
18	-5VDC	WHITE
19	+5VDC	RED
20	+5VDC	RED

Table 2.1 J21 Power Connectors (Part 2 of 2)

The CRT video terminal can be a VT100 type/ANSI terminal or emulator running with 9600 baud, 8 data bits, no parity, and 1 stop bit. RS232C connector, on the eval. Board uses a male 9-pin DTE connector (J1) of which only the RX, TX, and GND pins are necessary.

Jumper and Switch Settings

The jumper and switch settings and their default are listed below.

Jumper Selection	Function	Default
W1, W2, W3, W4	Supply VDD_IO (3.3V) to the processor.	Closed
W5, W6, W7, W8	Supply VDD_CORE (2.5V) to the processor.	Closed
W10	EPROM/FLASH selection for system boot EPROM: jumper in CD position FLASH: jumper in BD position	CD
W14	Flash memory writing enable. AB write disabled. BC write enabled.	AB

Table 2.2 Jumper and Switch Settings

Notes

S1: DIP Switch 1

S1	Function			
2	Pause (Ethernet)	Pause		
3,4,5	Ethernet Configuration	Autonegotiaton.	Speed	Duplex
		000 Disabled	10	Half
		001 Disabled	10	Full
		010 Disabled	100	Half
		011 Disabled	100	Full
		100 Enabled	100	Half
		101 Enabled	100	Full
		110 Enabled	10/100	Half
		111 Enabled	10/100	Full/Half

Table 2.3 S1: DIP Switch 1

S1 is a SPDT switch. 0 means – position on the switch, 1 means + position.

S3 and S4: Boot vector selection

Selection of 79EB351 Mode Bits during Power-on/ Cold reset (reset initialization vector).

0 – ON (CLOSED)

1 – OFF (OPEN)

S3-1: 0 (Reserved)

S3-2: 1 (Reserved)

S3-3: CPU/DMA Status Mode Enable

0 GPIO pin 4 works as GPIO/alternate function

1 Multiplex CPU/DMA status (CPUP) onto this pin

S3-4: Multiplex JTAG Reset pin on GPIO pin 2

0 GPIO pin 2 operates as GPIO/alternate function pin

1 Multiplex JTAG reset onto GPIO pin 2

S3-5: Hold SYSCLKP constant

0 Do not hold SYSCLKP constant

1 Hold SYSCLKP constant.

S3-6: DMA Debug enable. 79RC32351 drives DMA channel number on GPIO[25,23,9,8].

0 Do not multiplex DMA debug pins on GPIO[8,9,25,23]

1 Multiplex DMA debug pins on GPIO[8,9,25,23]

S3-7: Fast Reset

0 Normal reset (RSTN pin is driven low for at least 4096 cycles)

1 Fast reset (RSTN pin is driven low for 64 cycles)

S3-8: ICE Interface Enable

0 Do not multiplex ICE pins on GPIO[31,13:10]

1 Multiplex ICE pins on GPIO[31,13:10]

Boot Prom Width

Boot PROM Bus width.

S4-1: BPROMW1

S4-2: BPROMW0

Notes

S4-1 (Boot prom width 1)	S4-2 (Boot prom width 0)	Boot prom width
0	0	8 BITS (default)
0	1	16 BITS
1	0	32 BITS
1	1	RESERVED

Table 2.4 Boot Prom Width

S4-3: Debug boot mode

0 Regular mode

1 Debug boot mode (processor begins execution at ff200200)

S4-4: Reserved

Must be set to 0

S4-5: Endianess

Little endian 0

Big endian 1

Clock Multiplier

To generate Pipeline clock, input clock is multiplied by clock multiplier.

S4-6: MCLKX2

S4-7: MCLKX1

S4-8: MCLKX0

S4-6 MCLKX2	S4-7 MCLKX1	S4-8 MCLKX0	CLOCK MULTIPLIER
0	0	0	BY 2 (Default)
0	0	1	BY 3
0	1	0	BY 4
0	1	1	RESERVED
1	0	0	RESERVED
1	0	1	RESERVED
1	1	0	RESERVED
1	1	1	RESERVED

Table 2.5 Clock Multiplier

In the case of booting from flash or booting from flash and programming flash: (CS0 as chip select for flash devices for booting and programming), switch S4 (1and 2) are used to select flash port width for booting as well as "in system programming".

Switch configuration:

S4[1:2] as OFF and ON for 32 bit (4 chips)

S4[1:2] as ON and OFF for 16 bit (2 chips)

S4[1:2] as ON and ON for 8 bit (1 chip)

Notes

Jumper selection:

W14 between B and C

W10 between A and C and between B and D.

In case of booting from EPROM and programming flash:

Switch configuration:

Boot code vector bits [15:14] were hard wired in new EPLD code and switch (S3) 1&2 were used to select flash port width during in circuit programming (Using CS2 as chip select for flash programming).

Select:

S3[1:2] as OFF and ON for 32 bit (4 chips)

S3[1:2] as ON and OFF for 16 bit (2 chips)

S3[1:2] as ON and ON for 8 bit (1 chip)

Jumper selection:

W14 between B&C

W10 between A&B and C&D

System Software - IDT/SIM

EPROM's on the 79EB351 contain IDT's System Integration Manager (IDT/sim). IDT/sim is a software boot PROM debug monitor that provides functions for downloading software and for integrating hardware with software. Using IDT/sim, software can be downloaded onto the board from any computer with a RS-232C serial port or an ethernet port and a tftp server.

Drivers are added easily by using the IDT cross development software IDT/kit, and a user can acquire the IDT/sim source code to support other I/O devices or change I/O addresses to fit their specific application: for example, to change from big endian to little endian addressing.

Serial Port for CRT Video Terminal and Auxiliary Port

The 79EB351 system board has two RS232C serial port connectors.

The console port for the 79EB351 is the DB9P (9-pin female) connector designated as J1. The console port (CRT video terminal/PC/Work station) must be set for a data rate of 9600 baud with 8 bits of data, no parity bit, and one stop bit. The J2 port is for auxiliary use, such as down loading software from a PC or SPARCstation as described later in this chapter. The J2 port is also a DB9P (9-pin female). Pin assignments for J1 and J2 ports are listed in Table 2.6 and Table 2.7 below.

Pin	Board Signal
1	DCD
2	TXD
3	RXD
4	DSR
5	GND
6	DTR

Table 2.6 J1 Connector Pins and Signal Descriptions (Part 1 of 2)

Notes

Pin	Board Signal
7	CTS
8	RTS
9	RI

Table 2.6 J1 Connector Pins and Signal Descriptions (Part 2 of 2)

Pin	Boaard Signal
1	No connection
2	TXD
3	RXD
4	DSR
5	GND
6	DTR
7	CTS
8	RTS
9	No connection

Table 2.7 J2 Connector Pins and Signal Descriptions

Initialization and System Start-up

System start up is performed by turning on the power supply. If the power is already on, pressing the reset button will reinitialize the board. The board default configuration is Big Endian. Once started, IDT/sim will automatically boot and size the internal cache and main memory, and issue a message on the screen. The console is connected via CRT serial port. A message indicating cache and memory sizes, will appear along with the first command line prompt.

For more information on SIM commands, please refer IDT/sim User/Developer's Manual.

Connectors

J21: Power Connector

Pin	Signal	Color	Pin	Signal	Color
1	+3.3V	ORANGE	11	+3.3VDC (+3.3V default sense)	ORANGE (BROWN)
2	+3.3V	ORANGE	12	-12VDC	BLUE
3	COM	BLACK	13	COM	BLACK
4	+5VDC	RED	14	PS_ON#	GREEN
5	COM	BLACK	15	COM	BLACK
6	+5VDC	RED	16	COM	BLACK

Table 2.8 J21 Power Connector (Part 1 of 2)

Notes

Pin	Signal	Color	Pin	Signal	Color
7	COM	BLACK	17	COM	BLACK
8	PWR_OK	GRAY	18	-5VDC	WHITE
9	+5VSB	PURPLE	19	+5VDC	RED
10	+12VDC	YELLOW	20	+5VDC	RED

Table 2.8 J21 Power Connector (Part 2 of 2)

J6: JTAG Connector

All even Pins are GND.

Pin	Signal
1	TRST_N
3	TDI
5	TDO
7	TMS
9	TCK

Table 2.9 J6 JTAG Connector

J5: EJTAG Connector for 79RC32351

All even pins are GND.

Pin	Signal
1	TRST_N
3	TDI
5	TDO
7	TMS
9	TCK
11	RSTN
13	PCST0
15	PCST1
17	PCST2
19	DCLK
21	DEBUG BOOT
23	Vcc I/O

Table 2.10 J5 EJTAG Connector

Notes

Logic Analyzer POD Connectors

Logic Analyzer POD Connector J7

Pin	Signal	Pin	Signal
1	N.C	2	N.C.
3	GND	4	N.C.
5	MIC1_CLK	6	N.C
7	MII_TXCLK	8	WAITACK_N
9	MII_TXERR	10	INTEREQ_N
11	MII_TXEN	12	BG_N
13	MII_RXD3	14	BR_N
15	MII_RXD2	16	CS5_N
17	MII_RXD1	18	CS4_N
19	MII_RXD0	20	CS3_N
21	MII_COL	22	CS2_N
23	MII_CRS	24	CS1_N
25	MII_RXCLK	26	CS0_N
27	MII_RXER	28	USB_SOF
29	MII_RXDV	30	USB_CLK
31	MII_TXD3	32	USB_DN
33	MII_TXD2	34	USB_DP
35	MII_TXD1	36	MII_MDIO
37	MII_TXD0	38	MII_MDC

Table 2.11 Logic Analyzer POD Connector J7

Logic Analyzer POD Connector J8

Pin	Signal	Pin	Signal
1	N.C	2	N.C.
3	GND	4	N.C.
5	MIC2_CLK	6	N.C
7	N.C.	8	N.C.
9	N.C.	10	BOE1_N
11	N.C.	12	BOE0_N
13	N.C.	14	DMADONE_N
15	RW_N	16	DMAREQ_N
17	OE_N	18	U1CTS_DCLK
19	COLDRST_N	20	U1RD_DMA2

Table 2.12 Logic Analyzer POD Connector J8 (Part 1 of 2)

Notes

Pin	Signal	Pin	Signal
21	RST_N	22	U0_TD
23	NC	24	U0_CTS
25	NC	26	U0_RTS
27	NC	28	U0_DSR
29	NC	30	U0_DTR
31	NC	32	U0_DCD
33	NC	34	U0RI/TRST_N
35	NC	36	U0_RD
37	N.C.	38	U0_TD

Table 2.12 Logic Analyzer POD Connector J8 (Part 2 of 2)

Logic Analyzer POD Connector J9

Pin	Signal	Pin	Signal
1	N.C	2	N.C.
3	GND	4	N.C.
5	N.C.	6	N.C
7	D15	8	SDCS1_N
9	D14	10	SDCS0_N
11	D13	12	SDWE_N
13	D12	14	CAS_N
15	D11	16	RAS_N
17	D10	18	SDCKEN
19	D9	20	A7
21	D8	22	A6
23	D7	24	A5
25	D6	26	A4
27	D5	28	A3
29	D4	30	A2
31	D3	32	A1
33	D2	34	A0
35	D1	36	BWE1_U
37	D0	38	BWE0_U

Table 2.13 Logic Analyzer POD Connector J9

Notes

Logic Analyzer POD Connector J11

Pin	Signal	Pin	Signal
1	N.C	2	N.C.
3	GND	4	N.C.
5	N.C.	6	N.C
7.	ATM_TXD7	8	A24
9	ATM_TXD6	10	A23
11	ATM_TXD5	12	A22
13	ATM_TXD4	14	A21
15	ATM_TXD3	16	ATM_RXCLK
17	ATM_TXD2	18	RXCLAV
19	ATM_TXD1	20	RXSOC
21	ATM_TXD0	22	TXCLAV
23	ATM_RXD7	24	ATM_TXCLK
25	ATM_RXD6	26	TXSOC
27	ATM_RXD5	28	ATM_RXEN_N
29	ATM_RXD4	30	ATM_TXEN_N
31	ATM_RXD3	32	ATM_TXAD1
33	ATM_RXD2	34	ATM_TXAD0
35	ATM_RXD1	36	ATM_RXAD1
37	ATM_RXD0	38	ATM_RXAD0

Table 2.14 Logic Analyzer POD Connector J11

Logic Analyzer POD Connector J15

Pin	Signal	Pin	Signal
1	N.C	2	N.C.
3	GND	4	N.C.
5	SYSCLK_DIMM	6	SYSCLK_SODIMM
7	D31	8	N.C.
9	D30	10	BWE3_U_N
11	D29	12	BWE2_U_N
13	D28	14	A20
15	D27	16	A19
17	D26	18	A18
19	D25	20	A17
21	D24	22	A16
23	D23	24	A15

Table 2.15 Logic Analyzer POD Connector J15 (Part 1 of 2)

Notes

Pin	Signal	Pin	Signal
25	D22	26	A14
27	D21	28	A13
29	D20	30	A12
31	D19	32	A11
33	D18	34	A10
35	D17	36	A9
37	D16	38	A8

Table 2.15 Logic Analyzer POD Connector J15 (Part 2 of 2)

Notes

Theory of Operation and Design Notes

Notes

Introduction

This chapter provides information on the functional operation of the IDT79EB351 evaluation board for the RC32351 communications processor. For detailed schematics, refer to Chapter 4. For detailed PLD equations, refer to Chapter 5.

Address Space Decoding (Preliminary)

Physical addresses for the resources on the 79EB351 board use the following typical memory map.

Description	Chip Select Allocation	Physical Address Range
EPROM	CS0	1FC0_0000 to 1FCF_FFFF
FLASH	CS0/CS2	0C00_0000 to 0C7F_FFFF
SRAM	CS1	0200_0000 to 020F_FFFF
DRAM (SDRAM)		0000_0000 to 01FF_FFFF
LCD	CS3	1A00_2000 to 1A00_3FFF
RTC (real time clock)	CS3	1A00_4000 to 1A00_5FFF
ATM PHY	CS4	1400_0000 to 1400_FFFF

Table 3.1 Physical Address Mapping of the 79EB351 Board Resources

LEDs

DS1	Ethernet/CFG3
DS2	Ethernet/CFG2
DS3	Ethernet/CFG1
DS4	2.5 V present
DS8	3.3 V present
DS12	Cold reset
DS5	ATM TxLED0
DS6	ATM TxLED1
DS7	ATM TxLED2
DS9	ATM RxLED0
DS10	ATM RxLED1
DS11	ATM RxLED2

Table 3.2 LEDs

Notes

USB Device Speed Selection

Speed of a device is detected by pulling up the D+ or D- line. If the D+ line is pulled high (R34 installed), the device is at full speed. If the D- line is pulled high, the device is at low speed.

Schematics

Notes

Schematics Errata

This section reflects the changes to the 79EB351 Evaluation Board (18-511-000).

Revision History

March 12, 2001: Rev 01, Item #1.

January 18, 2002: Rev 02, added Item #2.

June 9, 2003: Rev 03, added Item #3.

Item #1

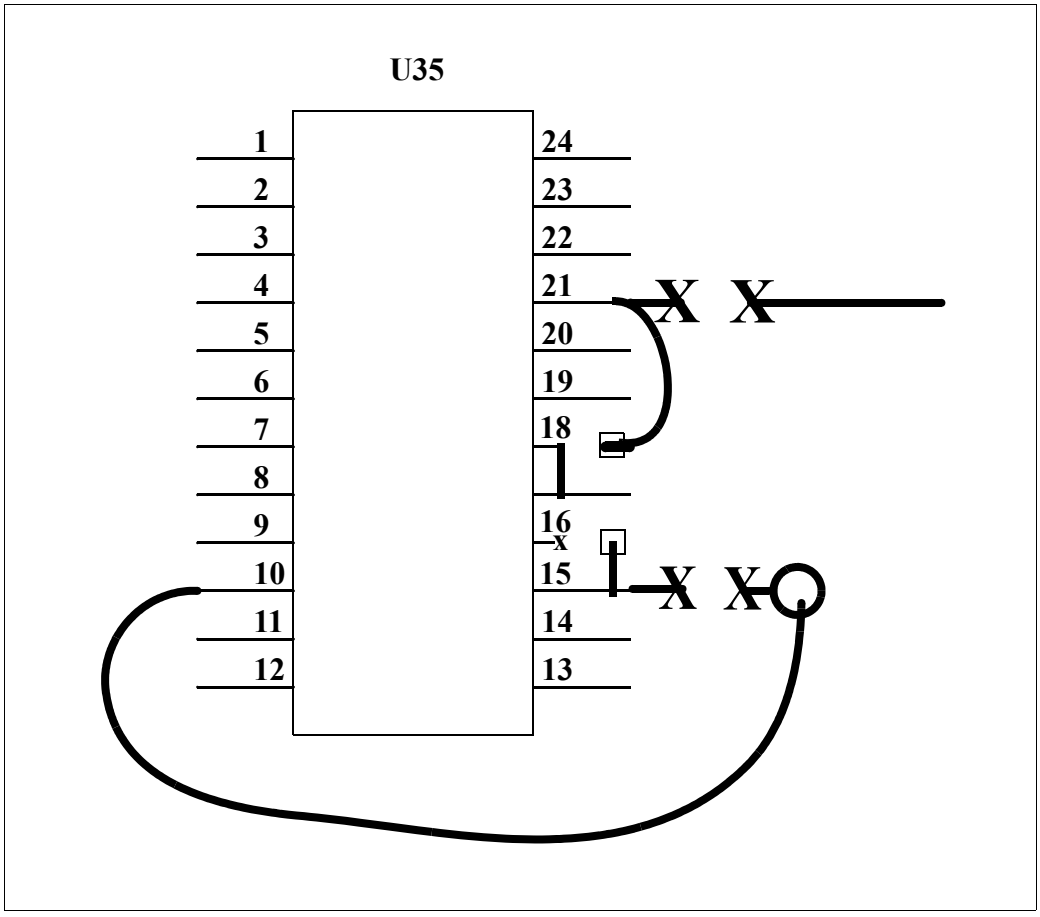


Figure 4.1 79EB351 Bluewire List

Data Line Misconnection U35 Rework List

Cuts

U35-15: Cut trace between via and pin 15

U35-21: Cut trace

Notes

U35-16: Either cut and remove or lift this pin.

Jumpers

Lift U35 Pin 18 & jumper to U35 pin 17

Jumper from U35 pad 18 to U35 pin 21

Jumper from via adjacent to U35 pin 15 to U35 pin 10.

Place solder dot between U35 pin 15 & U35 pad 16 (pin 16 was cut off earlier).

Don't Populate the Following Components:

- Oscillator 4.096Mhz @ position Y5 (Sheet #11 TDM related stuff).
- IC 72V8981 @ position U7 (Sheet #11 TDM related stuff).
- 2x5 pin Connector @ position J20 (Sheet #11 TDM related stuff).
- IC 24LC64 @ position U16 (Sheet #14 I2C related stuff).
- Zero ohm Resistors @ positions R16, R18 and R20 (Sheet #14 I2C related stuff).
- 1x4 pin jumper stick @ position J19 (Sheet #14 I2C related stuff).
- 1x2 pin jumper stick @ positions W11, W12 and W13 (Sheet #14 I2C related stuff).

Item #2

Ethernet Performance Fix

Because of signal integrity issues, the traces MII_TXCLK and MII_RXCLK that go to the PMC connector J22 has been disconnected from the circuits. This change has resulted in a significant improvement in the performance of the Ethernet interfaces. The locations of these trace disconnects are shown in the following two figures.

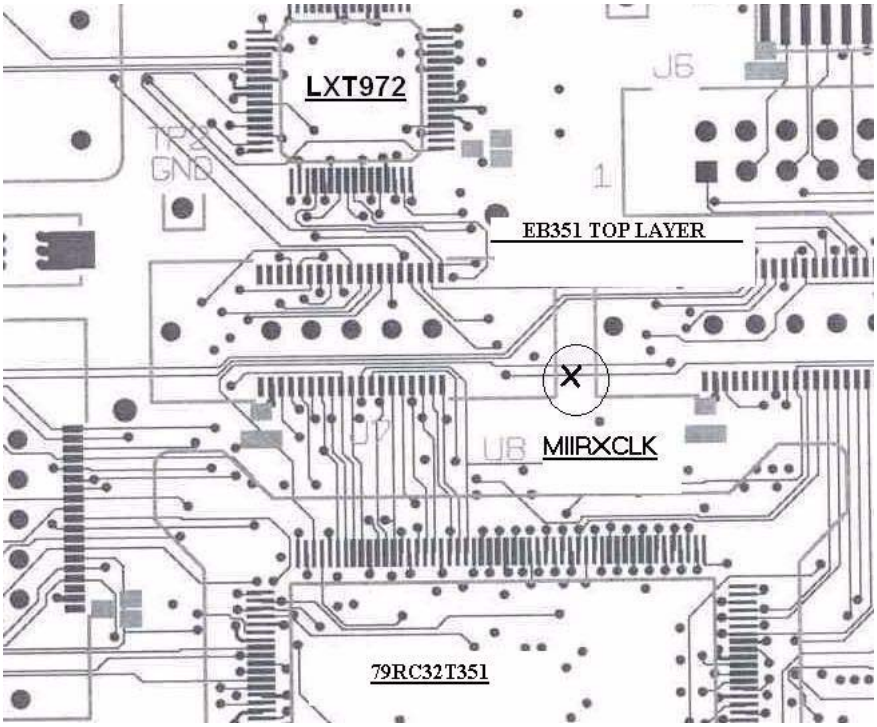


Figure 4.2 79EB351 Top Layer

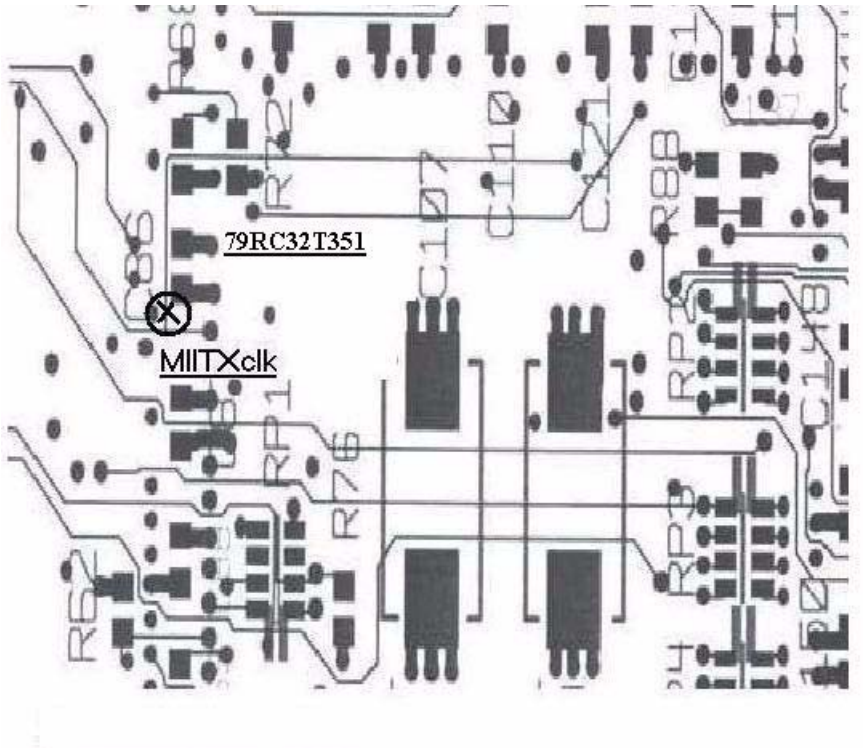


Figure 4.3 79EB351 Bottom Layer

Item #3

EPLD Code Did Not Support System Flash Programming or Control Wait/ack Input of CPU's Input by Multiple Devices

The following revisions were made (Notation "Component location-Pin number" ex: J7-16):

Added wire between J7-16 and U13-62 (else to the PAD of R15 that is close to the U13 Altera EPLD)

Added resistor 10K between J22-27 and J22-33.

Added resistor 10K between J13-58 and J18-8.

Replaced Serial number sticker from REV2.0 to REV3.0.

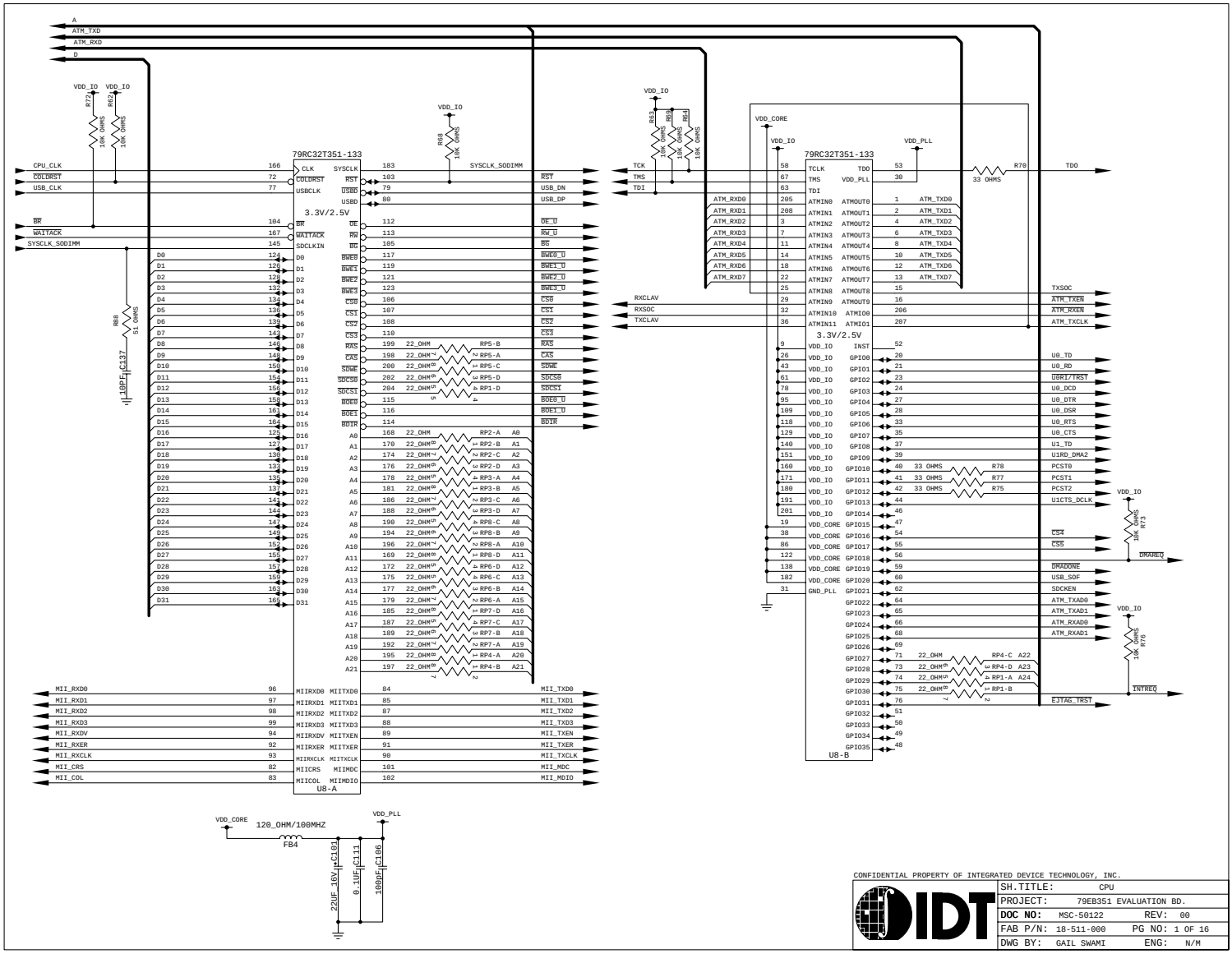
Reprogrammed the EPLD with new program.

Schematics

REVISIONS

DCN	REV	DESCRIPTION	DATE	APPR
100768	00	INITIAL RELEASE	1-11-02	DS

SH.TITLE:	TABLE OF CONTENTS
PROJECT:	79EB351 EVALUATION BD.
DOC NO:	MSC-50122 REV: 00
FAB P/N:	18-511-000 PG NO: 0 OF 16
DWG BY:	GAIL SWAMI ENG: N/M



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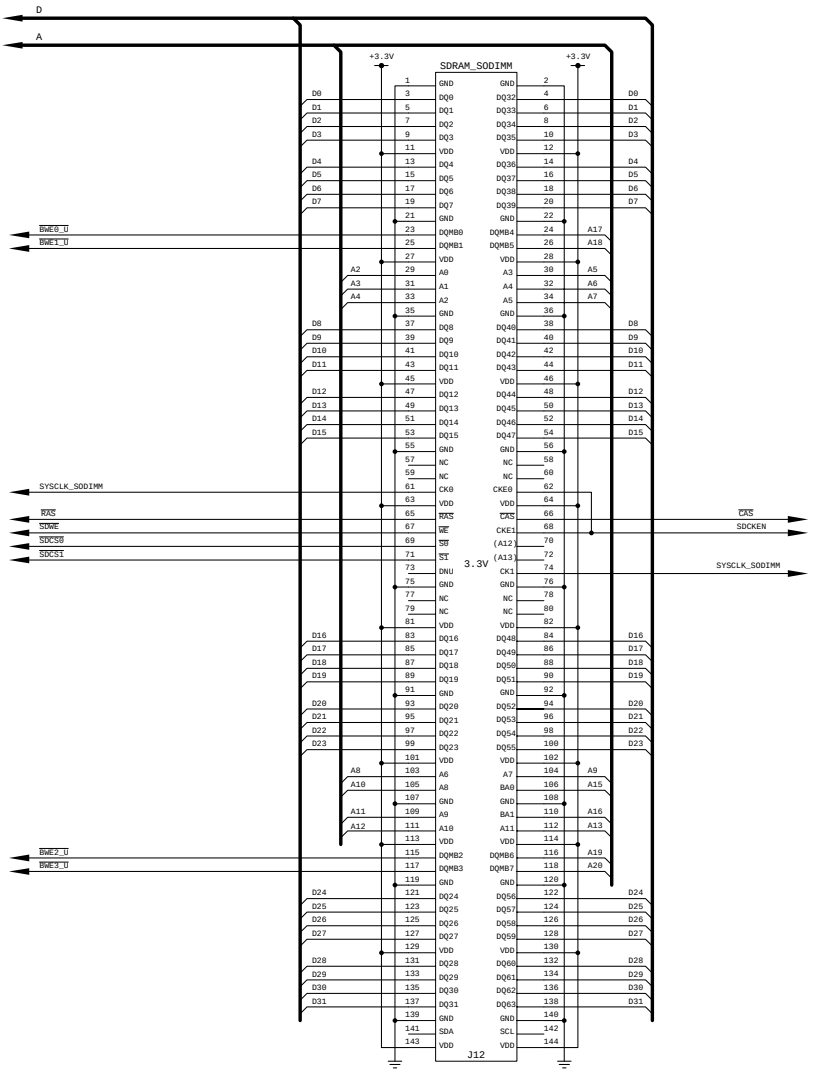
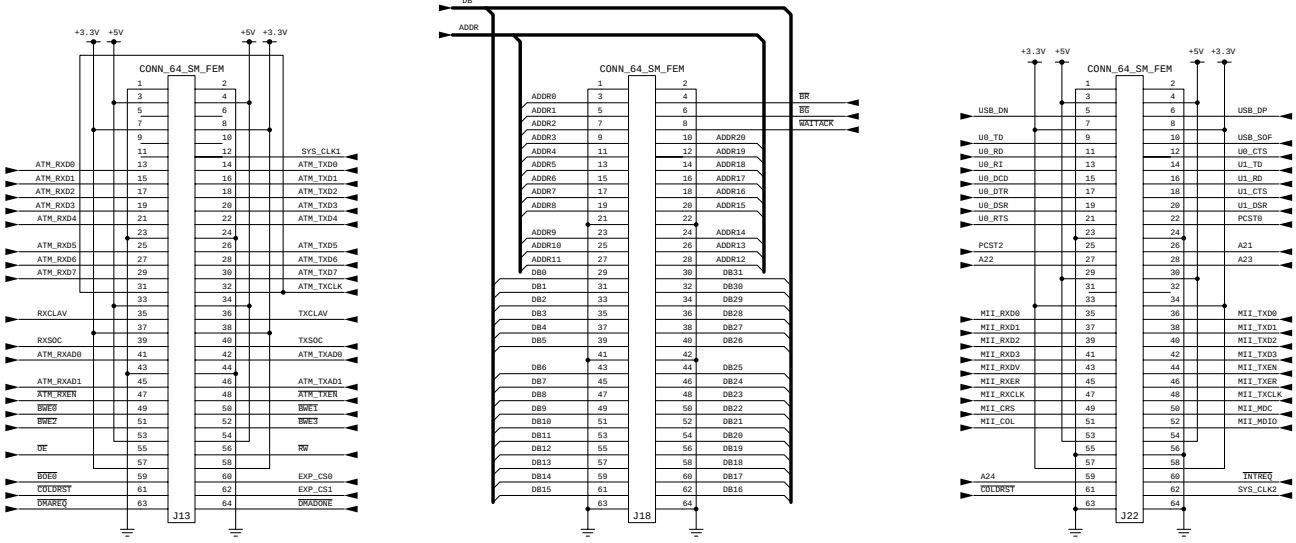
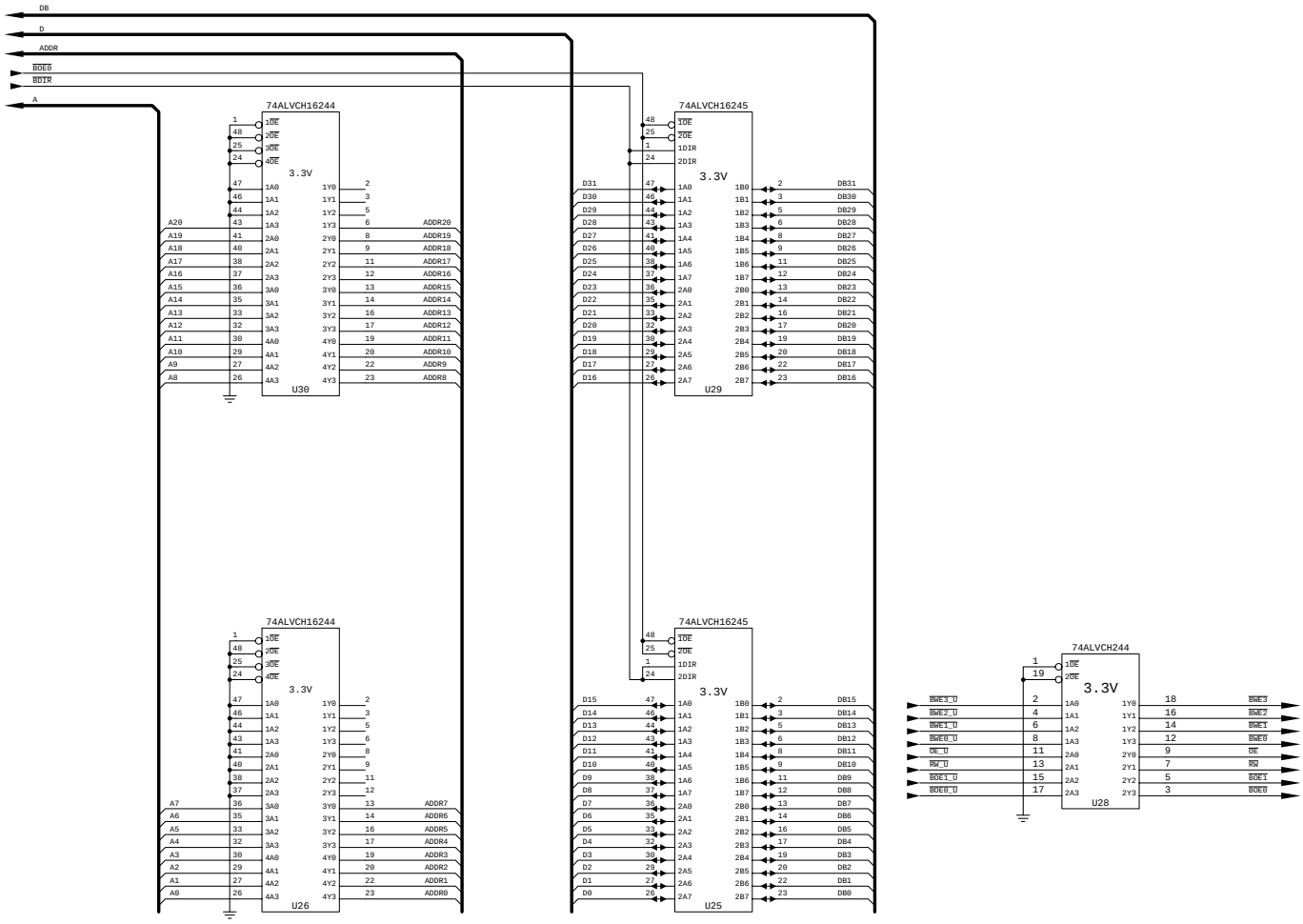
SH.TITLE:	CPU
PROJECT:	79EB351 EVALUATION BD.
DOC NO: MSC-50122	REV: 00
FAB P/N: 18-511-000	PG NO: 1 OF 16
DWG BY: GAIL SWAMI	ENG: N/M



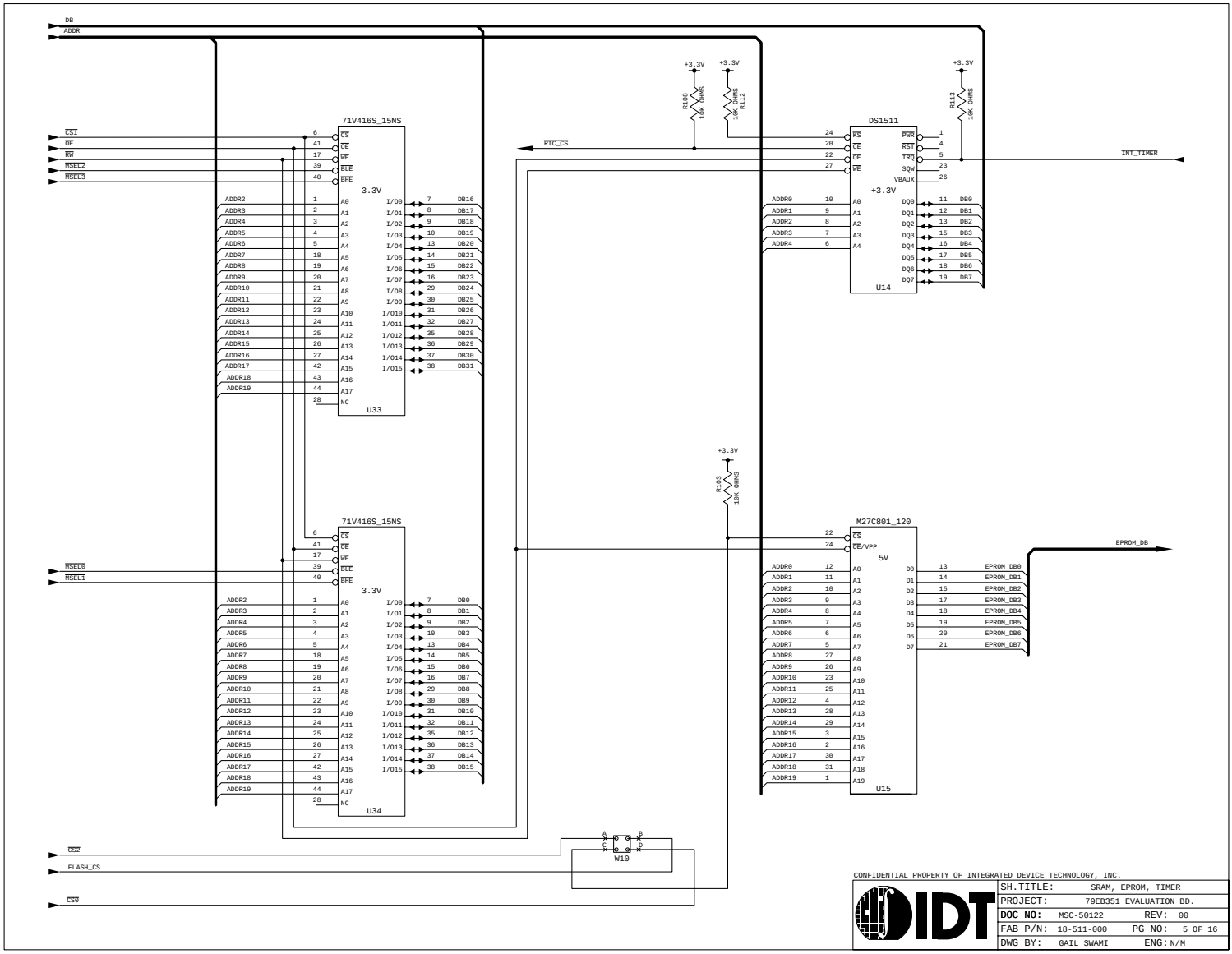
SH.TITLE:	SDRAM
PROJECT:	79EB351 EVALUATION BD.
DOC NO: MSC-50122	REV: 00
FAB P/N: 18-511-000	PG NO: 2 OF 16
DWG BY: GAIL SWAMI	ENG: N/M



SH.TITLE:	EXPANSION CONNECTORS
PROJECT:	79EB351 EVALUATION BD.
DOC NO:	MSC-50122 REV: 00
FAB P/N:	81-511-000 PG NO: 3 OF 16
DWG BY:	GAIL SWAMI ENG: N/M



SH.TITLE:	BUFFERS
PROJECT:	79EB351 EVALUATION BD.
DOC NO:	MSC-50122 REV: 00
FAB P/N:	18-511-000 PG NO: 4 OF 16
DWG BY:	GAIL SWAMI ENG: N/M



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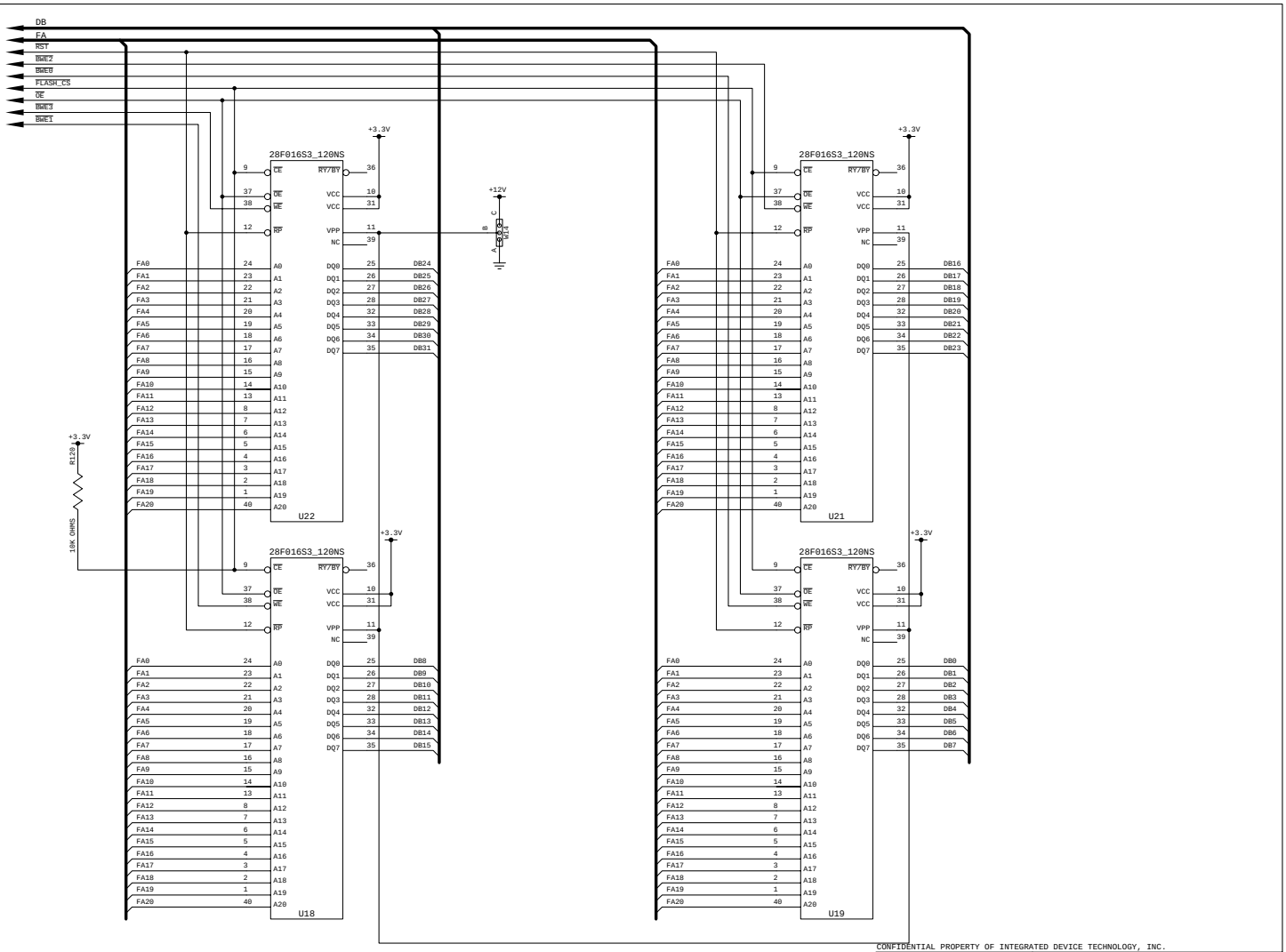
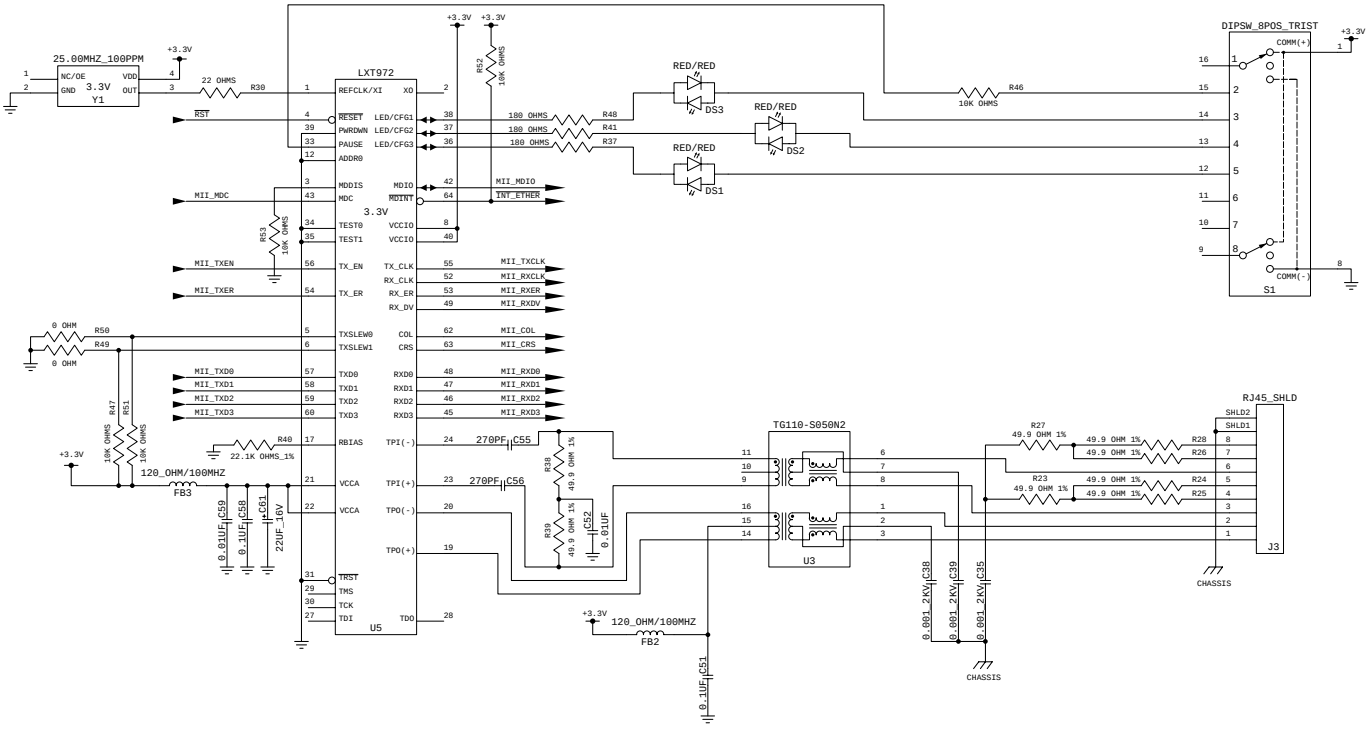
SH.TITLE:	SRAM, EPROM, TIMER		
PROJECT:	79EB351 EVALUATION BD.		
DOC NO:	MSC-50122	REV:	00
FAB P/N:	18-511-000	PG NO:	5 OF 16
DWG BY:	GAIL SWAMI	ENG:	N/M

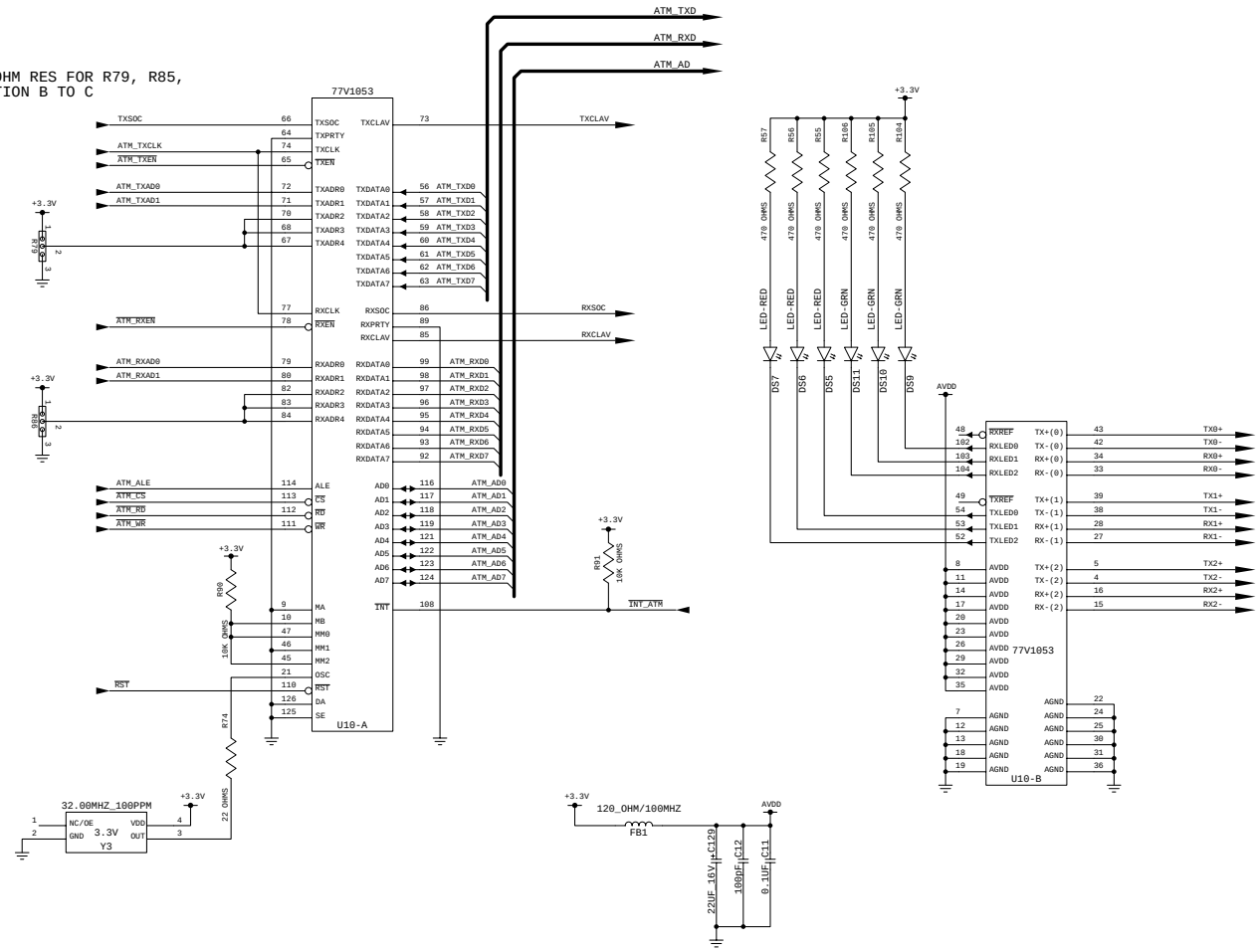


SH.TITLE:	FLASH MEMORY		
PROJECT:	79EB351 EVALUATION BD.		
DOC NO:	MSC-50122	REV:	00
FAB P/N:	18-511-000	PG NO:	6 OF 16
DWG BY:	GAIL SWAMI	ENG:	N/M

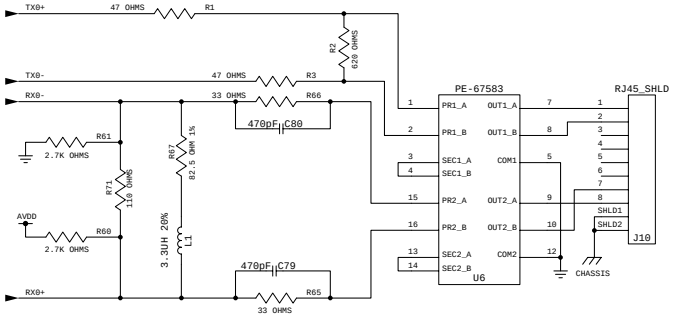


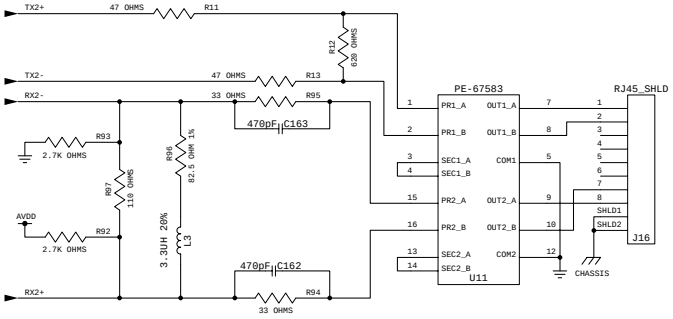
CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.

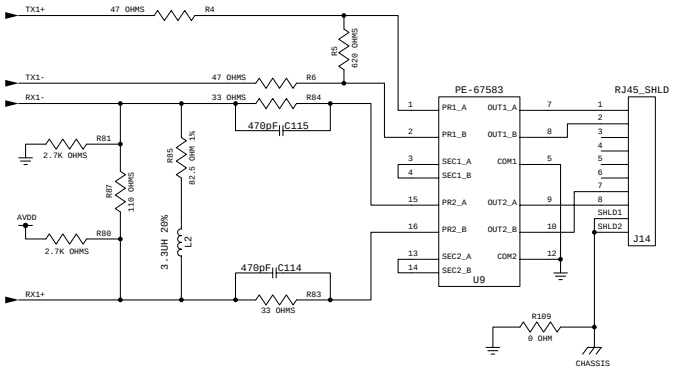
SH.TITLE:	ETHERNET PHY		
PROJECT:	79EB351 EVALUATION BD.		
DOC NO:	MSC-50122	REV:	00
FAB P/N:	18-511-000	PG NO:	7 OF 16
DWG BY:	GAIL SWAMI	ENG:	N/M



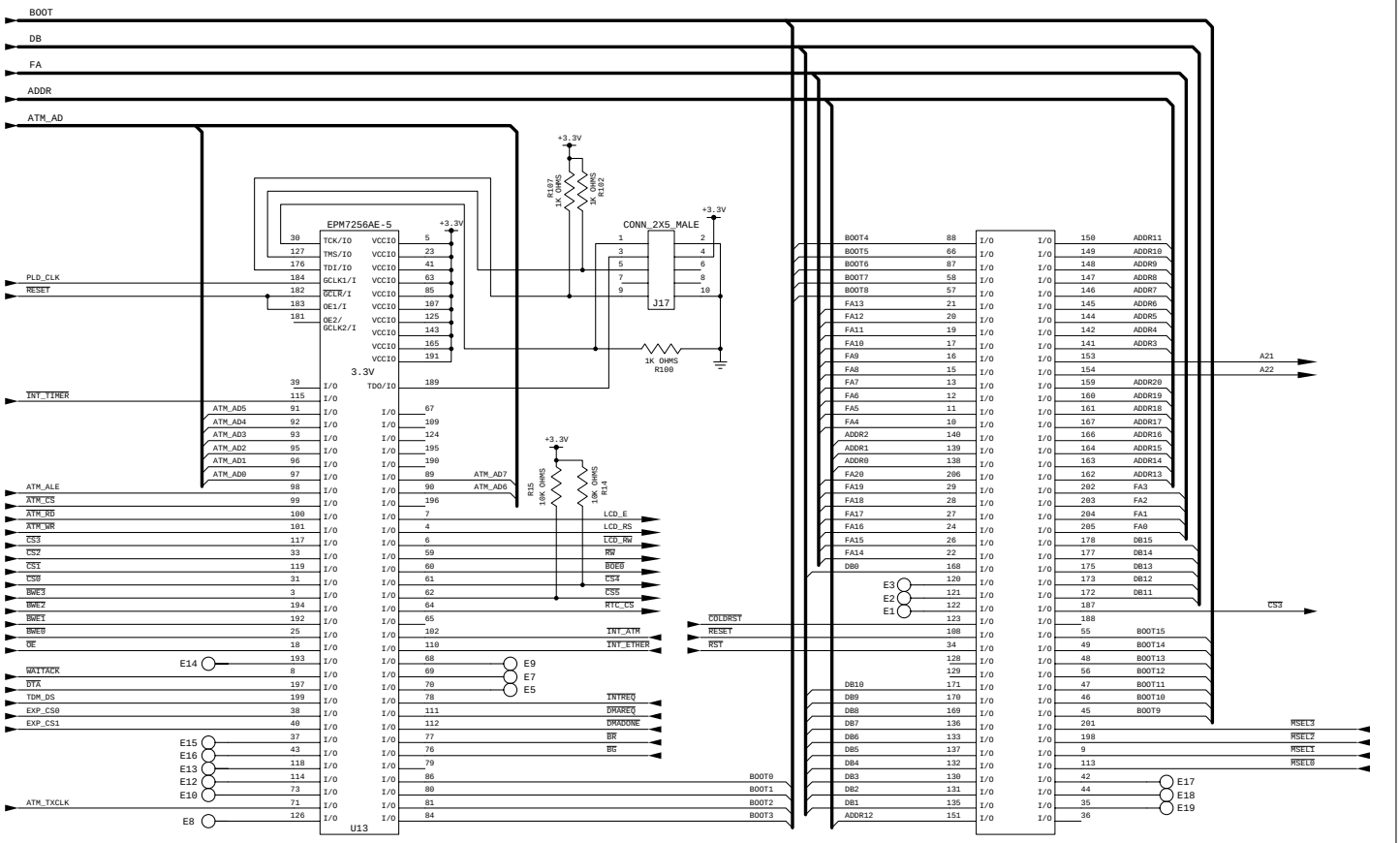
SH.TITLE:	ATM PHY
PROJECT:	79EB351 EVALUATION BD.
DOC NO:	MSC-50122 REV: 00
FAB P/N:	18-511-000 PG NO: 8 OF 16
DWG BY:	GAIL SWAMI ENG: N/M



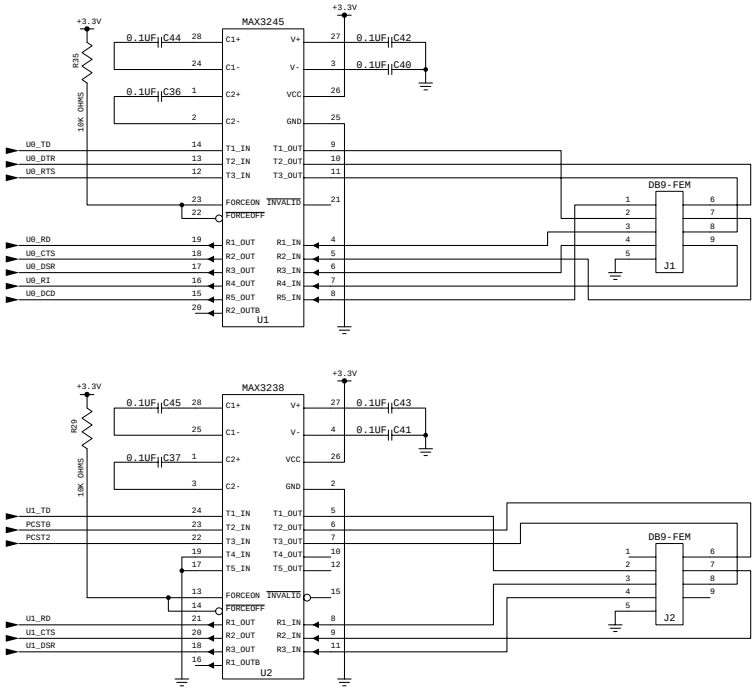




SH.TITLE:	ATM MAGNETICS		
PROJECT:	79EB351 EVALUATION BD.		
DOC NO:	MSC-50122	REV:	00
FAB P/N:	18-511-000	PG NO:	9 OF 16
DWG BY:	GAIL SWAMI	ENG:	N/M

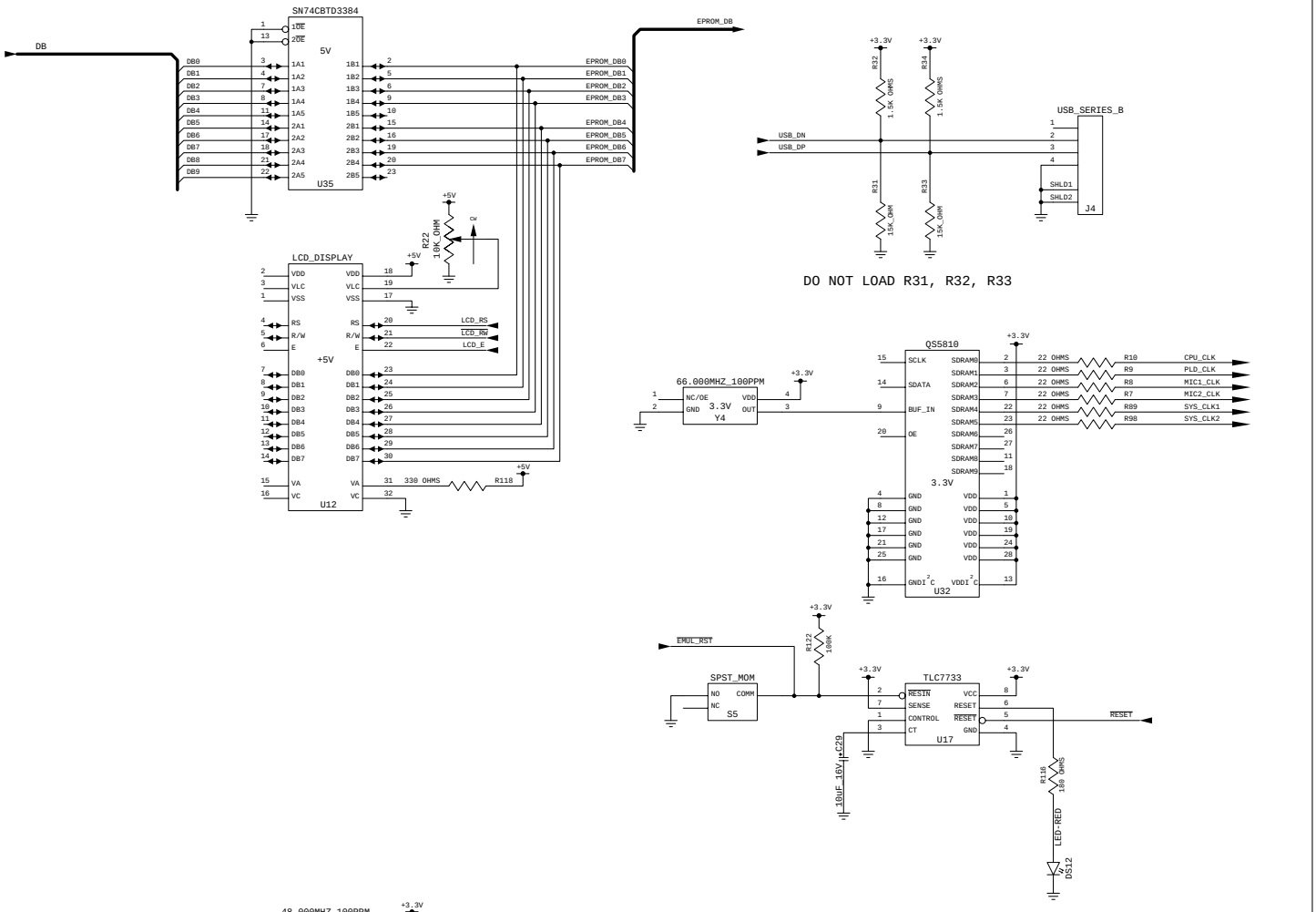


SH.TITLE:	EPLD, INTERRUPT STATUS
PROJECT:	79EB351 EVALUATION BD.
DOC NO:	MSC-50122 REV: 00
FAB P/N:	18-511-000 PG NO: 10 OF 16
DWG BY:	GAIL SWAMI ENG: N/M

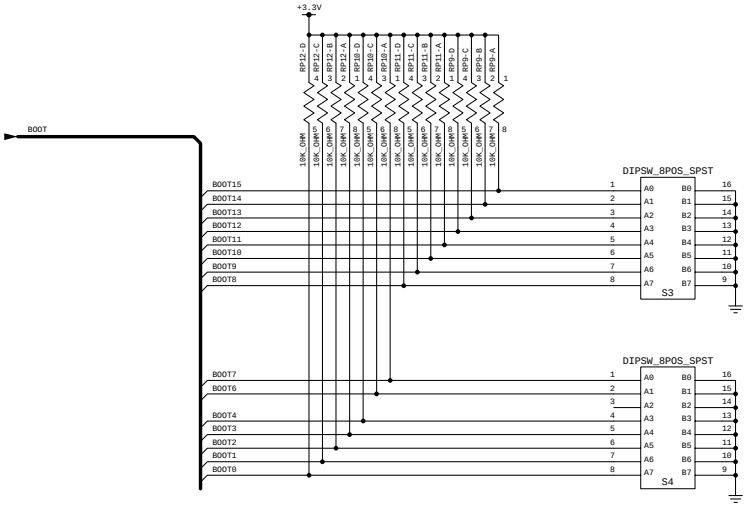


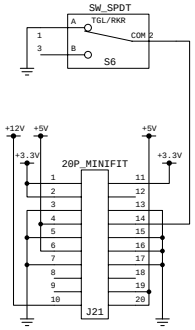
CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.

SH.TITLE:	UART
PROJECT:	79EB351 EVALUATION BD.
DOC NO: MSC-50122	REV: 00
FAB P/N: 18-511-000	PG NO: 11 0F 16
DWG BY: GAIL SWAMI	ENG: N/M

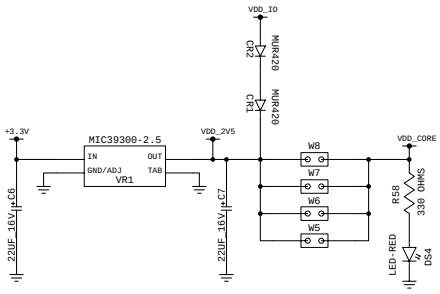


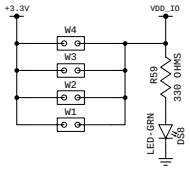
SH.TITLE:	LCD, RESET, USB
PROJECT:	79EB351 EVALUATION BD.
DOC NO:	MSC-50122 REV: 00
FAB P/N:	18-511-000 PG NO: 12 OF 16
DWG BY:	GAIL SWAMI ENG: N/M



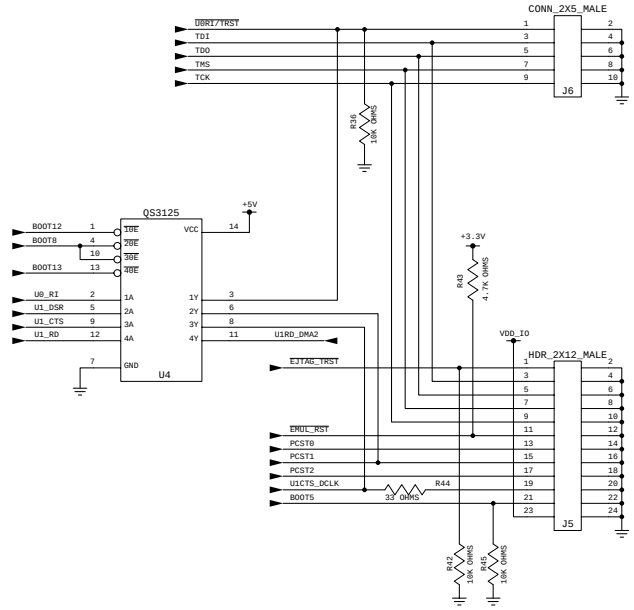


ATX POWER SUPPLY

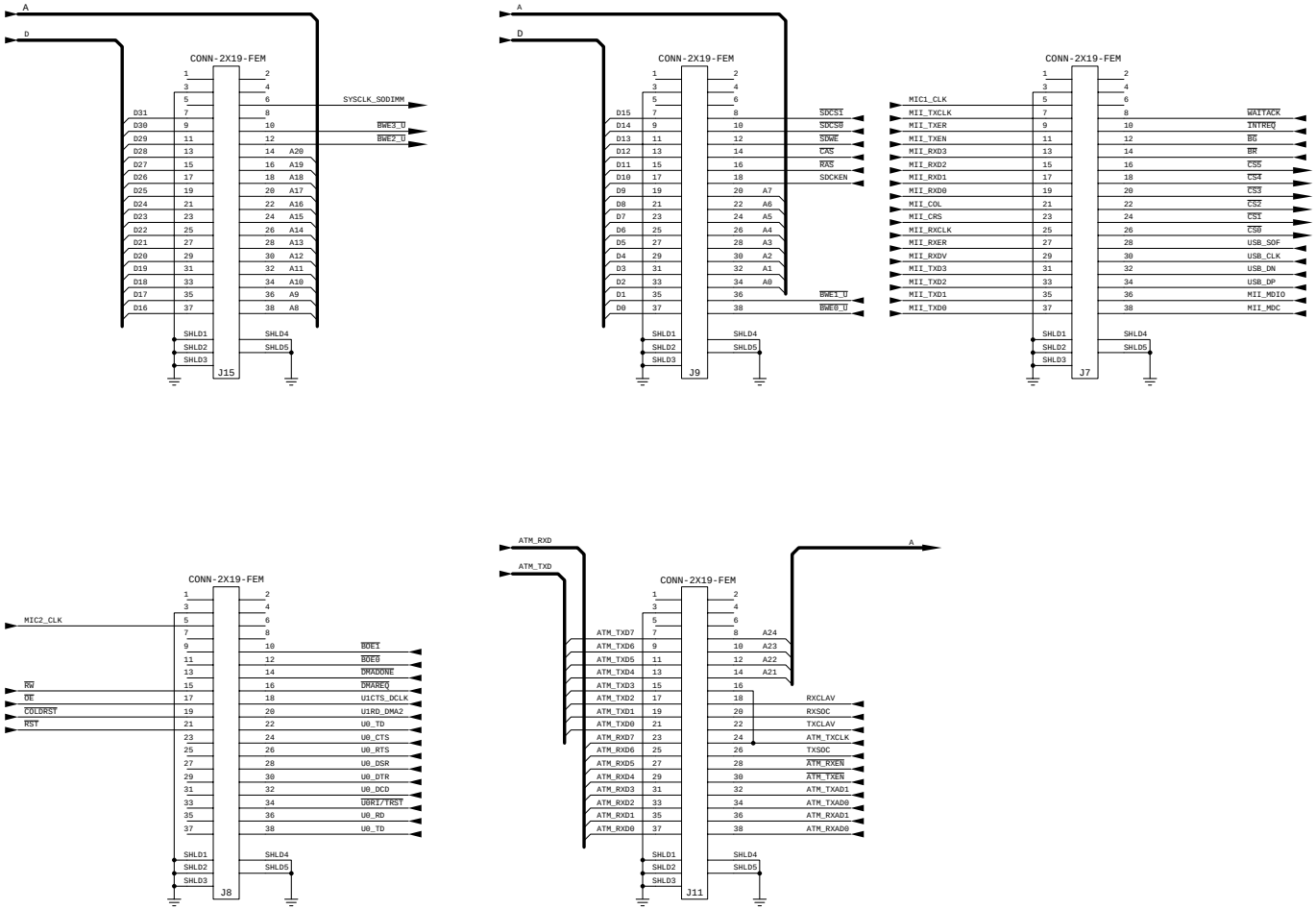




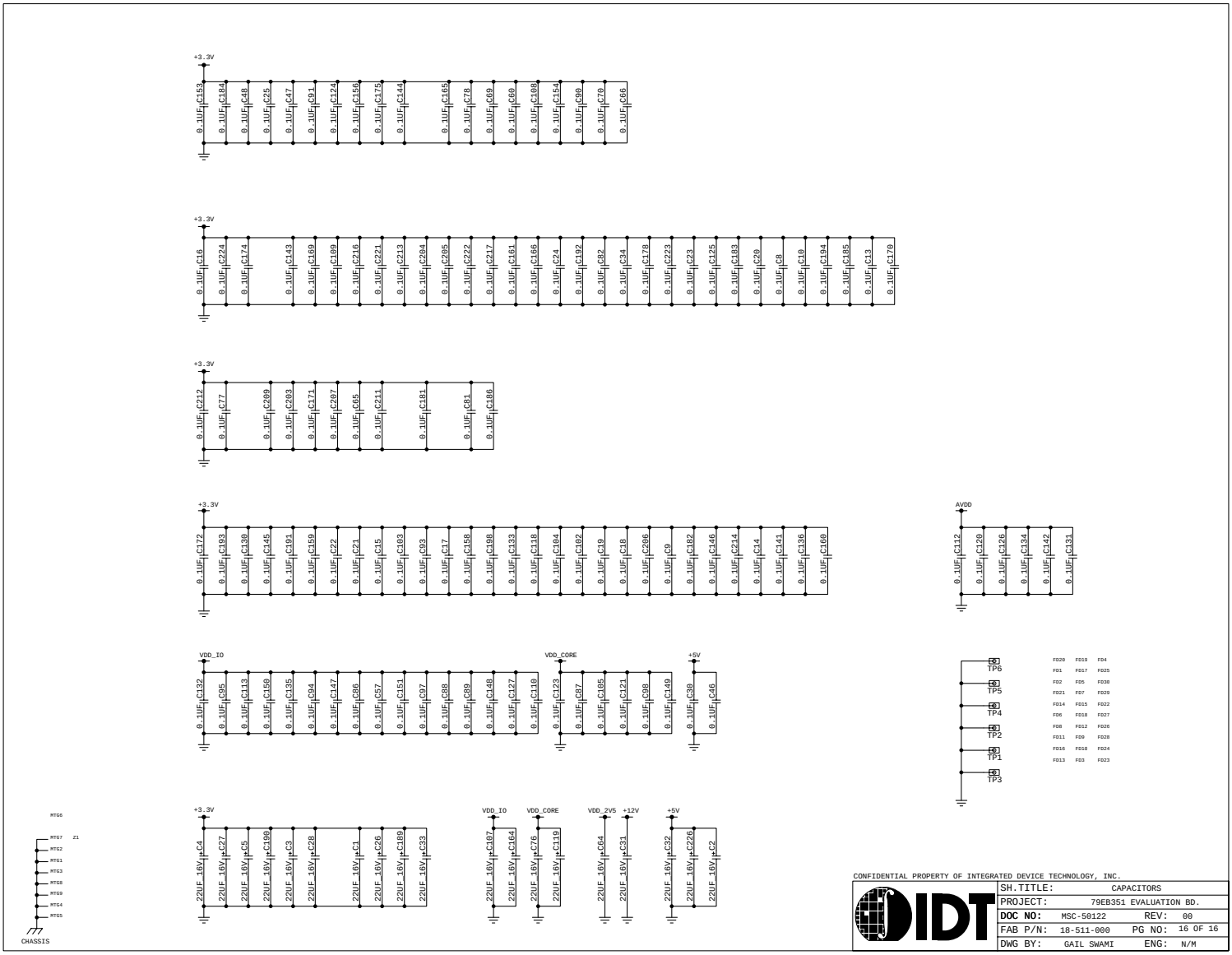
SH.TITLE:	CONFIG, POWER SUPPLY		
PROJECT:	79EB351 EVALUATION BD.		
DOC NO:	MSC-50122	REV:	00
FAB P/N:	18-511-000	PG NO:	13 OF 16
DWG BY:	GAIL SWAMI	ENG:	N/M



SH.TITLE:	LOGIC ANALYZER CONNECTORS
PROJECT:	79EB351 EVALUATION BD.
DOC NO:	MSC-50122 REV: 00
FAB P/N:	18-511-000 PG NO: 14 OF 16
DWG BY:	GAIL SWAMI ENG: N/M



SH.TITLE:	LOGIC ANALYZER CONNECTORS
PROJECT:	79EB351 EVALUATION BD.
DOC NO:	MSC-50122 REV: 00
FAB P/N:	18-511-000 PG NO: 15 OF 16
DWG BY:	GAIL SWAMI ENG: N/M



SH.TITLE:	CAPACITORS
PROJECT:	79EB351 EVALUATION BD.
DOC NO:	MSC-50122 REV: 00
FAB P/N:	18-511-000 PG NO: 16 OF 16
DWG BY:	GAIL SWAMI ENG: N/M

EPLD Equation

Notes

```
SUBDESIGN EB351_reset
(
   boot[15..0] :INPUT;
   db[15..8] :OUTPUT;
   d[7..0]:bidir;
   addr[20..0] : INPUT;
   a[22..21]:INPUT;

   fa[20..0] : OUTPUT;
   mem_sel_n[3..0] : OUTPUT;
   bwe_n[3..0] : INPUT;
   rw_n:input;

   reset_n : input;  %183%
   coldrst_n: output; %123%

   lcd_e:output;
   lcd_rw_n:output;
   lcd_rs:output;


   atm_ad[7..0]:bidir;
   atm_clk:input;
   atm_ale:output;
   atm_rd:output;
   atm_wr:output;
   boe_n:input;
   cs4:input;
   atm_cs: output;
   int_atm:input;


   rtc_cs:output;
   cs5:input;
   tdm_cs:output;
   cs3_remove:input;
   sdclk_dlyd:output;

% bogus junk to make pins behave %
   reset_n2: input;  %108%
   dummyrst : input; %182%
   sys_clk:input;    %184%
   %reset_n2out : output; %
   cs0: input; %31%
   cs1: input;  %119%
   cs2: input; %33%
```

Notes

```
    cs3: input; %117%
    cs_combined: output; %118%
    rst : input; %34%
    oe : input; %18%
% end bogus junk %

    waitack_n : output; %8%
    busreq : output; %77%
    busgnt : input; %76%

    exp_cs0_n : output;
    exp_cs1_n : output;
    dmareq_n : input;
    dmadone_n : input;

        )
VARIABLE
    rstcntrl:NODE;
    atm_ale1:node;
    ale_en1, ale_en2:dff;
    atm_wr1_en, atm_wr2_en:dff;
    atm_wr_en:node;


BEGIN

    cs_combined = cs1 & cs0 & cs2 & cs3 & rst & busgnt & oe;
    busreq = VCC;
    waitack_n = VCC;

    coldrst_n = reset_n;
    rstcntrl = !reset_n;

    --db[15] = TRI(boot[15], rstcntrl);
    db[15] = TRI(GND, rstcntrl);

    --db[14] = TRI(boot[14], rstcntrl);
    db[14] = TRI(GND, rstcntrl);

    db[13] = TRI(boot[13], rstcntrl);
    db[12] = TRI(boot[12], rstcntrl);
    db[11] = TRI(boot[11], rstcntrl);
    db[10] = TRI(boot[10], rstcntrl);
    db[9] = TRI(boot[9], rstcntrl);
    db[8] = TRI(boot[8], rstcntrl);

    mem_sel_n[3..0] = bwe_n[3..0] & oe;

%
    case boot[7..6] is
      when 0 =>
```

Notes

```
      fa[20..0]=addr[20..0];
    when 1 =>
      fa[20..0]=(a21,addr[20..1]);
    when 2 =>
      fa[20..0]= (gnd,a21,addr[20..2]);
  endcase;
%
% Code changed for flash address %
    IF !cs2 THEN
  case boot[15..14] is
    when 0 =>
      fa[20..0]=addr[20..0];
    when 1 =>
      fa[20..0]=(a21,addr[20..1]);
    when 2 =>
      fa[20..0]= (a22,a21,addr[20..2]);
  end case;
    ELSE
  case boot[7..6] is
    when 0 =>
      fa[20..0]=addr[20..0];
    when 1 =>
      fa[20..0]=(a21,addr[20..1]);
    when 2 =>
      fa[20..0]= (a22,a21,addr[20..2]);
  end case;
    END IF;

  %LCD Module Control Signals%
  lcd_rs          = addr0;
  lcd_rw_n        = rw_n;
  lcd_e           = !cs3 & !addr15 & !addr14 & addr13 &(oe$bwe_n0);

  % ATM PHY Control  %
  atm_cs          = lcell(lcell(lcell(cs4)));
  atm_ale         = !boe_n & cs4;

  % delay for address hold time%
  ale_en1.clk     = !sys_clk;
  ale_en1.clrn    = dummyrst;
  ale_en1.d       = atm_ale;
  ale_en2.clk     = !sys_clk;
  ale_en2.clrn    = dummyrst;
  ale_en2.d       = ale_en1.q;
  atm_ale1        = ale_en2.q;

  atm_rd          = oe # !rw_n # cs4;
  atm_wr          = rw_n # bwe_n0 # cs4;

  atm_wr1_en.clk  = !sys_clk;
  atm_wr1_en.clrn = dummyrst;
```

Notes

```
atm_wr1_en.d    = !bwe_n0 & !cs4 & !rw_n;
atm_wr2_en.clk  = !sys_clk;
atm_wr2_en.clrn = dummyrst;
atm_wr2_en.d    = atm_wr1_en.q;
atm_wr_en       = atm_wr2_en.q;

atm_ad[7] = tri(reset_n & (d[7] & atm_wr_en # addr[9] & atm_ale1),
                reset_n & (atm_ale1 # atm_wr_en));
atm_ad[6] = tri(reset_n & (d[6] & atm_wr_en # addr[8] & atm_ale1),
               reset_n & (atm_ale1 # atm_wr_en));
atm_ad[5] = tri(reset_n & (d[5] & atm_wr_en # addr[7] & atm_ale1),
                reset_n & (atm_ale1 # atm_wr_en));
atm_ad[4] = tri(reset_n & (d[4] & atm_wr_en # addr[6] & atm_ale1),
                reset_n & (atm_ale1 # atm_wr_en));
atm_ad[3] = tri(reset_n & (d[3] & atm_wr_en # addr[5] & atm_ale1),
                reset_n & (atm_ale1 # atm_wr_en));
atm_ad[2] = tri(reset_n & (d[2] & atm_wr_en # addr[4] & atm_ale1),
                reset_n & (atm_ale1 # atm_wr_en));
atm_ad[1] = tri(reset_n & (d[1] & atm_wr_en # addr[3] & atm_ale1),
                reset_n & (atm_ale1 # atm_wr_en));
atm_ad[0] = tri(reset_n & (d[0] & atm_wr_en # addr[2] & atm_ale1),
                reset_n & (atm_ale1 # atm_wr_en));

d[7] = tri(atm_ad7 & !cs4 & !oe & rw_n & reset_n # boot7 & !reset_n, !reset_n # !cs4 &
           !oe & rw_n);
d[6] = tri(atm_ad6 & !cs4 & !oe & rw_n & reset_n # boot6 & !reset_n, !reset_n # !cs4 &
           !oe & rw_n);
d[5] = tri(atm_ad5 & !cs4 & !oe & rw_n & reset_n # boot5 & !reset_n, !reset_n # !cs4 &
           !oe & rw_n);
d[4] = tri(atm_ad4 & !cs4 & !oe & rw_n & reset_n # boot4 & !reset_n, !reset_n # !cs4 &
           !oe & rw_n);
d[3] = tri(atm_ad3 & !cs4 & !oe & rw_n & reset_n # boot3 & !reset_n, !reset_n # !cs4 &
           !oe & rw_n);
d[2] = tri(atm_ad2 & !cs4 & !oe & rw_n & reset_n # boot2 & !reset_n, !reset_n # !cs4 &
           !oe & rw_n);
d[1] = tri(atm_ad1 & !cs4 & !oe & rw_n & reset_n # boot1 & !reset_n, !reset_n # !cs4 &
           !oe & rw_n);
d[0] = tri(atm_ad0 & !cs4 & !oe & rw_n & reset_n # boot0 & !reset_n, !reset_n # !cs4 &
           !oe & rw_n);

rtc_cs = !(!cs3 & !addr15 & addr14 & !addr13);
tdm_cs = !(!cs3 & !addr15 & !addr14 & !addr13);

sdclk_dlyd = lcell(!sys_clk);

exp_cs0_n = !(!cs5 & !addr15 & !addr14 & !addr13 & !addr12 & !addr11 & !addr10 &
              !coldrst_n);
exp_cs1_n = !(!cs5 & !addr15 & !addr14 & !addr13 & !addr12 & addr11 & addr10 &
              !coldrst_n);

END;
```