## **ST7FLITE2** Easv Reference



### **Memory Map CPU Registers** Α HW Register 007Fł SHORT ADDRESSING RAM (ZERO PAGE) 00FF RAM (384 Bytes) х TACK (UP TO 128 BYTES) 01FF 7 **Y** 15 PCH 8 7 PCL 0FFFh 1000h RCCRO DATA EEPROM (256 Bytes) RCCRI 10FF 1100 15 SP RESET VALUE = STACK HIGHER ADDRES RCCR0 RCCRI DFFFh E000h 3 1 2 FLASH MEMORY (8192 BYTES) INTERRUPT AND RESET VECTOR FFFFh 20-Pin SO 20 OSC1/CLKIN VSS 🗔 VDD OSC2 PA0 (HS)/LTIC Package SS/AINO/PB0 PA1 (HS)/ATIC ; ; \_] **/** SCK/AIN1/PB1 PA2 (HS)/ATPWM0 PA3 (HS)/ATPWM1 57 MOSI/AIN3/PB3 PA4 (HS)/ATPWM2 PA5 (HS)/ATPWM3/ICCDATA CLKIN/AIN4/PB4 O AIN5/PB5 PA6/MCO/ICCCLK/BREAK AIN6/PB6 PA7 (HS) ofTec (HS): 20 mA High-Sink Capability eix: Associated External Interrupt Vector the **Block** LVD ST7FLITE: VDD VSS POWER SUPPLY Diagram CLKIN OSC1 OSC2 INTERNAL CLOCK GENERATOR 12-BIT AUTO-RELOAD TIMER 2 MCU CONTROL RESET -8-BIT ALU 8-BIT LITE TIMER 2





### **Instruction Set**

Minemonic	Description	Operation			
ADC d, s	Add with carry, s to d	d ← d + s + C	A	mem	H, N, Z, C
ADD d, s	Add s to d	d ← d + s	A	mem	H, N, Z, C
AND d, s	Logical AND (d with s)	d ← d AND s	A	mem	N, Z
BCPs.d	Bit compare	IN.ZI ← s AND d	A	mem	N.Z.
RRFSdh	Ritracet	d = d AND (NOT (2 <sup>b</sup> ))	mem		
PCET 4 b	Pit cot	4, 408/00			
over 4 b and	have all the second second				
513F 0, 0, rei	Jump II bit is take (0)	PC + PC + NITP (G AND (2*)) = 0	mam		
BTJT d, b, rel	Jump if bit is true (1)	PC ← PC + nel IF (d AND (27)) ≠ 0	mem		C
CALL	Call subroutine	PUSH (PC); PC ← d	mem		
CALLR d	Call subroutine relative	PUSH (PC); PC ← PC + d	mem		
CLR d	Clear d	d ← 0	reg, mem		N = 0, Z = 1
CP d, s	Arithmetic compare	$(N, Z, C) \leftarrow \text{TEST} (d \cdot s)$	reg	mem	N, Z, C
CPL d	Logical 1-complement of d	$d \leftarrow d \text{ XOR FFh, or FFh} \cdot d$	reg, mem		N, Z, C = 1
DEC d	Decrement d	d ← d - 1	reg, mem		N, Z
HALT	Halt	1 ← 0			1=0
INC d	Increment d	d ← d + 1	reg, mem		N, Z
IRET	Interrupt routine return	POP CC, A, X, PC			H, I, N, Z, C
JP d	Absolute jump	PC ← d	mem		
JRA d	Jump relative always	PC ← PC + d	mem		
197.4	humo relativo aluctur	PC / PC / d			
105.4	Nour inter	10000	man		
	have beleve a the state	PC - PC - d Classer To - blab			
brunt d	Jump Relative if Port IN I prn = 1	PC ← PC + d P interrupt the high	mem		
JRILd	Jump Relative if Port INT pin = 0	PC ← PC + d IF interrupt line low	mem		
лин а	Jump Helative if H = 1	PC ← PC + d IF H = 1	mem		
JRNH d	Jump Relative if H = 0	$PC \leftarrow PC + d \parallel FH = 0$	mem		
JRM d	Jump Relative if I = 1	$PC \leftarrow PC + d \parallel F \parallel = 1$	mem		
JRNM d	Jump Relative if I = 0	$PC \gets PC + d \: IF \: I = 0$	mem		
JRMI d	Jump Relative if N = 1	$PC \gets PC + d \: IF \: N = 1$	mem		
JRPL d	Jump Relative if N = 0	$PC \gets PC + d \: IF \: N = 0$	mem		
JREQ d	Jump Relative if Z = 1	$PC \leftarrow PC + d \parallel FZ = 1$	mem		
JRNE d	Jump Relative if Z = 0	PC ← PC + d IF Z = 0	mem		
JRCd	Jump Relative if C = 1	PC ← PC + d IF C = 1	mem		
IRNCA	lumo Belative if C = 0	PC + PC + d EC = 0	mam		
INIITA	huma Polatico IC = 1	PC / PC / 415 C - 1			
IDUICE 4	Jump Matrix I C = 1		mam		
	Jump Analyse 200 - 20		mam		
JRUGT d	Jump Nelative if (C + Z) = 0	$PC \leftarrow PC + d \gg (C OR 2) = 0$	mem		
JRULE d	Jump Helative if (C + Z) = 1	$M_{c} \leftarrow M_{c} + d \parallel F (C \text{ OR } Z) = 1$	mem		
LD d, s	Load s in d	d ← s	reg, mem	reg, mem	N, Z
MUL d, s	Multiply d by s	ds ← d * s	reg	reg	H = 0, C = 0
NEG d	Negate d (logical 2-complement)	$d \leftarrow (d XOR FFh) + 1$	reg, mem		N, Z, C
NOP	No operation				
OR d, s	Logical OR (d with s)	$d \leftarrow d  OR  s$	A	mem	N, Z
POPd	Pop from the Stack	d ← (++SP)	neg		H, I, N, Z, C
PUSH d	Push onto the Stack	(SP) ← d		reg	
RCF	Reset carry flag	C ← 0			C=0
RET	Subroutine return	POP PC			
RIM	Reset interrupt mask	100			1=0
RICA	Rotate left through carry	-	neo mem		NZC
99C 4	Rotate sight through carry		ma ma		N 7.C
nnc a	Notate right through carry	C-FITTING	Ng, mem		N, Z, C
nor .	nuset stack pointêr	SP +- reset variae			
sac d' a	Subtract s from d with carry	d ← d - s - C	A	mem	N, Z, C
SCF	Set carry flag	C ← 1			C = 1
SIM	Set interrupt mask	1←1			1-1
SLA d	Shift left arithmetic (equal to SLL d)	0-00000-0	reg, mem		N, Z, C
SLLd	Shift left logical	0-0111110-0	reg, mem		N, Z, C
SRA d	Shift right arithmetic	Garranee	reg, mem		N, Z, C
SRLd	Shift right logical	0-000000-0	reg, mem		N = 0, Z, C
SUB d, s	Subtract s from d	d ← d - s	A	mem	N, Z, C
SWAP d	Swap nibbles	d(7:4) ↔ d(3:0)	req.mem		NZ
TNZ d	Test for nenative and zero	(N 7) - TEST (4)	no mem		N Z
TRAD	Cofference interment	PC / PC / 1-915H PC V A CC-PC / Manuarter	any main		1-1
	Socrate interrupt	I c ← i c + i; Poon PC, A, A, CC, PC ← d'ap vector			
N1+1	Wart for interrupt	1←0			1=0
XOR d. s	Logical exclusive OR (d with s)	d ← d XOR s	A	mem	N.Z

SIGNAL PINS PROTOTYPE AREA 8 USB TO ICC INTERFACE RESET ROGRAM MEMOR<sup>1</sup> (8K BYTES) OSC\_CLK SPI RESET USB OSC2 USB D ICCCLK PA [0..7] ICCDATA RAM (384 BYTES) ADC + OP AMP DATA EEPRON (256 BYTES) VSS VSS VSS VSS VSS WATCHDOG ENABLE **PK-ST7FLITE2** Ş DEBUG MODULE PA7 **Block Diagram** 

VSS

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# PK-ST7FLITE2 Quickstart Tutorial







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