High Performance 8-bit Microcontrollers

Z8 Encore!® F083x Series

Programming Specification

PRS001003-1207

Flash Memory Programming Overview

Zilog's Z8 Encore!® MCU family of products are the first in line of Zilog microcontroller products, based on the 8-bit eZ8 CPU. Z8 Encore!® F083x series of products expand on Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows the faster development time and program changes in the field. The new eZ8 CPU is upward compatible with existing Z8® CPU instructions. The rich peripheral set of Z8 Encore! F083x series makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

The on-chip Flash controller can be bypassed, allowing direct control of the Flash signals through the general purpose input/output (GPIO) pins. The Flash memory can be programmed faster by controlling the Flash memory signals directly. This method is beneficial when programming a large number of devices and is helpful to those who are developing the multi-site gang programmers.

Z8 Encore! F083x reuses most of the existing test modes from Z8 Encore! XP F0822 Series Flash Microcontrollers. It supports the following modes for programming the Flash:

- Flash Test Mode
- Bypassing the Flash Controller

Only one of the above test modes can be selected at a time. Multiple combinations result in pin conflicts. Each test mode is enabled by setting the corresponding enable bit in the on-chip debugger's (OCD's) test mode register. Flash test mode can also be enabled by pulling the $\overline{\text{TESTMODE}}$ pad Low if certain conditions on the option bit states are satisfied.

Flash Test Mode

Flash test mode allows testing of the Flash memory. It is used at wafer level testing by UMC with the VPP pin to improve programming/erase times. It is also used on packaged part without the use of the VPP pin.

Setup

The setup conditions required for the Flash test mode are:

1. Apply Vdd = 3.3 V type (UMC specification), AVDD = 3.3 V.
2. Drive the $\overline{\text{TESTMODE}}$ pad Low.
3. Wait for the Power-On Reset (POR) to exit. POR is clocked by an internal RC oscillator and lasts approximately 5 ms after the brown-out threshold is passed.

Flash Test Mode Entry Prevention

If, IWP[3:0] (bits 7:4 at Flash Information Area address FE05H) is set to 0110b and FWP (bit 2 of Program Memory address 0000H) is set to 0, then Flash test mode cannot be entered. Program Memory is erased through the OCD, disabling the Flash read protect and then allowing entry into Flash test mode.

Entering Flash Test Mode

Flash test mode can be entered in two ways.

1. One way is to drive the $\overline{\text{TESTMODE}}$ pad Low. The $\overline{\text{TESTMODE}}$ pad is accessible before the part is packaged.
2. Flash test mode can also be entered by setting bit 2 in the OCDs test mode register to 1.

Bypassing the Flash Controller

Flash controller bypass mode is enabled by writing three bytes to the OCD via the DBG interface.

1. **80H**—Initiates auto-baud calculation of the DBG interface data and clock rate.
2. **F0H**—OCD write testmode register command.
3. **04H**—Data to be written to the testmode register. This enables Flash controller bypass mode.

Flash Memory Control Signals

Depending on the size (number of bytes) available in the Flash memory, the Flash memory makes use of 38 signals.

- 14 signals for the address lines.
- 8 signals for data input.
- 8 signals for data output.
- 8 user mode control signals.

The Flash memory control signals are listed and described in Table 1.

Table 1. Flash Memory Control Signals

Signal	Description
ADDR[13:0]	Address input bus
DIN[7:0]	Data input bus
DOUT[7:0]	Data output bus
AE	Address enable
CE	Chip enable
OE	Out enable, tri-state DOUT when OE=0
IFREN	Information block enable
NVSTR	Defines non-volatile store cycle
PROG	Defines program cycle
SERA	Defines Sector Erase cycle
MASE	Defines Mass Erase cycle
VDD	Power supply
GND	Ground
FME, HILO	Reserve
MUXENB, TMR	Reserve
TM[3:0]	Reserve, analog pin used in test mode

Flash Memory Operations

When bypassing the Flash controller, all Flash memory operations (Read, Program, Page Erase, and Mass Erase) are available. The mode of operation is set by the Flash memory control signals as described in Table 2. The IFREN signal is used to select between the Flash main memory and the Flash Information Area.

Table 2. User Mode Truth Table

Mode*	CE	AE	OE	PROG	SERA	MASE	DIN	DOUT	ADDR	NVSTR	IRFEN
Standby	L	L	L	L	L	L	X	Z	X	L	L
Read	H	H	H	L	L	L	X	Active	Active	L	Active
Program	H	H	L	H	L	L	Active	Z	Active	Active	Active

Table 2. User Mode Truth Table (Continued)

Sector Erase	H	H	L	L	H	L	X	Z	Active	Active	Active
Mass Erase	H	H	L	L	L	H	X	Z	X	Active	Active
*X stands for don't care, and it is necessary to bias at either "H" or "L", L stands for logic Low, H stands for logic High, and Z stands for High impedance.											

Table 3. IFREN Truth Table

Mode	IFREN=1	IFREN=0
Read	Read information block	Read main memory block
Program	Program information block	Program main memory block
Sector Erase	Erase information block	Erase selected sector
Mass Erase	Erase both block	Erase main memory block

Flash Bypass Mode Register Structure

To facilitate using Flash controller bypass mode for all package sizes, all the signals are registered internally, allowing all data access to occur through a single 8-bit GPIO port (Port A). Among the three other GPIO port pins (PortB1, PortB0, and PortC0), select one of the input data registers or the data output register as shown in Table 4.

In Flash test mode, PortA[7:0] becomes an input/output data port, and PortB[1], PortB[0], and PortC[0] form a three input register address select as shown in Table 4.

When $\overline{\text{TESTMODE}}$ pad is asserted, which is equal to 0 then:

- PadTM[0] is shared with PortB7.
- PadTM[1] is shared with PortC4.
- PadTM[2] is shared with PortC5.
- PadTM[3] is shared with PortC6.

Table 4. Flash Bypass Mode Register Structure

	Register Select [Port B1, Port B0, Port C0]						
	000	**001**	**010**	**011**	**100**	**101**	**110-111**
Input/Output	**Input**	**Input**	**Input**	**Input**	**Input**	**Output**	**Input**
Port A7	ADDR[15]	ADDR[7]	DIN[7]	AE	TMR	DOUT[7]	NOP
Port A6	ADDR14]	ADDR[6]	DIN[6]	IFREN	MUXENB	DOUT[6]	NOP
Port A5	ADDR[13]	ADDR[5]	DIN[5]	CE	NOP	DOUT[5]	NOP
Port A4	ADDR[12]	ADDR[4]	DIN[4]	OE	NOP	DOUT[4]	NOP
Port A3	ADDR[11]	ADDR[3]	DIN[3]	ERASE	NOP	DOUT[3]	NOP
Port A2	ADDR[10]	ADDR[2]	DIN[2]	PROG	NOP	DOUT[2]	NOP
Port A1	ADDR[9]	ADDR[1]	DIN[1]	MAS	NOP	DOUT[1]	NOP
Port A0	ADDR[8]	ADDR[0]	DIN[0]	NVSTR	NOP	DOUT[0]	NOP

If Flash test mode is entered through the OCD test mode register, the ERASE, PROG, MAS1, and NVSTR signals are subject to the state of ERASE_EN and PROG_EN Zilog option bits at Flash Information Area address FE05H. The IFREN signal is subject to the IWP[0] Zilog option bit at Flash Information Area address FE05H.

Driving the $\overline{\text{TESTMODE}}$ pad Low overrides all Zilog option bit settings.

Figure 1 displays the multiplexed register structure that allows access to all Flash memory signals through GPIO Port A

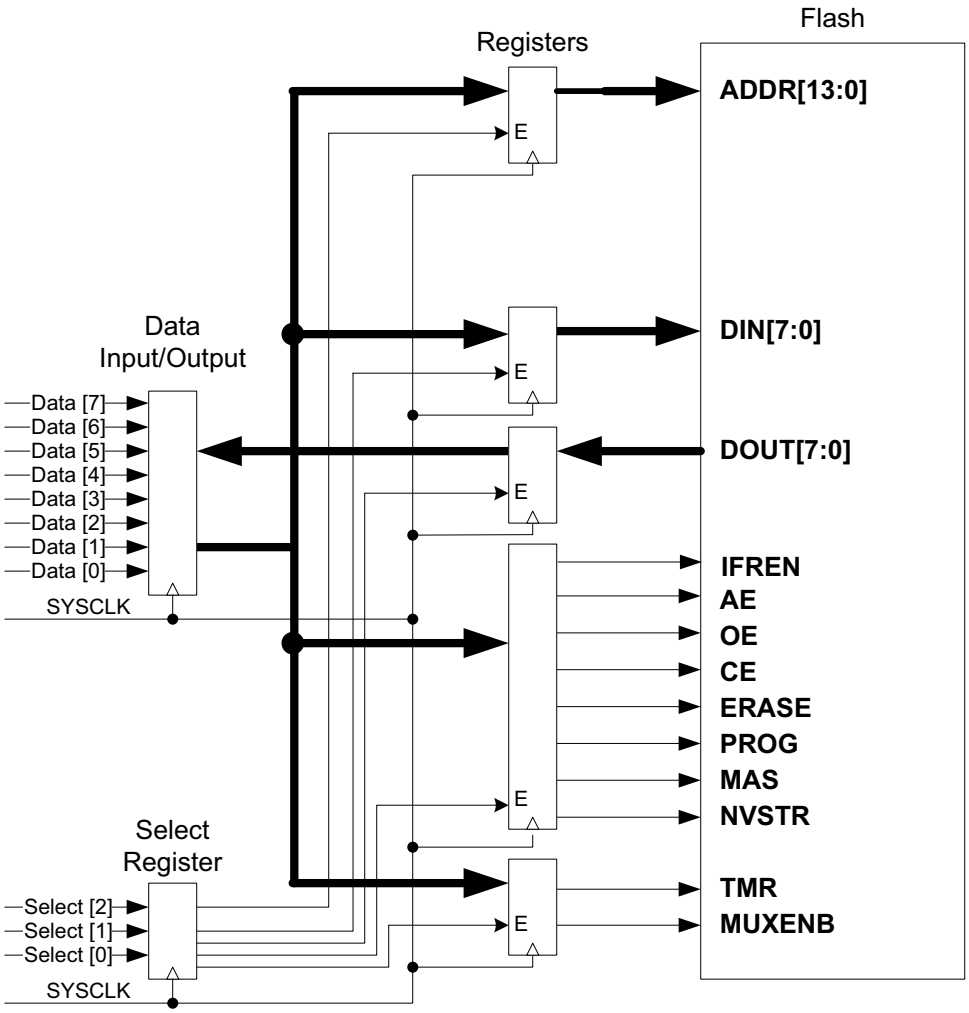

Figure 1. Flash Memory Signal Access Through GPIO Port A

Figure 2 displays the general `addr` and control signal timing based on system clock rising edge (SysClk is provided by PB3, and Select is a combined signal of PB0, PB1, and PC0). Figure 3 displays how to read data through PortA.

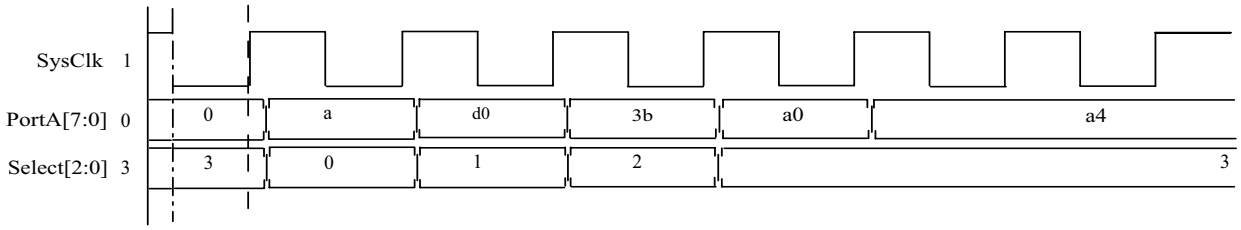

Figure 2. `addr` and Control Signal Timing

1. Set Select = 0 and apply high 8-bit `addr` onto PortA, here apply 0aH on rising edge of SysClk.
2. Set Select = 1 and apply low 8-bit `addr` onto PortA, here apply d0H on rising edge of SysClk.
3. Set Select = 2 and apply input data onto PortA, here apply 3bH on rising edge of SysClk.
4. Set Select = 3 and apply control signals onto PortA according to Flash operation type, here apply a0 and a4 on rising edge of SysClk.
5. Note the waveform between the cursor.
6. When Set Select = 5 on the rising edge of SysClk, the data will be available in the next rising edge. Since the input/output port is PortA, the default must be made high impedance.

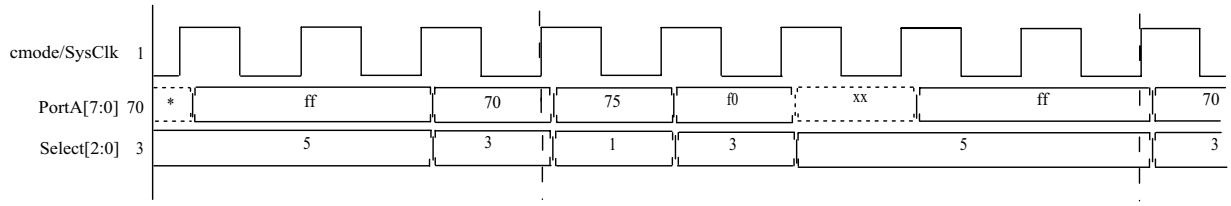

Figure 3. Read Out Data Through PortA

Bypass Mode Register Read Timing

Figure 4 displays the single read operation timing.

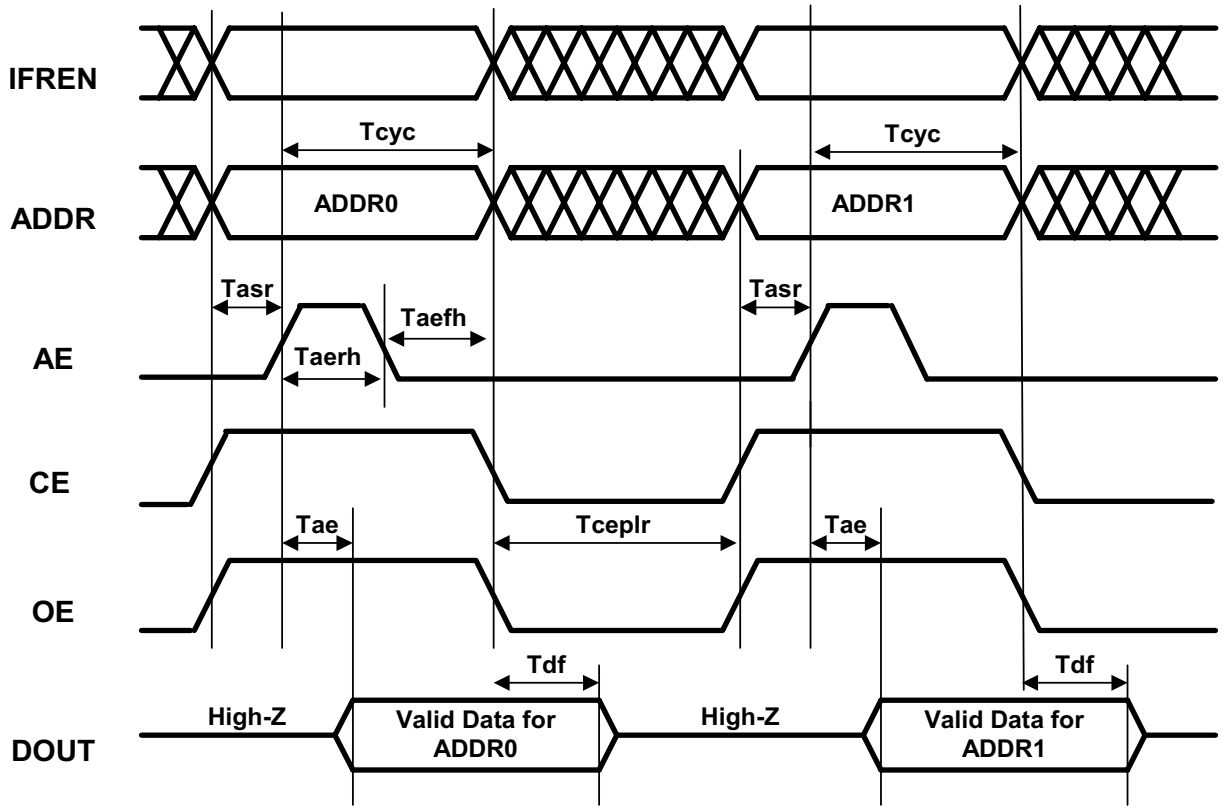

Figure 4. Single Read Operation Timing

Continuous Read Operation Timing

Figure 5 displays the continuous read operation timing. Table 5 describes the read operation parameters.

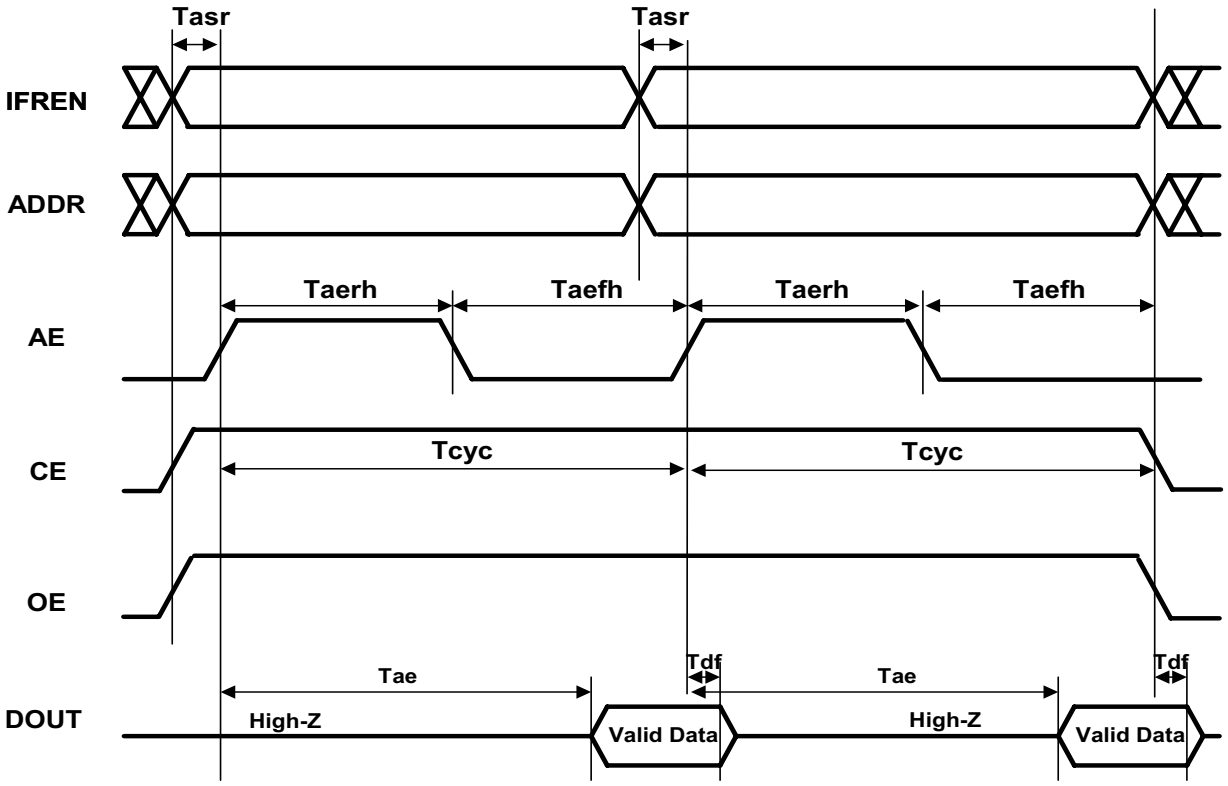

Figure 5. Continuous Read Operation Timing

Table 5. Read Operation Parameters

Parameter	Symbol	Minimum	Maximum	Unit
Address, CE, OE to AE setup time	Tasr	0	-	ns
Read cycle time	Tcyc	50	-	ns
AE pulse high hold time at Tcyc	Taerh	28	Tcyc-10	ns
AE pulse low hold time at Tcyc	Taefh	Tcyc-Taerh	Tcyc-Taerh	ns
AE access time	Tae	-	45 ns	ns
CE pulse low hold time at read	Tceplr	10	-	ns
Valid data hold time at Tcyc	Tdf	1	-	ns

Notes:

1. *During read operation, PROG, SERA, MASE, and NVSTR are always logic "L".*
2. *IFREN pin determines whether the macros, CE and AE must be asserted; otherwise macro will ignore any change from control pins and address.*
3. *To enable the macro, CE and AE must be asserted; otherwise macro will ignore any change from control pins and address.*
4. *For continuous read, Address and IFREN are allowed to be in transition.*
5. *In order to access information block, ADDR[13:7] are don't care. ADDR[6:0] are used to select one column in each I/O within the information block.*
6. *Reading operation starts from AE rising edge. Prior to AE's rising edge; CE, OE, ADDR must be valid.*
7. *All input waveforms are with rising time (tr) and falling time (tf) of 1 ns. The* capacitor *loading for the eFlash macro input pin is 0.5 pF.*
8. *Access time (Tae) is measured with 0.1 pF load capacitance.*
9. *Tdf refers to data hold time from the end of Tcyc. Output data will not be valid after Tdf.*

Flash Program Operation Timing

Figure 6 displays the program operation timing. Table 6 describes the program operation parameters.

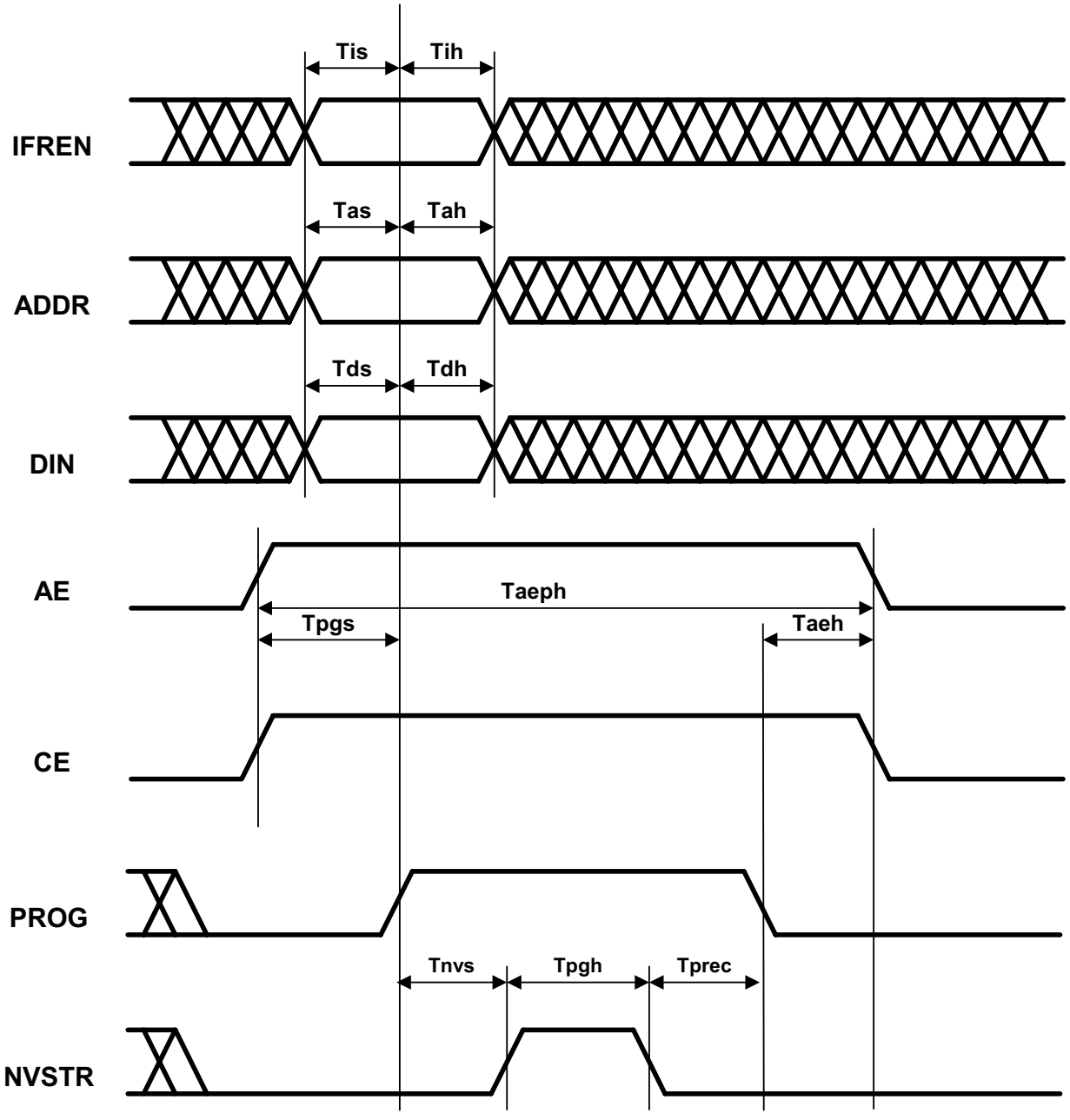

Figure 6. Program Operation Timing

Continuous Program Operation Timing

Figure 7 displays the continuous program operation timing.

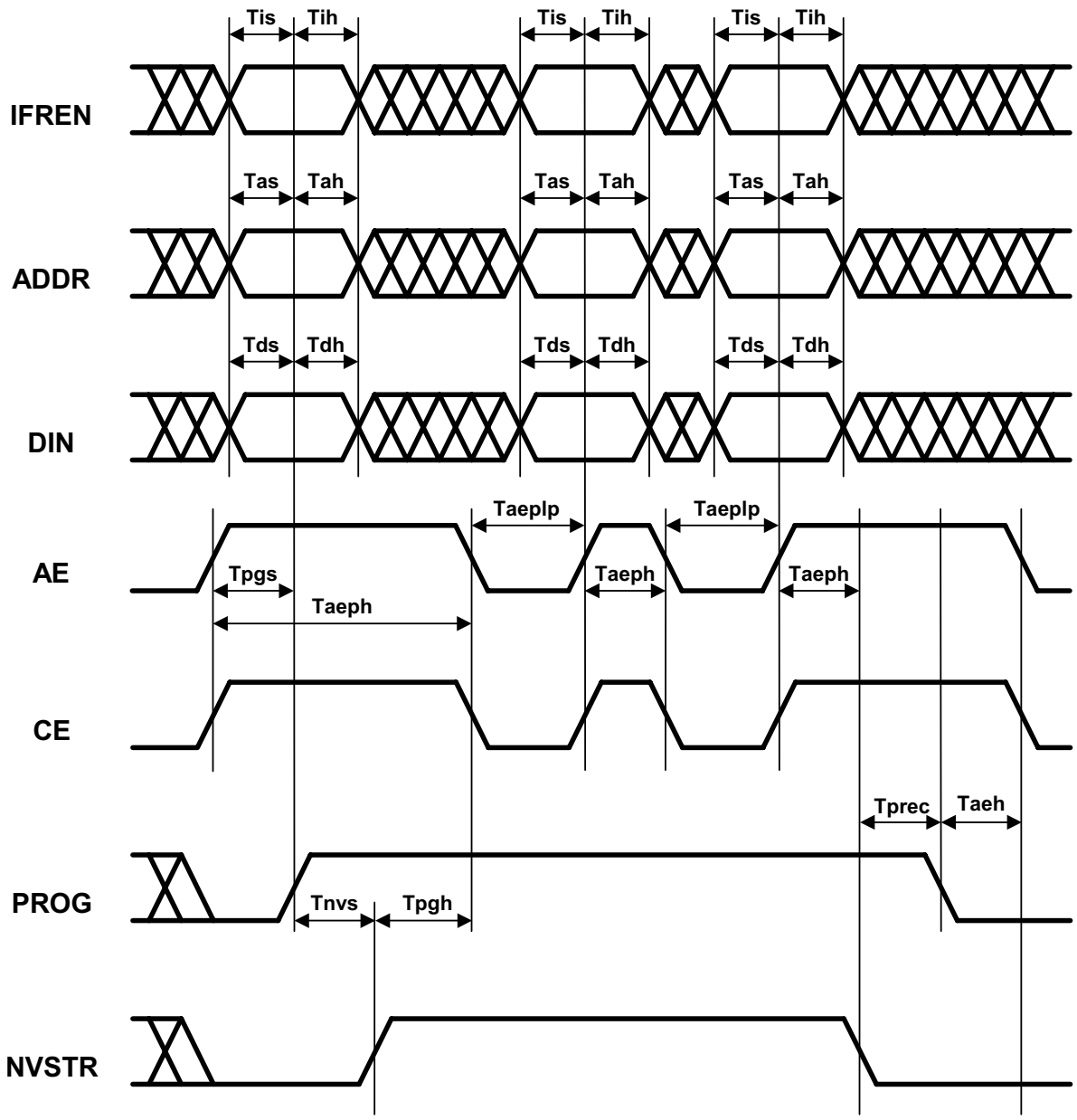

Figure 7. Continuous Program Operation Timing

Figure 8 displays the Read Operation After Program Timing.

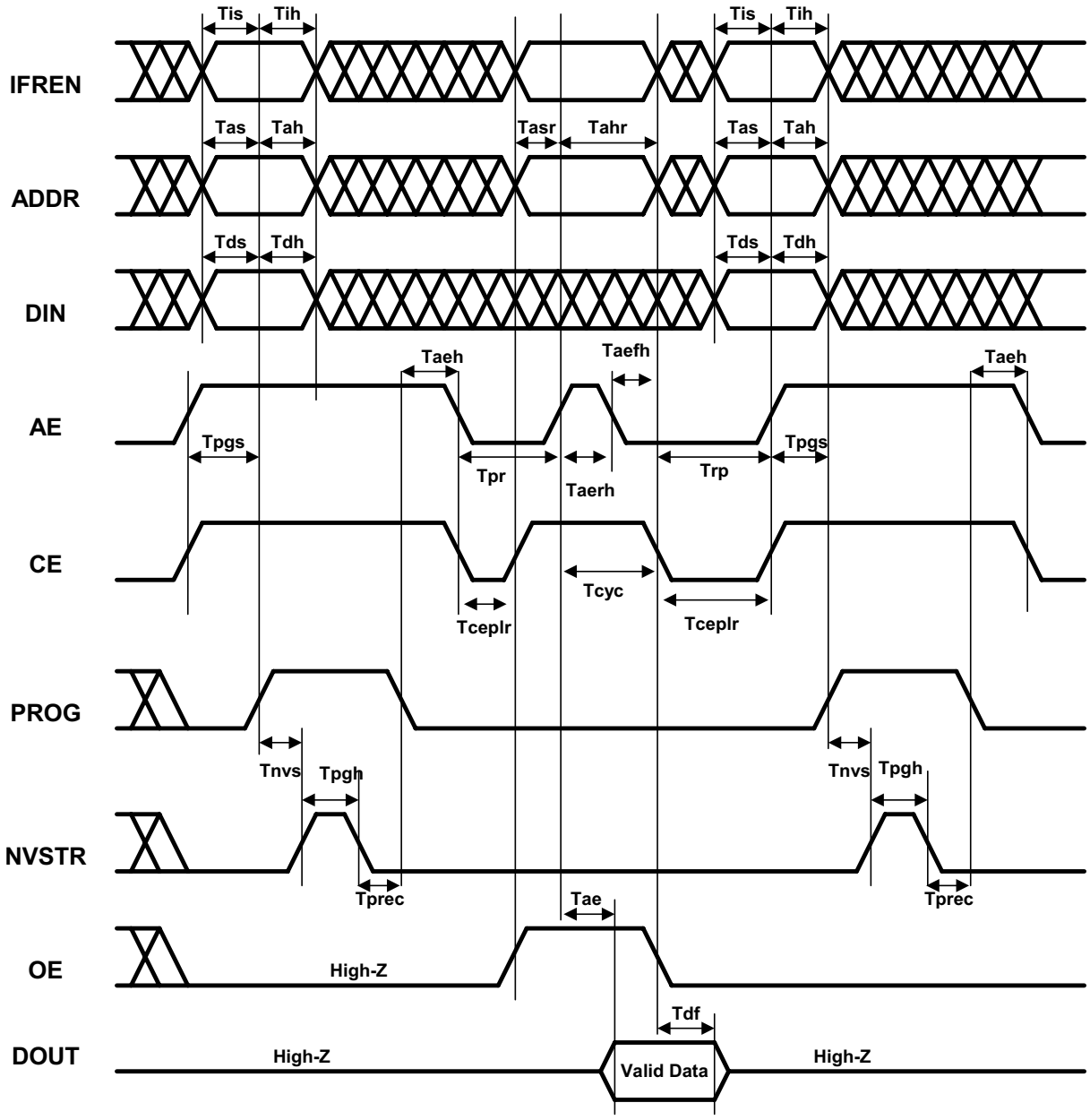

Figure 8. Read Operation After Program Timing

Table 6. Program Operation Parameters

Parameter	Symbol	Min.	Max.	Unit
Read cycle time	Tcyc	50	-	ns
Program setup time	Tpgs	20	-	ns
AE enable program hold time	Taeph	20	-	µs
NVSTR setup time	Tnvs	120	-	ns
Program hold time	Tpgh	20	-	µs
Program recovery time	Tprec	3	-	µs
AE hold time	Taeh	0	-	ns
IFREN setup time in program	Tis	0	-	ns
IFREN hold time in program	Tih	20	-	ns
Address setup time	Tas	0	-	ns
Address hold time	Tah	20	-	ns
Data setup time	Tds	0	-	ns
Data hold time	Tdh	20	-	ns
Address setup time at Tcyc	Tasr	0	-	ns
Address hold time at Tcyc	Tahr	Tcyc	-	ns
AE pulse high hold time at Tcyc	Taerh	28	Tcyc-10	ns
AE pulse low hold time at Tcyc	Taefh	Tcyc-Taerh	Tcyc-Taerh	ns
AE access time	Tae	-	45 ns	ns
AE to output high Z	Tdf	1	-	ns
AE pulse low hold time at PGM	Taeplp	40	-	ns
AE disable hold time in PGM and read	Tpr	10	-	ns
AE disable hold time in PGM and read	Trp	10+Taefh	-	ns
CE pulse low hold time at PGM	Tceplr	10	-	ns

Notes: 1. *During program operation, PROG is high, and SERA and MASE are always logic "L".*

2. *IFREN pin determines, whether the data will be programmed in main memory block or information block.*

3. *For information block programming, ADDR [13:7] are don't care. ADDR [6:0] are used to select one column in each I/O within the information block.*
4. *If you do not follow the timing spec such as Tnvs and Tprec, it may cause fatal damage*.
5. *No recovery time required from standby to first read and first program.*
6. *All input waveforms are with rising time (tr) and falling time (tf) of 1 ns. The* capacitor *loading for all the eFlash macro input pin is 0.5 pF.*
7. *Access time (Tae) is measured with 0.1 pF loading capacitance*
8. *Tdf means data hold time from the end of Tcyc. Output data will not be valid after Tdf.*

Sector Erase Operation Timing

The main memory block is organized into twenty-four 4 K bits uniform sectors. The information block contains one single sector of 1 Kb. A Sector Erase operation allows erasing any individual sector. Pre-programming the sector is not required prior to Sector Erase operation. CE, AE, SERA, NVSTR, and IFREN signals activate a Sector Erase operation. The sector addresses are latched on the rising edge of SERA.

The Sector Erase operation is similar to Mass Erase operation except the addresses; and IFREN will be used to select the sector for erasure. Each Sector Erase operation erases one sector at a time. The IFREN signal determines whether to erase a sector in main memory block or information block. If IFREN is pulled low (VIL), the main memory sector will be erased. Similarly, if IFREN is pulled high (VIH), the information block will be erased. The internal erasure voltages and timing is controlled by NVSTR signal. Figure 9 displays the Sector Erase operation timing.

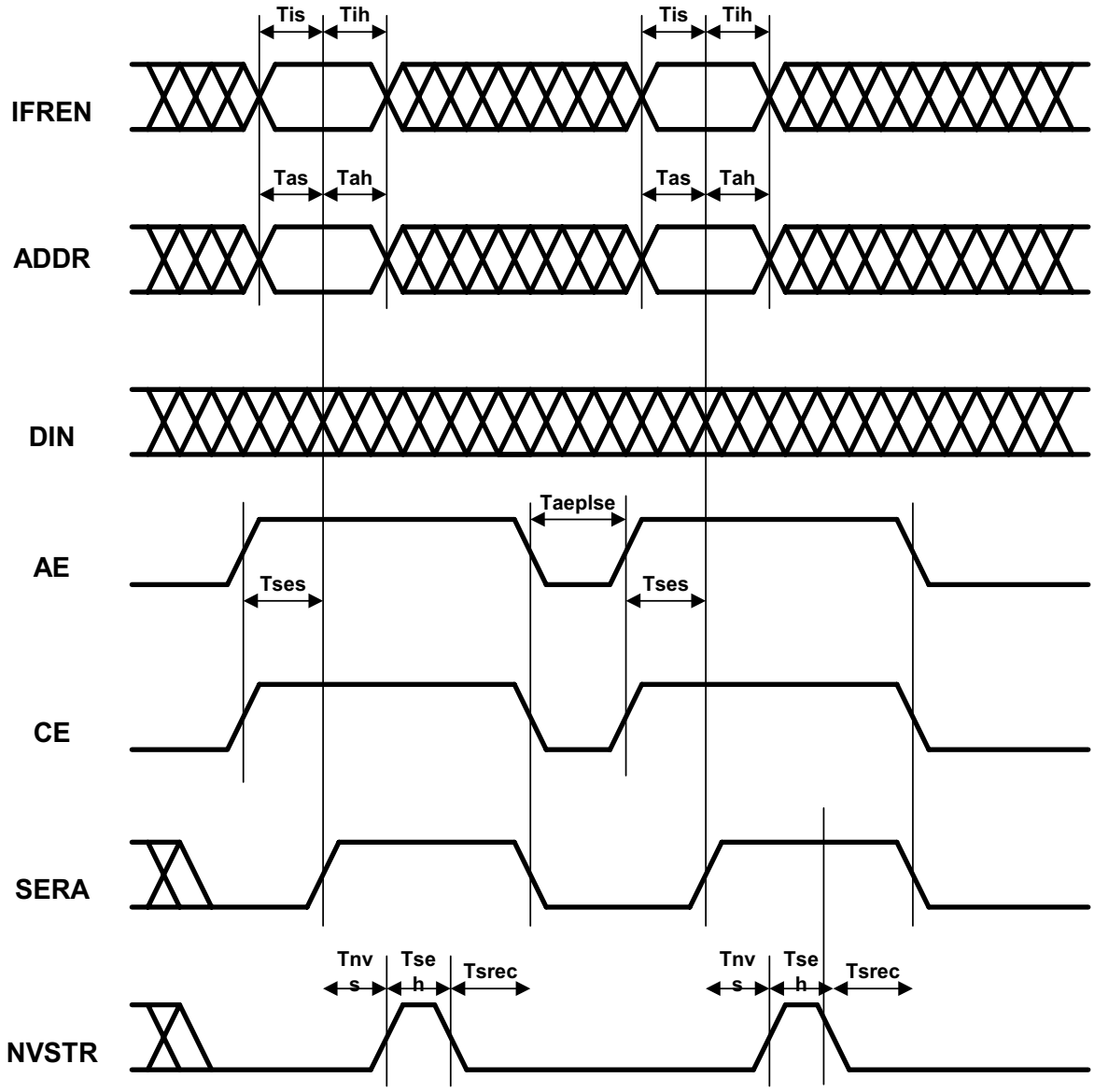

Figure 9. Sector Erase Operation Timing

Read Operation After Sector Erase Timing

Figure 10 displays the read operation after Sector Erase timing. Table 7 describes the erase operation parameters.

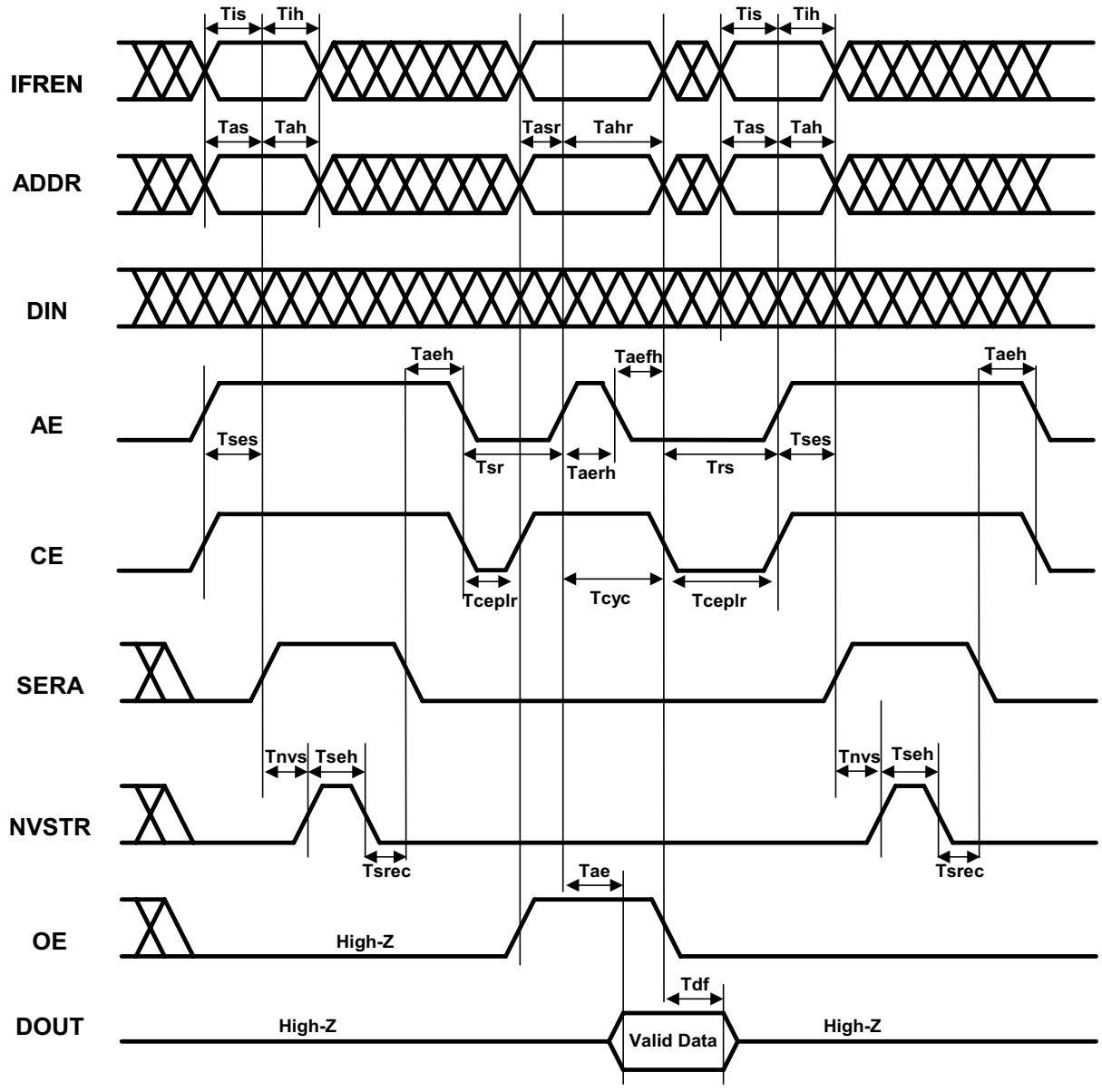

Figure 10. Read Operation After Sector Erase Timing

Table 7. Sector Erase Operation Parameters

Parameter	Symbol	Min.	Max.	Unit
Read cycle time	Tcyc	50	-	ns
Sector Erase setup time	Tses	20	-	ns
NVSTR setup time	Tnvs	120	-	ns
Sector Erase hold time	Tseh	50	80	ms
Sector Erase recovery time	Tsrec	100	-	µs
AE hold time	Taeh	0	-	ns
IFREN setup time in SERA	Tis	0	-	ns
IFREN hold time in SERA	Tih	20		ns
Address setup time	Tas	0	-	ns
Address hold time	Tah	20	-	ns
Address setup time at read	Tasr	0		ns
Address hold time at read	Tahr	Tcyc		ns
AE pulse high hold time at Tcyc	Taerh	28	Tcyc-10	ns
AE pulse low hold time at Tcyc	Taefh	Tcyc-Taerh	Tcyc-Taerh	ns
AE access time	Tae	-	45 ns	ns
AE to output high Z	Tdf	1	-	ns
AE pulse low hold time at SERA	Taeplse	10		ns
AE disable hold time in SERA and read	Tsr	10	-	ns
AE disable hold time in read and SERA	Trs	10	-	ns
CE pulse low hold time at ERASE	Tceplr	10	-	ns

Notes:
1. *During Sector Erase operation, SERA is high, and OE, PROG, MASE are always logic "L".*
2. *IFREN pin determines, whether the main memory block or information block will be erased.*
3. *One sector is composed of four rows and 1024 columns and information block has just one row with the same number of column with main array block.*
4. *The sector addresses (A13~A9) is required to be latched triggered by SERA signal, the rest of addresses and data inputs are don't care.*

5. *If you do not follow the timing specification such as Tnvs and Tsrec it may cause fatal damage.*
6. *All input waveforms are with rising time (tr) and falling time (tf) of 1 ns. The capacitor loading for all the eFlash macro input pin is 0.5 pF.*
7. *Access time (Tae) is measured with 0.1 pF loading capacitance.*
8. *Tdf means data hold time from the end of Tcyc. Output data will not be valid after Tdf.*

Flash Mass Erase Timing

The Flash memory can also be mass erased using the Flash controller, but only by using the OCD. Mass erasing the Flash memory sets all bytes to the value FFH. With the Flash controller unlocked and the Mass Erase successfully enabled, writing the value 63H to the Flash control register initiates the Mass Erase operation. While the Flash controller executes the Mass Erase operation, the eZ8 CPU idles, but the system clock and on-chip peripherals continues to operate. Using the OCD, poll the Flash status register to determine when the Mass Erase operation is complete. When the Mass Erase is complete, the Flash controller returns to its locked state. Figure 11 displays the Mass Erase operation timing.

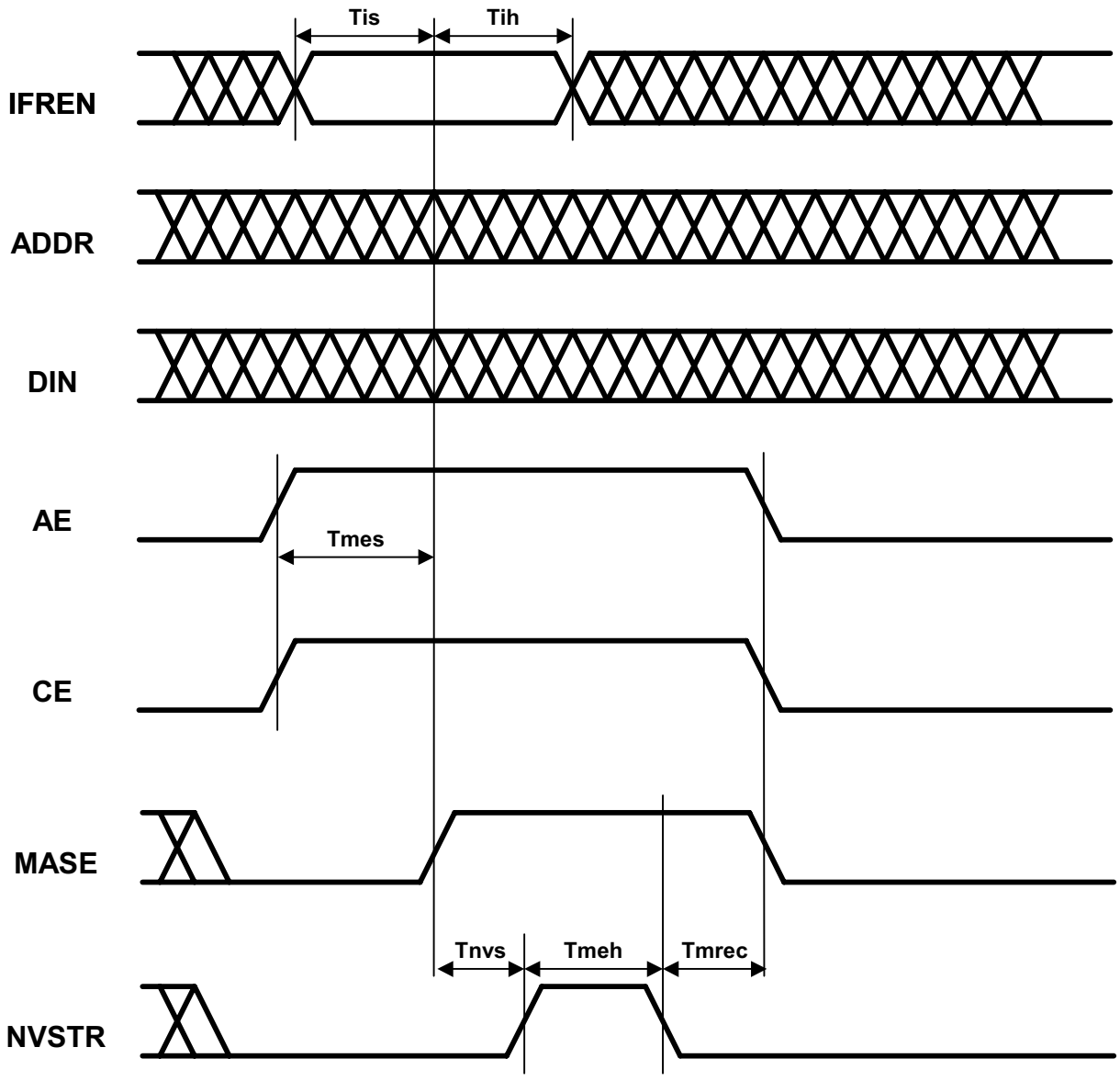

Figure 11. Mass Erase Operation Timing

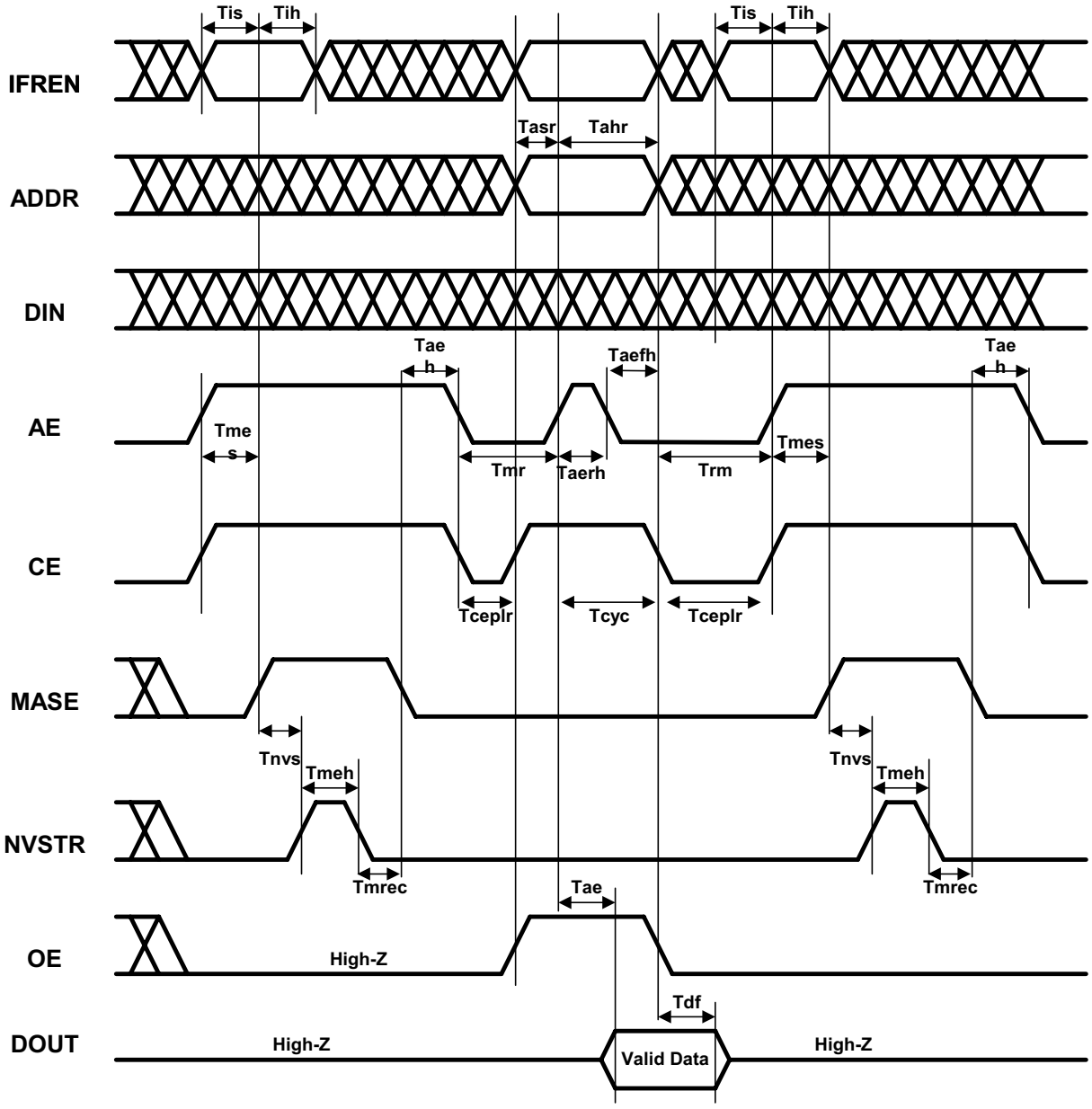

Figure 12. Read Operation After Mass Erase Operation Timing

Table 8. Mass Erase Operation Parameters

Parameter	Symbol	Min.	Max.	Unit
Read cycle time	Tcyc	50	-	ns
Mass erase setup time	Tmes	20	-	ns
NVSTR setup time	Tnvs	120	-	ns
Mass Erase hold time	Tmeh	50	80	ms
Mass Erase recovery time	Tmrec	100	-	µs
AE hold time	Taeh	0	-	ns
IFREN setup time in ME	Tis	0	-	ns
IFREN hold time in ME	Tih	20		ns
Address setup time at read	Tasr	0	-	ns
Address hold time at read	Tahr	Tcyc	-	ns
AE pulse high hold time at Tcyc	Taerh	28	Tcyc-10	ns
AE pulse low hold time at Tcyc	Taefh	Tcyc-Taerh	Tcyc-Taerh	ns
AE access time	Tae	-	45 ns	ns
AE to output high Z	Tdf	1	-	ns
AE disable hold time in ME and read	Tmr	10	-	ns
AE disable hold time in read and ME	Trm	10	-	ns
CE pulse low hold time at MASE	Tceplr	10	-	ns

Notes:
1. *During Mass Erase operation, MASE is high, and OE, PROG, SERA are always logic "L".*
2. *IFREN pin determines whether, both the main memory block and information block, or only the main memory block will be erased.*
3. *All memory cell will be erased to "1". During this mode, information block will be erased when IFREN is high.*
4. *All addresses and data inputs are don't care for Mass Erase operation.*
5. *If you do not follow the timing specification such as Tnvs and Tmrec it may cause fatal damage.*
6. *All input waveforms are with rising time (tr) and falling time (tf) of 1 ns. The capacitor loading for all the eFlash macro input pin is 0.5 pF.*

7. *Access time (Tae) is measured with 0.1 pF loading capacitance.*
8. *Tdf means data hold time from the end of Tcyc. Output data will not be valid after Tdf.*

Z8 Encore!® F083x Flash Programming Flowchart

Figure 13 displays an example flowchart for read and write operations.

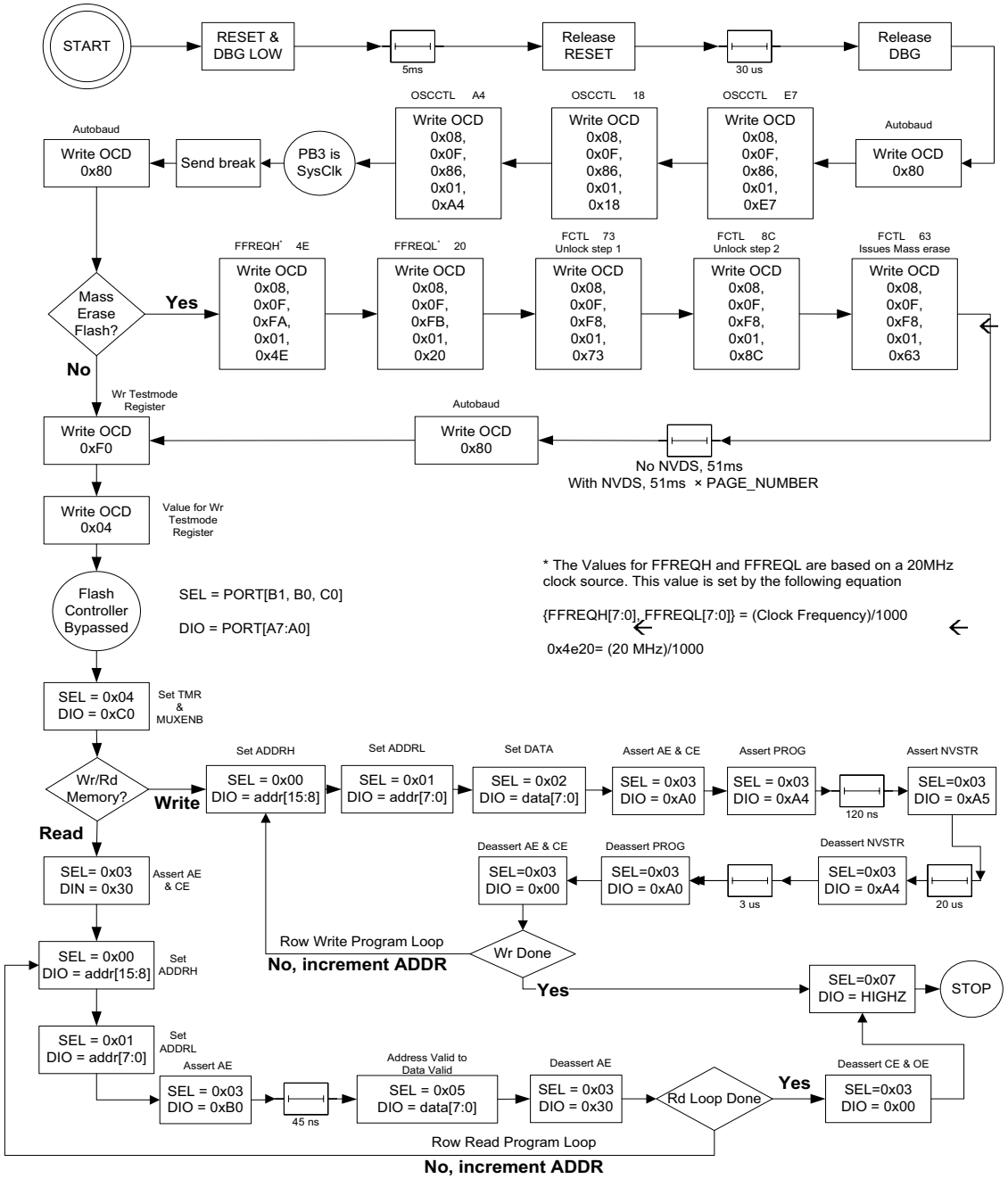

Figure 13. Z8 Encore!® F083x Flash Programming Flowchart