ADuC842/843 MicroConverter® Quick Reference Guide

Instruction Set

Data Transfer Operations

		bytes	OSC periods
MOV A,Rn	move	1	1
MOV A,@Ri		1	2
MOV A,direct		2	2
MOV A,#data		2	2
MOV Rn,A		1	1
MOV Rn,direct		2	2
MOV Rn,#data		2	2
MOV direct,A		2	2
MOV direct,Rn		2	2
MOV direct,@Ri		2	2
MOV direct,direct		3	3
MOV direct,#data		3	3
MOV @Ri,A		1	2
MOV @Ri,direct		2	2
MOV @Ri,#data		2	2
MOV DPTR,#data16		3	3
MOVC A,@A+DPTR	move from code memory	1	4
MOVC A,@A+PC		1	4
MOVX A,@Ri	move to/from data memory	1	4
MOVX A,@DPTR		1	4
MOVX @Ri,A		1	4
MOVX @DPTR,A		1	4
PUSH direct	push onto stack	2	2
POP direct	pop from stack	2	2
XCH A,Rn	exchange bytes	1	1
XCH A,@Ri		1	2
XCH A,direct		2	2
XCHD A,@Ri	exchg low digits	1	2

Arithmetic Operations

		bytes	OSC periods
ADD A,Rn	add source to A	1	1
ADD A,@Ri		1	2
ADD A,direct		2	2
ADD A,#data		2	2
ADDC A,Rn	add with carry	1	1
ADDC A,@Ri		1	2
ADDC A,direct		2	2
ADDC A,#data		2	2
SUBB A,Rn	subtract from A with borrow	1	1
SUBB A,@Ri		1	2
SUBB A,direct		2	2
SUBB A,#data		2	2
INC A	increment	1	1
INC Rn		1	1
INC @Ri		1	2
INC direct		2	2
INC DPTR *		1	3
DEC A	decrement	1	1
DEC Rn		1	1
DEC @Ri		1	2
DEC direct		2	2
MUL AB	multiply A by B	1	9
DIV AB	divide A by B	1	9
DA A	decimal adjust	1	2

* INC DPTR increments the 24bit value DPP/DPH/DPL

Boolean Variable Manipulation

		bytes	OSC periods
CLR C	clear bit to zero	1	1
CLR bit		2	2
SETB C	set bit to one	1	1
SETB bit		2	2
CPL C	complement bit	1	1
CPL bit		2	2
ANL C,bit	AND bit with C	2	2
ANL C,/bit	AND (NOTbit) with C	2	2
ORL C,bit	OR bit with C	2	2
ORL C,/bit	OR (NOTbit) with C	2	2
MOV C,bit	move bit to bit	2	2
MOV bit,C		2	2

Logical Operations

		bytes	OSC periods
ANL A,Rn	logical AND	1	1
ANL A,@Ri		1	2
ANL A,direct		2	2
ANL A,#data		2	2
ANL direct,A		2	2
ANL direct,#data		3	3
ORL A,Rn	logical OR	1	1
ORL A,@Ri		1	2
ORL A,direct		2	2
ORL A,#data		2	2
ORL direct,A		2	2
ORL direct,#data		3	3
XRL A,Rn	logical XOR	1	1
XRL A,@Ri		1	2
XRL A,direct		2	2
XRL A,#data		2	2
XRL direct,A		2	2
XRL direct,#data		3	3
CLR A	clear A to zero	1	1
CPL A	complement A	1	1
RL A	rotate A left	1	1
RLC A	....through C	1	1
RR A	rotate A right	1	1
RRC A	....through C	1	1
SWAP A	swap nibbles	1	1

Program Branching

		bytes	OSC periods
ACALL addr11	call subroutine	2	3
LCALL addr16		3	4
RET	return from sub.	1	4
RETI	return from int.	1	4
AJMP addr11	jump	2	3
LJMP addr16		3	4
SJMP rel		2	3
JMP @A+DPTR		1	3
JC rel	jump if C set	2	3
JNC rel	jmp if C not set	2	3
JB bit,rel	jump if bit set	3	4
JNB bit,rel	jmp if bit not set	3	4
JBC bit,rel	jmp&clear if set	3	4
JZ rel	jump if A = 0	2	3
JNZ rel	jump if A not 0	2	3
CJNE A,direct,rel	compare and jump if not equal	3	4
CJNE A,#data,rel		3	4
CJNE Rn,#data,rel		3	4
CJNE @Ri,#data,rel		3	4
DJNZ Rn,rel	decrement and jump if not zero	2	3
DJNZ direct, rel		3	4
NOP	no operation	1	1

Legend

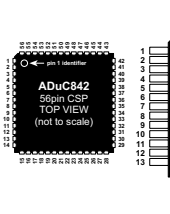
Rn	register addressing using R0-R7
@Ri	indirect addressing using R0 or R1
direct	8bit internal address (00h-FFh)
#data	8bit constant included in instruction
#data16	16bit constant included in instruction
bit	8bit direct address of bit
rel	signed 8bit offset
addr11	11bit address in current 2K page
addr16	16bit address
x	any of: Rn, @Ri, direct, #data

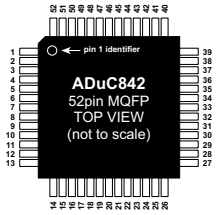
Instructions That Affect Flags

ADD A,x	C = carry out of bit 7 AC = carry out of bit 3 OV = carry out of bit 6, but not 7	DA A	C = C *or* (x>100)
		RRC A	C = ACC.7
ADDC A,x	C = carry out of bit 7 AC = carry out of bit 3 OV = carry out of bit 6, but not 7	RLC A	C = ACC.0
		SETB C	C = 1
		CLR C	C = 0
SUBB A,x	C = borrow into bit 7 AC = borrow into bit 3 OV = borrow into bit 6, but not 7	ANL C,bit	C = C *and* bit
		ANL C,/bit	C = C *and* NOTbit
		ORL C,bit	C = C *or* bit
MUL AB	C = 0 OV = (result>255)	ORL C,/bit	C = C *or* NOTbit
		MOV C,bit	C = bit
DIV AB	C = 0 OV = divide by zero	CJNE x,y,rel	C = (x<y)

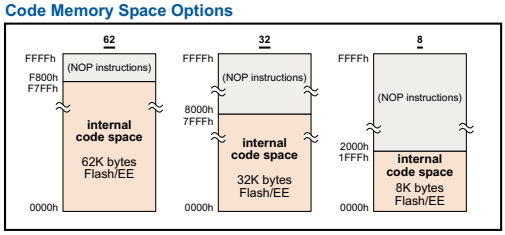
Pin Functions

MQFP	CSP	
1	56	P1.0 / ADC0 / T2
2	1	P1.1 / ADC1 / T2EX
3	2	P1.2 / ADC2
4	3	P1.3 / ADC3
5	4,5	AV_{DD}
6	6,7,8	AGND
7	9	C_{REF}
8	10	V_{REF}
9	11	DAC0
10	12	DAC1
11	13	P1.4 / ADC4
12	14	P1.5 / ADC5 / $\overline{SS}$
13	15	P1.6 / ADC6
14	16	P1.7 / ADC7
15	17	RESET
16	18	P3.0 / RxD
17	19	P3.1 / TxD
18	20	P3.2 / $\overline{INT0}$
19	21	P3.3/$\overline{INT1}$/MISO/PWM1
20	22	DV_{DD}
21	23	DGND
22	24	P3.4 / T0 / PWMC / PWM0 / EXTCLK
23	25	P3.5 / T1 / $\overline{CONVST}$
24	26	P3.6 / $\overline{WR}$
25	27	P3.7 / $\overline{RD}$
26	28	SCLOCK
27	29	SDATA / MOSI
28	30	P2.0 / A8 / A16
29	31	P2.1 / A9 / A17
30	32	P2.2 / A10 / A18
31	33	P2.3 / A11 / A19
32	34	XTAL1 (in)
33	35	XTAL2 (out)
34	36	DV_{DD}
35	37,38	DGND
36	39	P2.4 / A12 / A20
37	40	P2.5 / A13 / A21
38	41	P2.6/A14/A22/PWM0
39	42	P2.7/A15/A23/PWM1
40	43	$\overline{EA}$
41	44	$\overline{PSEN}$
42	45	ALE
43	46	P0.0 / AD0
44	47	P0.1 / AD1
45	48	P0.2 / AD2
46	49	P0.3 / AD3
47	50	DGND
48	51	DV_{DD}
49	52	P0.4 / AD4
50	53	P0.5 / AD5
51	54	P0.6 / AD6
52	55	P0.7 / AD7





Code Memory Space Options



Interrupt Vector Addresses

Interrupt Bit	Interrupt Name	Vector Address	Relative Priority
PSMCON.5	Power Supply Monitor Interrupt	43h	1
WDS	WatchDog Timer Interrupt	5Bh	2
IE0	External Interrupt 0	03h	3
ADCI	End of ADC Conversion Interrupt	33h	4
TF0	Timer0 Overflow Interrupt	0Bh	5
IE1	External Interrupt 1	13h	6
TF1	Timer1 Overflow Interrupt	1Bh	7
ISPI/I2CI	SPI/I²C Interrupt	3Bh	8
RI/TI	UART Interrupt	23h	9
TF2/EXF2	Timer2 Interrupt	2Bh	10
TIMECON.2	Time Interval Counter Interrupt	53h	11

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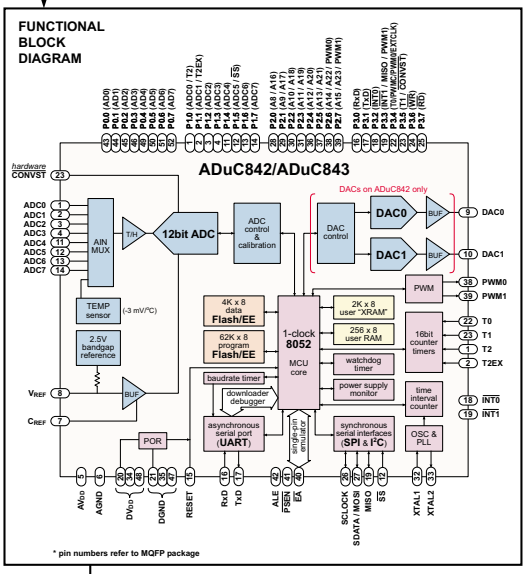
FUNCTIONAL BLOCK DIAGRAM



A *Precision Analog* Flash MCU

The ADuC842/ADuC843 is:

ADC:
12bit, 5µs, 8channel, self calibrating
0.5LSB INL & 70dB SNR

DAC (ADuC842 only):
dual, 12bit, 15µs, voltage output
<1LSB DNL

Flash/EEPROM:
62K bytes Flash/EE program memory
4K bytes Flash/EE data memory

Microcontroller:
"single-cycle" 8052, up to 16.8MIPS
32 I/O lines, programmable PLL clock
(131KHz to 16.8MHz from 32KHz crystal)

Embedded Tools Support:
on-chip download/debug & single-pin emulation functions

Other on-chip features:
temperature monitor, power supply monitor, watchdog timer, flexible serial interface ports, voltage reference, time interval counter, dual 8/16bit PWM, power-on-reset

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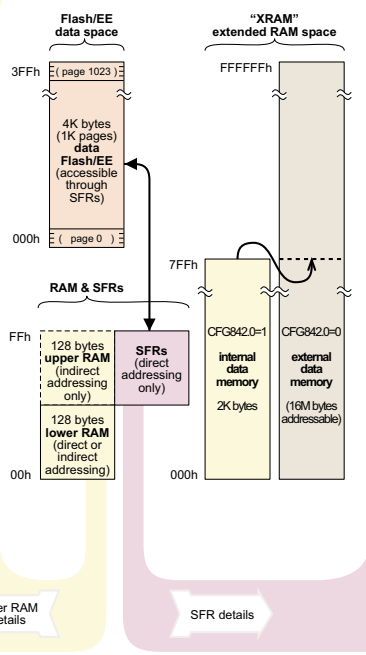
Data Memory: RAM, SFRs, user Flash/EE (all read/write)

Lower RAM

decimal address	HEX address		MSB address			(bit addresses)				LSB address
127	7Fh	General Purpose Area								
...	...									
48	30h									
47	2Fh	Bit Addressable Area	7Fh	7Eh	7Dh	7Ch	7Bh	7Ah	79h	78h
46	2Eh		77h	76h	75h	74h	73h	72h	71h	70h
45	2Dh		6Fh	6Eh	6Dh	6Ch	6Bh	6Ah	69h	68h
44	2Ch		67h	66h	65h	64h	63h	62h	61h	60h
43	2Bh		5Fh	5Eh	5Dh	5Ch	5Bh	5Ah	59h	58h
42	2Ah		57h	56h	55h	54h	53h	52h	51h	50h
41	29h		4Fh	4Eh	4Dh	4Ch	4Bh	4Ah	49h	48h
40	28h		47h	46h	45h	44h	43h	42h	41h	40h
39	27h		3Fh	3Eh	3Dh	3Ch	3Bh	3Ah	39h	38h
38	26h		37h	36h	35h	34h	33h	32h	31h	30h
37	25h		2Fh	2Eh	2Dh	2Ch	2Bh	2Ah	29h	28h
36	24h		27h	26h	25h	24h	23h	22g	21h	20h
35	23h		1Fh	1Eh	1Dh	1Ch	1Bh	1Ah	19h	18h
34	22h		17h	16h	15h	14h	13h	12h	11g	10h
33	21h		0Fh	0Eh	0Dh	0Ch	0Bh	0Ah	09h	08h
32	20h		07h	06h	05h	04h	03h	02h	01h	00h
31	1Fh	R7	Register Bank 3							
30	1Eh	R6								
29	1Dh	R5								
28	1Ch	R4								
27	1Bh	R3								
26	1Ah	R2								
25	19h	R1								
24	18h	R0								
23	17h	R7	Register Bank 2							
22	16h	R6								
21	15h	R5								
20	14h	R4								
19	13h	R3								
18	12h	R2								
17	11h	R1								
16	10h	R0								
15	0Fh	R7	Register Bank 1							
14	0Eh	R6								
13	0Dh	R5								
12	0Ch	R4								
11	0Bh	R3								
10	0Ah	R2								
9	09h	R1								
8	08h	R0								
7	07h	R7	Register Bank 0							
6	06h	R6								
5	05h	R5								
4	04h	R4								
3	03h	R3								
2	02h	R2								
1	01h	R1								
0	00h	R0								



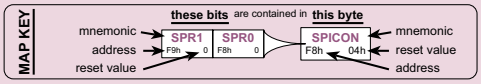
lower RAM details

SFR details

SFR Map

SPICON F8h 04h	(reserved)	(reserved)	SPIDAT F7h 00h	(reserved)	(reserved)	(reserved)	(reserved)
B F0h 00h	(reserved)	(reserved)	ADCCON1 EFh 40h	(reserved)	(reserved)	(reserved)	(reserved)
I2CCON E8h 00h	(reserved)	(reserved)	(reserved)	(reserved)	PSMCON DFh DEh	(reserved)	(reserved)
ACC E0h 00h	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	PLLCON D7h 53h	(reserved)
ADCCON2 D8h 00h	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	EADRH C7h 00h
PSW D0h 00h	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	EADRL C6h 00h
T2CON C8h 00h	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	EDATA3 BEh 00h
WDCON C0h 10h	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	EDATA4 BFh 00h
IP B8h 00h	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	SPH B7h 00h
P3 FFh 00h	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	CFG842 AFh 00h
IE A8h 00h	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	PWMCON AEh 00h
P2 A0h FFh	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	INTVAL A9h 00h
SCON 98h 00h	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	T3CON 9Bh 00h
P1 90h FFh	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(not used)
TCON 88h 00h	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(not used)
P0 80h FFh	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	PCON 87h 00h
SPR0 F9h 0	DACCON FDh 00h	DAC1H FCh 00h	DAC1L FBh 00h	DAC0H FAh 00h	DAC0L F9h 00h	SPICON F8h 04h	
SPR1 F9h 0	ADCCON3 F9h 00h	ADCGAINH F4h '00h	ADCGAINL F3h '00h	ADCOFSH F2h '20h	ADCOFSL F1h '00h	B F0h 00h	
I2CTX E9h 0	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	I2CCON E8h 00h	
I2CRS EAh 0	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	ACC E0h 00h	
CPHA F2h 0	DMAP D4h 00h	TL2 CCh 00h	RCAP2H CBh 00h	RCAP2L CAh 00h	ADCDATAH DAh 00h	ADCDATAL D9h 00h	ADCCON2 D8h 00h
I2CM E8h 0	EDATA1 BCh 00h	EDATA2 BDh 00h	PWM1H B4h 00h	PWM1L B3h 00h	PWM0H B2h 00h	PWM0L B1h 00h	PSW D0h 00h
SPIM F5h 0	I2CID0 EDh MCO 0	DMAH D3h 00h	DMAL D2h 00h	CHIPID C2h AXh	ECON C2h (reserved)	WDCON C0h 10h	T2CON C8h 00h
SPE F5h 0	I2CID1 EDh MDE 0	TH2 CDh 00h	TH1 8Dh 00h	TH0 8Ch 00h	TL1 8Bh 00h	TL0 8Ah 00h	IP B8h 00h
WCOL F5h 0	I2CGC EBh MDO 0	EADC AEh 0	ET2 ADh 0	ES ACh 0	ET1 ABh 0	EX1 AAh 0	EX0 A8h 0
ISPI F5h 0	I2CSI EBh MDO 0	PRE2 C6h 0	PRE1 C5h 0	PRE0 C4h 0	WDIR C3h 0	WDS C2h 0	WDE C1h 0
		ADCI D5h 0	DMA D6h 0	CCONV D5h 0	SCONV D4h 0	CS3 D3h 0	CS2 D2h 0
		CY D7h 0	AC D6h 0	F0 D5h 0	RS1 D4h 0	RS0 D3h 0	OV D2h 0
		TF2 CFh 0	EXF2 CEh 0	RCLK CDh 0	TCLK CCh 0	EXEN2 CBh 0	TR2 CAh 0
		PRE3 C7h 0	PADC BFh 0	PT2 BDh 0	PS BCh 0	PT1 BBh 0	PX1 BAh 0
		RD B7h 1	WR B6h 1	T1 B5h 1	T0 B4h 1	INT1 B3h 1	INT0 B2h 1
		EA AFh 0	EADC AEh 0	ET2 ADh 0	ES ACh 0	ET1 ABh 0	EX1 AAh 0
		SM0 9Fh 0	SM1 9Eh 0	SM2 9Dh 0	REN 9Ch 0	TB8 9Bh 0	RB8 9Ah 0
		TF1 8Fh 0	TR1 8Eh 0	TF0 8Dh 0	TR0 8Ch 0	IE1 8Bh 0	IE0 8Ah 0
		87h 1	86h 1	85h 1	84h 1	83h 1	82h 1
		97h 1	96h 1	95h 1	94h 1	93h 1	92h 1
		A7h 1	A6h 1	A5h 1	A4h 1	A3h 1	A2h 1
		B7h 1	B6h 1	B5h 1	B4h 1	B3h 1	B2h 1
		C7h 1	C6h 1	C5h 1	C4h 1	C3h 1	C2h 1
		D7h 1	D6h 1	D5h 1	D4h 1	D3h 1	D2h 1
		E7h 1	E6h 1	E5h 1	E4h 1	E3h 1	E2h 1
		F7h 1	F6h 1	F5h 1	F4h 1	F3h 1	F2h 1
		87h 1	86h 1	85h 1	84h 1	83h 1	82h 1
		8Fh 1	8Eh 1	8Dh 1	8Ch 1	8Bh 1	8Ah 1
		97h 1	96h 1	95h 1	94h 1	93h 1	92h 1
		A7h 1	A6h 1	A5h 1	A4h 1	A3h 1	A2h 1
		B7h 1	B6h 1	B5h 1	B4h 1	B3h 1	B2h 1
		C7h 1	C6h 1	C5h 1	C4h 1	C3h 1	C2h 1
		D7h 1	D6h 1	D5h 1	D4h 1	D3h 1	D2h 1
		E7h 1	E6h 1	E5h 1	E4h 1	E3h 1	E2h 1
		F7h 1	F6h 1	F5h 1	F4h 1	F3h 1	F2h 1

MAP KEY



* calibration coefficients are preconfigured at power-up to factory calibrated values

ADCCON1 ADC Control register #1
ADCCON1.7 ADC mode (0=off, 1=on)
ADCCON1.6 external Vref select bit (0=on-chip Vref)
ADCCON1.5 conversion time = 16 / ADCclk
ADCCON1.4 ADCclk = 16,777,216Hz / [32,4,8,2]
ADCCON1.3 acquisition time select bits
ADCCON1.2 acq time = [1,2,3,4] / ADCclk
ADCCON1.1 Timer2 convert enable
ADCCON1.0 external CONVST enable

ADCCON2 ADC Control register #2
ADCI ADC interrupt flag
DMA DMA mode enable
CCONV continuous conversion enable bit
SCONV single conversion start bit
CS3 input channel select bits:
CS2 0 - 7 = ADC0 - ADC7
CS1 8 = temperature sensor
CS0 9=DAC0_A=DAC1, B=AGND, C=VREF

ADCCON3 ADC Control register #3
ADCCON3.7 busy indicator flag (0=ADC not active)
ADCCON3.6 (this bit must contain zero)
ADCCON3.5 number of averages selection bits:
ADCCON3.4 [1\5,1\31,6\3]
ADCCON3.3 (this bit must contain zero)
ADCCON3.2 (this bit must contain one when calibrating)
ADCCON3.1 cal type select (0=offset, 1=gain)
ADCCON3.0 start calibration bit, cleared by hardware

ADCDATAH
ADCDATAL ADC Data registers

DMAP,DMAH,DMAL DMA address pointer

ADCGAINH
ADCGAINL ADC Gain calibration coefficients

ADCOFSH
ADCOFSL ADC Offset calibration coefficients

DACCON DAC Control register
DACCON.7 ModeSelect (0=12bit, 1=8bit)
DACCON.6 DAC1 RangeSelect (0=V_{REF}, 1=V_{DD})
DACCON.5 DAC0 RangeSelect (0=V_{REF}, 1=V_{DD})
DACCON.4 Clear DAC1 (0=0V, 1=normal operation)
DACCON.3 Clear DAC0 (0=0V, 1=normal operation)
DACCON.2 Synchronous\Update (1=asynchronous)
DACCON.1 PowerDown DAC1 (0=off, 1=on)
DACCON.0 PowerDown DAC0 (0=off, 1=on)

DAC1H,DAC1L DAC1 data registers

DAC0H,DAC0L DAC0 data registers

PLLCON PLL Control register
PLLCON.7 oscillator powerdown control bit (0=XTAL on)
PLLCON.6 PLL lock indicator flag (0=out of lock)
PLLCON.5 (this bit must contain zero)
PLLCON.4 (this bit must contain zero)
PLLCON.3 "fast interrupt" control bit (0=normal)
PLLCON.2 3-bit clock divider value, "CD" (default=3):
PLLCON.1 $F_{CORE} = 16,777,216Hz / 2^{CD}$
PLLCON.0

TIMECON Time Interval Counter Control Register
TIMECON.6 24-hour mode select (0=0..255hour, 1=0..23hour)
TIMECON.5 INTVAL timebase select bits
TIMECON.4 [128th sec, seconds, minutes, hours]
TIMECON.3 single time interval control bit (0=reload&restart)
TIMECON.2 time interval interrupt bit, "TII"
TIMECON.1 time interval enable bit (0=disable&clear)
TIMECON.0 time clock enable bit (0=disable)

INTVAL TIC Interval Register

HTHSEC TIC Elapsed 128th Second Register
SEC TIC Elapsed Seconds Register
MIN TIC Elapsed Minutes Register
HOUR TIC Elapsed Hours Register

ECON Data Flash/EE command register
01h READ page 82h PROGRAM byte
02h PROGRAM page 0Fh EXIT ULOAD mode
04h VERIFY page F0h ENTER ULOAD mode
05h ERASE page (all others reserved)
06h ERASE ALL

EADRH,EADRL Data Flash/EE address registers

EDATA1,EDATA2,EDATA3,EDATA4 Data Flash/EE data registers

SPICON SPI Control register
ISPI SPI interrupt (set by hardware at end of SPI transfer)
WCOL write collision error flag
SPE SPI enable (0=I^2C enable, 1=SPI enable)
SPIM master mode select (0=slave)
CPOL clock polarity select (0=SCLK idles low)
CPHA clock phase select (0=leading edge latch)
SPR1 SPI bit rate select bits:
SPR0 bitrate = F_{CORE} / [2,4,8,16] (slave: SPR0=SS)

SPIDAT SPI Data register

I2CCON I^2C Control register (in *slave mode*)
I2CSI slave mode stop interrupt enable bit (0=disable)
I2CGC slave mode general call status flag
I2CID1 slave mode interrupt decode bits
I2CID0 [start, repeated-start, data, stop]
I2CM master mode select bit (0=slave mode)
I2CRS serial port reset
I2CTX transmission direction status (0=RX,1=TX)
I2CI serial interface interrupt

I2CCON I^2C Control register (in *master mode*)
MDO master mode SDATA output bit
MDE master mode SDATA output enable (0=disable)
MCO master mode SCLK output bit
MDI master mode SDATA input bit
I2CM master mode select bit (0=slave mode)

I2CADD I^2C slave Address register

I2CADD1,I2CADD2,I2CADD3
I^2C secondary slave Address registers

I2CDAT I^2C Data register

PWMCON PWM Control register
PWMCON.7 disable P2.6/P3.4 PWM output (0=enable)
PWMCON.6 PWM mode bits (0=dual16bit, 1=single/averaging,
PWMCON.5 2=twin/8bit, 3=twin/16bit, 4=dual/16bitNRZ,
PWMCON.4 5=dual/8bit, 6=dual/16bitRZ, 7=(reserved))
PWMCON.3 PWM clock divide bit
PWMCON.2 PWM counter = clock / [1,4,16,64]
PWMCON.1 PWM clock source bits (0=F_{XTAL}/15, 1=F_{XTAL},
PWMCON.0 2=10 ext.int.rate, 3=F_{VCO}/16,777MHz)

PWM0H,PWM0L PWM0 data registers

PWM1H,PWM1L PWM1 data registers

DPCON Data Pointer Control register
DPCON.6 data pointer auto-toggle enable (0=disable)
DPCON.5 shadow data pointer mode control bits
DPCON.4 [1=8052, 2=post-inc, 3=post-dec, 4=LSBtgl]
DPCON.3 main data pointer mode control bits
DPCON.2 [1=8052, 2=post-inc, 3=post-dec, 4=LSBtgl]
DPCON.1 (not implemented to allow INC DPCON toggling)
DPCON.0 data pointer select (0=main, 1=shadow)

T3CON Timer 3 Control register
T3CON.7 Timer 3 baud rate enable (0=disable)
T3CON.2 binary divide factor (DIV)
T3CON.1 DIV = log[F_{CORE}/(16·baudrate)] / log2
T3CON.0 (rounded down)

T3FD Timer 3 Fractional Divider register
T3FD = ($2 \cdot F_{CORE}$) / (baudrate $\cdot 2^{(DIV-1)}$) - 64

CHIPID Chip ID Register (AX hex = ADuC842/843)

CFG842/CFG843 ADuC84x Config. Register
CFG842.7 extended stack-pointer enable (0=disable)
CFG842.6 PWM pins select (0=P2.6/P2.7,1=P3.4/P3.3)
CFG842.5 DAC output buffer bypass (0=buffer enabled)
CFG842.4 external clock select (0=internal clock)
CFG842.3 (this bit must contain 0)
CFG842.2 (this bit must contain 0)
CFG842.1 select SPI pins (0=default, 1=P3.3/P3.4/P3.5)
CFG842.0 internal XRAM select (0=external XRAM)

WDCON Watchdog Timer control register
PRE3 watchdog timeout selection bits
PRE2 0-7=[15.6,31.2,62.5,125,250,500,1000,2000]ms
PRE1 8=0ms (immediate reset)
PRE0 >8=reserved
WDIR watchdog interrupt response bit
WDS watchdog status flag (1 indicates watchdog timeout)
WDE watchdog enable control (0=disabled)
WDWR watchdog write enable bit (set to enable write)

PSMCON Power Supply Monitor control register
PSMCON.6 PSM status bit (1=normal / 0=fault)
PSMCON.5 PSM interrupt bit
PSMCON.4 trip point select bits
PSMCON.3 [(reserved), 3.08V, 2.93V, (reserved)]
PSMCON.2 (this bit must contain zero)
PSMCON.1 (reserved)
PSMCON.0 PSM powerdown control (1=on / 0=off)

SP Stack Pointer

SPH Stack Pointer High byte

IE Interrupt Enable register #1
EA enable interrupts (0=all interrupts disabled)
EADC enable ADCI (ADC interrupt)
ET2 enable TF2/EXF2 (Timer2 overflow interrupt)
ES enable RI/TI (serial port interrupt)
ET1 enable TF1 (Timer1 overflow interrupt)
EX1 enable IE1 (external interrupt 1)
ET0 enable TF0 (Timer0 overflow interrupt)
EX0 enable IE0 (external interrupt 0)

IEIP2 Interrupt Enable/Priority register #2
IEIP2.6 priority of TII interrupt (time interval)
IEIP2.5 priority of PSMI interrupt (power supply monitor)
IEIP2.4 priority of ISPI interrupt (serial interface)
IEIP2.3 (this bit must contain zero)
IEIP2.2 enable TII interrupt (time interval)
IEIP2.1 enable PSMI (power supply monitor interrupt)
IEIP2.0 enable ISPI interrupt (serial interface)

IP Interrupt Priority register
PADC priority of ADCI (ADC interrupt)
PT2 priority of TF2/EXF2 (Timer2 overflow interrupt)
PS priority of RI/TI (serial port interrupt)
PT1 priority of TF1 (Timer1 overflow interrupt)
PX1 priority of IE1 (external interrupt 1)
PT0 priority of TF0 (Timer0 overflow interrupt)
PX0 priority of IE0 (external interrupt 0)

TMOD Timer Mode register
TMOD.3/.7 gate control bit (0=ignore INTx)
TMOD.2/.6 counter/timer select bit (0=timer)
TMOD.1/.5 timer mode selection bits
TMOD.0/.4 [13bIT, 16bIT/C, 8bIT/Creload, 2x8bIT]
(upper nibble = Timer1, lower nibble = Timer0)

TCON Timer Control register
TF1 Timer1 overflow flag (auto cleared on vector to ISR)
TR1 Timer1 run control (0=off, 1=run)
TF0 Timer0 overflow flag (auto cleared on vector to ISR)
TR0 Timer0 run control (0=off, 1=run)
IE1 external INT1 flag (auto cleared on vector to ISR)
IT1 IE1 type (0=level trig, 1=edge trig)
IE0 external INT0 flag (auto cleared on vector to ISR)
IT0 IE0 type (0=level trig, 1=edge trig)

TH0,TL0 Timer0 registers

TH1,TL1 Timer1 registers

T2CON Timer2 control register
TF2 overflow flag
EXF2 external flag
RCLK receive clock enable (0=Timer1 used for RxD clk)
TCLK transmit clock enable (0=Timer1 used for TxD clk)
EXEN2 external enable (0=ignore T2EX, 1=cap/rld on T2EX)
TR2 run control (0=stop, 1=run)
CNT2 timer/counter select (0=timer, 1=counter)
CAP2 capture/reload select (0=reload, 1=capture)

TH2,TL2 Timer2 register

RCAP2H,RCAP2L Timer2 Reload/Capture

P0 Port0 register (also A0-A7 & D0-D7)

P1 Port1 register (analog & digital inputs)
T2EX timer/counter 2 capture/reload trigger
T2 timer/counter 2 external input

P2 Port2 register (also A8-A15 & A16-A23)

P3 Port3 register
RD external data memory read strobe
WR external data memory write strobe
T1 timer/counter 1 external input
T0 timer/counter 0 external input
INT1 external interrupt 1
INT0 external interrupt 0
TxD serial port transmit data line
RxD serial port receive data line

SCON Serial communications Control register
SM0 UART mode control bits baud rate:
SM1 00 - 8bit shiftReg $F_{CORE}/12$
01 - 8bit UART - variable
10 - 9bit UART - $F_{CORE}/64$ (x2)
11 - 9bit UART - variable
SM2 in modes 2&3, enables multiprocessor communication
REN receive enable control bit
TB8 in modes 2&3, 9th bit transmitted
RB8 in modes 2&3, 9th bit received
TI transmit interrupt flag
RI receive interrupt flag

SBUF Serial port Buffer register

PCON Power Control register
PCON.7 double baud rate control
PCON.4 ALE disable (0=normal, 1=forces ALE high)
PCON.3 general purpose flag
PCON.2 general purpose flag
PCON.1 power-down control bit (recoverable with hard reset)
PCON.0 idle-mode control (recoverable with enabled interrupt)

PSW Program Status Word
CY carry flag
AC auxiliary carry flag
F0 general purpose flag 0
RS1 register bank select control bits
RS0 active register bank = [0,1,2,3]
OV overflow flag
F1 general purpose flag 1
P parity of ACC

DPP Data Pointer Page

DPH,DPL (DPTR) Data Pointer

ACC Accumulator

B auxiliary math register