

REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic ready for layout - Alpha Release	04/01/07	RRP
B	Pre-production release - Beta Release	07/01/07	RRP
C	Production release for 0.50 mm	09/01/07	RRP
D	Pre-production release for 0.65 mm	09/28/07	RRP

Memory Address Table		
CHIP SELECT	BASE ADDRESS HEX	FUNCTION
CE0 - NAND CS0	0x0200 0000	NAND FLASH CS0 R/W
CE0 - NAND CS1	0x0200 4000	NAND FLASH CS1 R/W
CE1 - PHY/MAC CHIP	0x0401 4000	DM9000A READ WRITE

ARM ADDRESSING															
A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	WORD
X	X	1	1		1	1	1	1	1	1	1	1	1	1	1
					F				F				F		

I2C Address Table			
ADDRESS		DEVICE	FUNCTION
HEX	BINARY		
0x25	00100011B	MSP430	RTC,IR CTL, IO CTL, POWER MONITOR
0x1B	00011011B	AIC33	AUDIO CODEC - 00110(MFP1)(MFP0)
0x5D	01011101B	TVP5146	VIDEO DECODER - 101110(I2CA)

SCHEMATIC CONTENTS

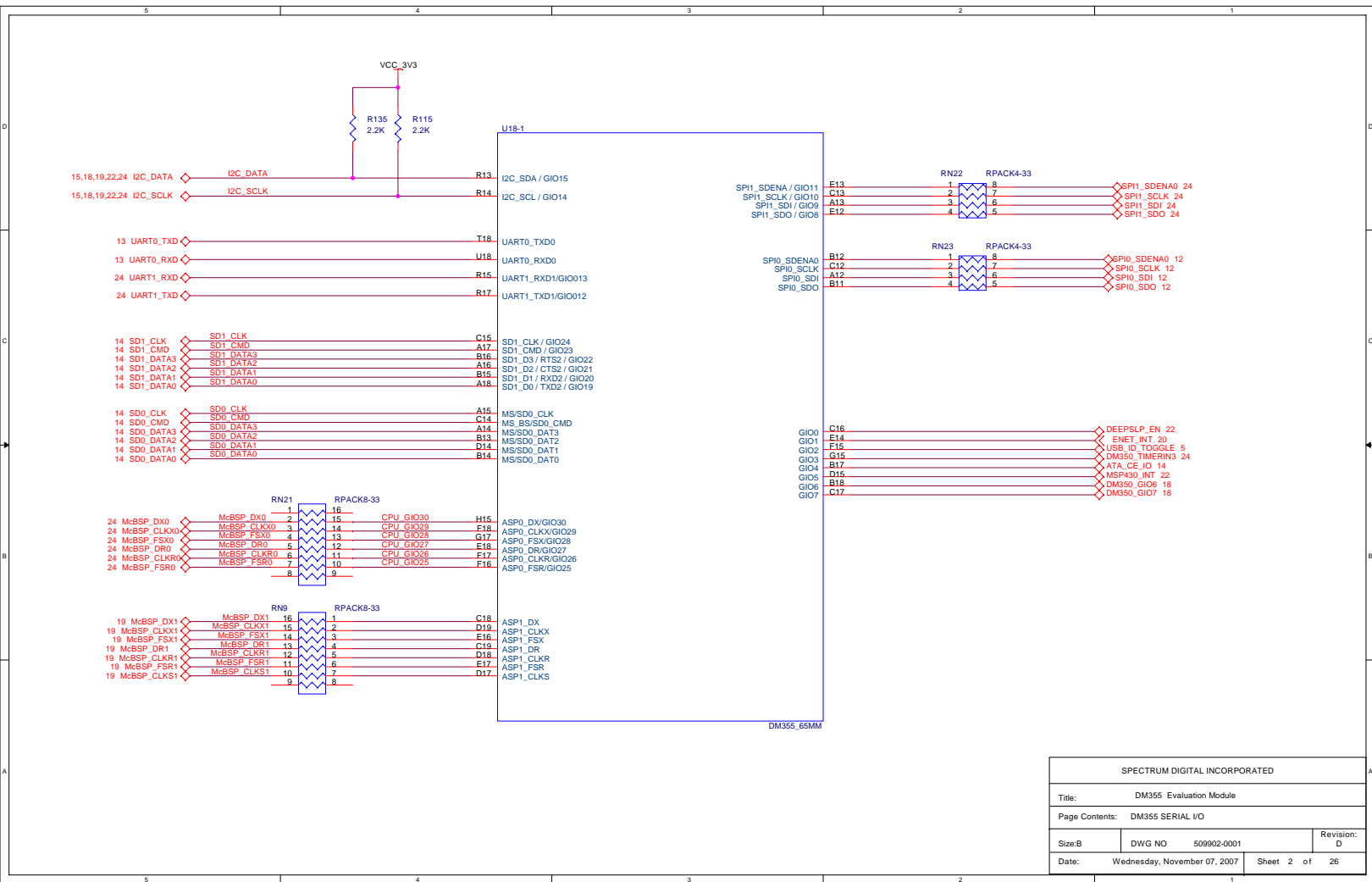
- SHEET01 - TITLE
- SHEET02 - DM355 SERIAL I/O
- SHEET03 - DM355 DDR2 INTERFACE
- SHEET04 - DM355 EMIF
- SHEET05 - DM355 USB
- SHEET06 - DM355 VIDEO
- SHEET07 - DM355 JTAG,CLKS,RESET
- SHEET08 - DM355 POWER/GND-pins
- SHEET09 - DM355 DECOUPLING CAPS

- SHEET10 - DDR2 MEMORY
- SHEET11 - JTAG CONNECTORS
- SHEET12 - NAND FLASH, SPI EEPROM, EMIF I/O DC
- SHEET13 - RS232 INTERFACE
- SHEET14 - SD/MMC IF - CE ATA IF
- SHEET15 - VIDEO INPUT MULTIPLEXER
- SHEET16 - IMAGER INTERFACE
- SHEET17 - 5146 DECODER
- SHEET18 - VIDEO DAUGHTER CARD IF
- SHEET19 - AIC33

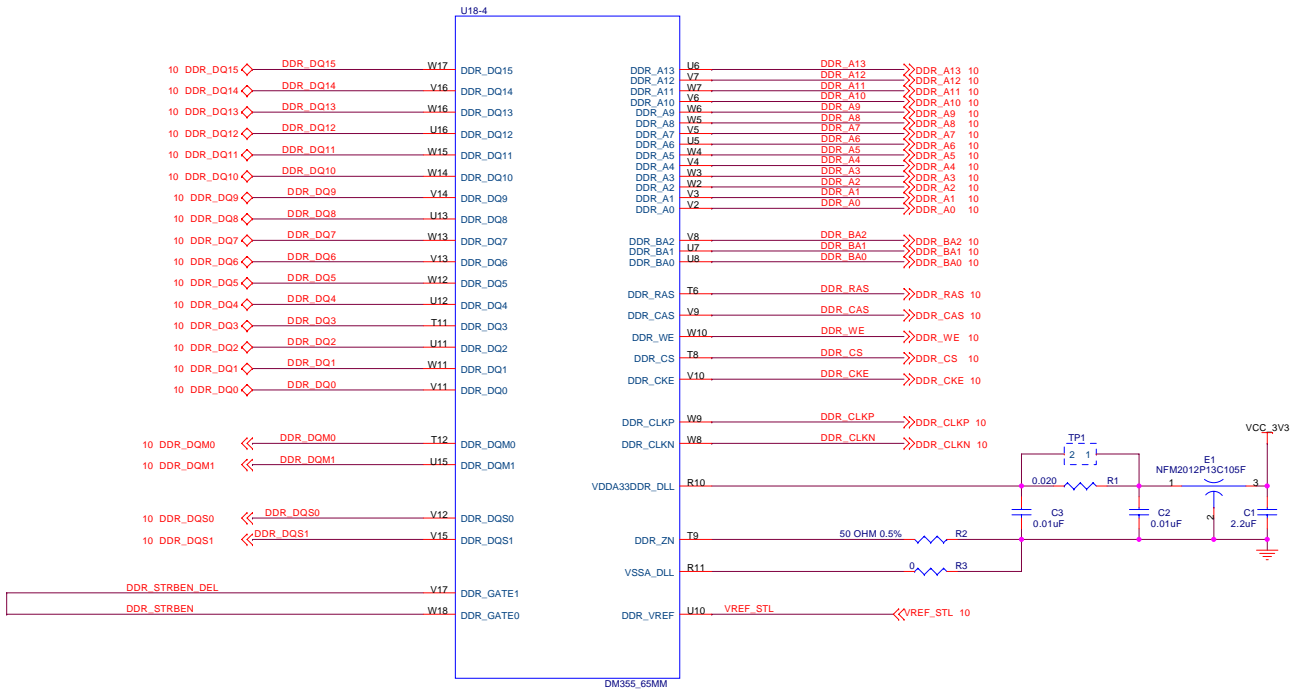
- SHEET20 - DM9000A ENET CONTROLLER
- SHEET21 - ETHERNET CONNECTOR
- SHEET22 - MSP430
- SHEET23 - LEDS/SWITCHED ETC
- SHEET24 - I/O DAUGHTER CARD IF
- SHEET26 - CORE PWR SUPPLY,MSP430 PWR SUPPLY
- SHEET27 - 3V3 AND 1V8 POWER SUPPLY

REVISION STATUS OF SHEETS										DATE	DATE	
A	A	A	A							DATE	DATE	
31	32	33	34							ENR	R.R.P.	04/01/2007
										CHC	T.W.K.	04/01/2007
										ENGR	R.R.P.	04/01/2007
										ENGR-MGR	R.R.P.	04/01/2007
										DA	C.M.D.	04/01/2007
										RFQ	R.R.P.	04/01/2007
										RLSE	R.R.P.	04/01/2007
1	2	3	4	5	6	7	8	9	10	APPLICATION		

SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: TITLE SHEET			
Size: B	DWG NO	509902-0001	Revision: D2
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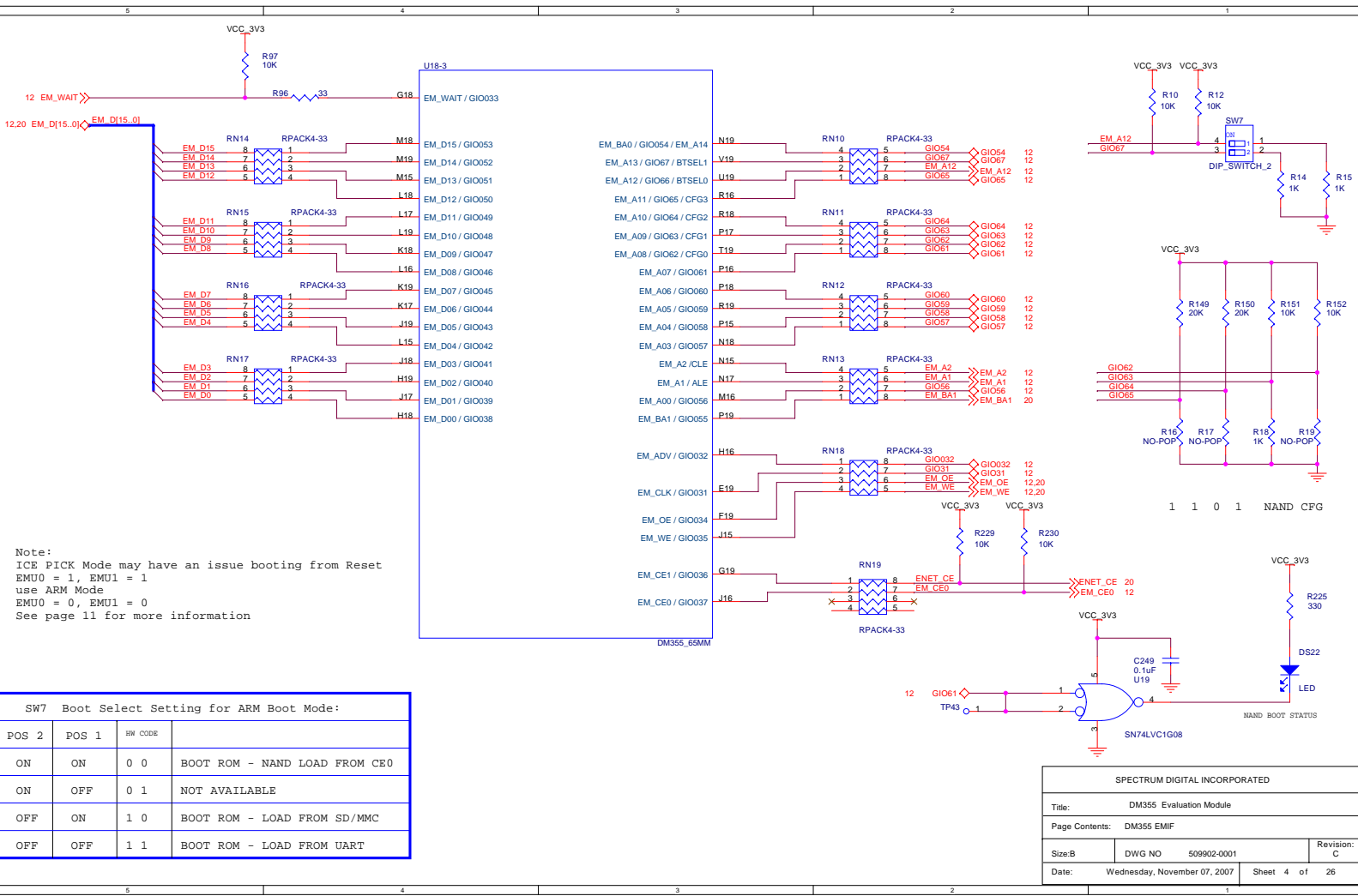
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: DM355 SERIAL I/O			
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Trace to DDR memory
for delay compensation

This net is equal to the DDR_CLKP (or DDR_CLKN)
plus
the length of DDR_DQXX Average Trace length

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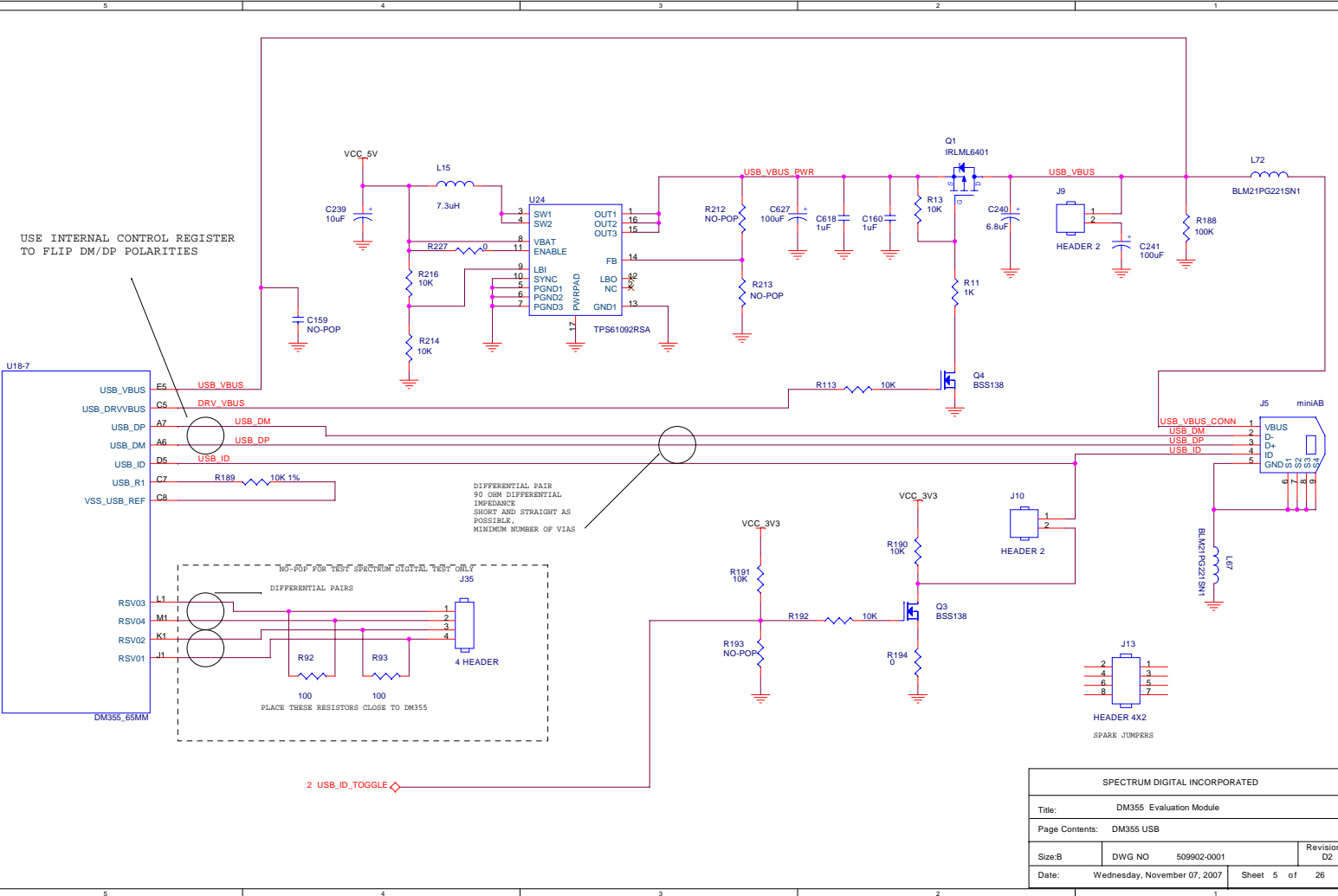


Note:
 ICE PICK Mode may have an issue booting from Reset
 EMU0 = 1, EMU1 = 1
 use ARM Mode
 EMU0 = 0, EMU1 = 0
 See page 11 for more information

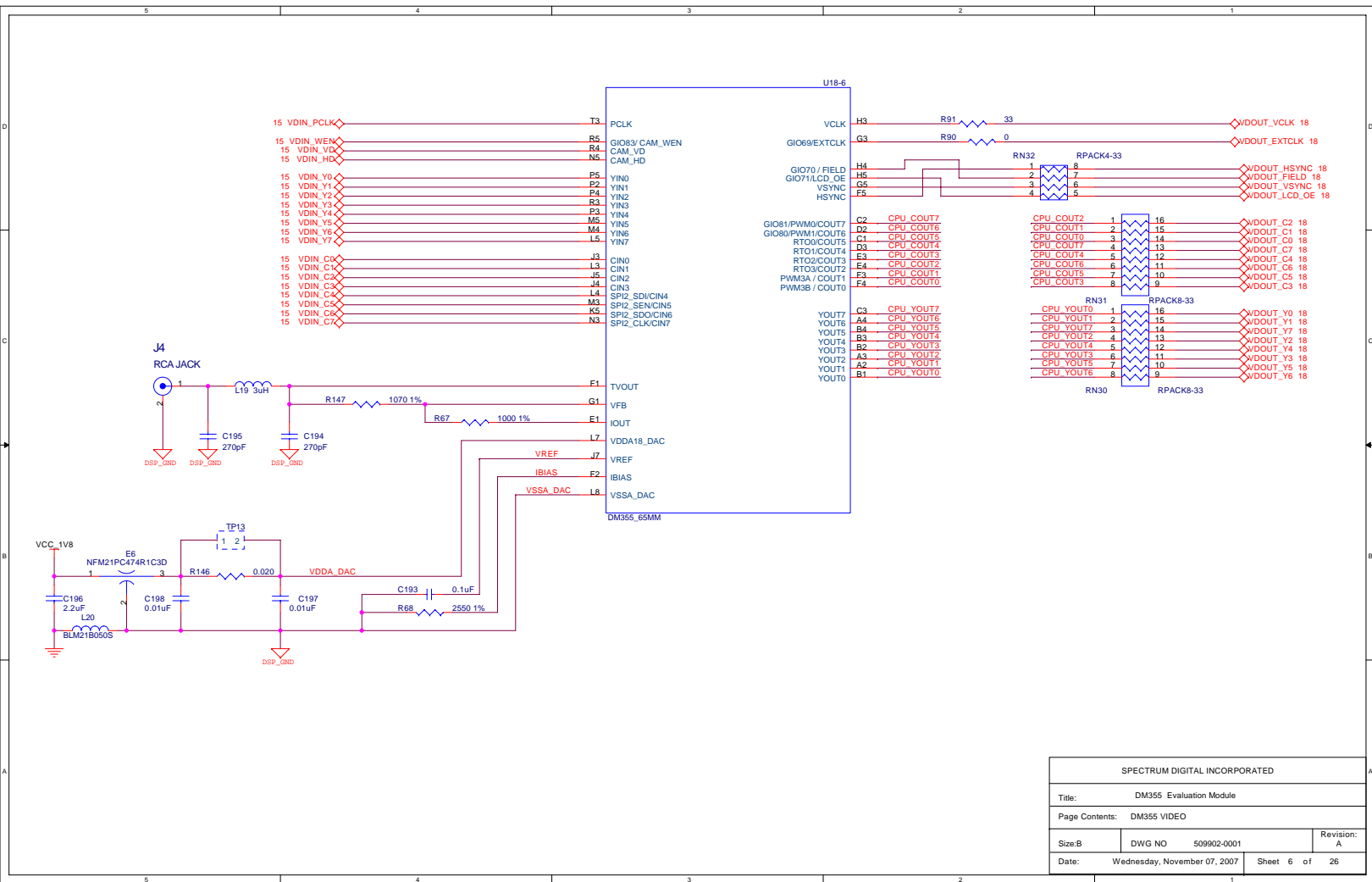
SW7 Boot Select Setting for ARM Boot Mode:			
POS 2	POS 1	HW CODE	
ON	ON	0 0	BOOT ROM - NAND LOAD FROM CE0
ON	OFF	0 1	NOT AVAILABLE
OFF	ON	1 0	BOOT ROM - LOAD FROM SD/MMC
OFF	OFF	1 1	BOOT ROM - LOAD FROM UART

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Title: DM355 Evaluation Module			
Page Contents: DM355 EMIF			
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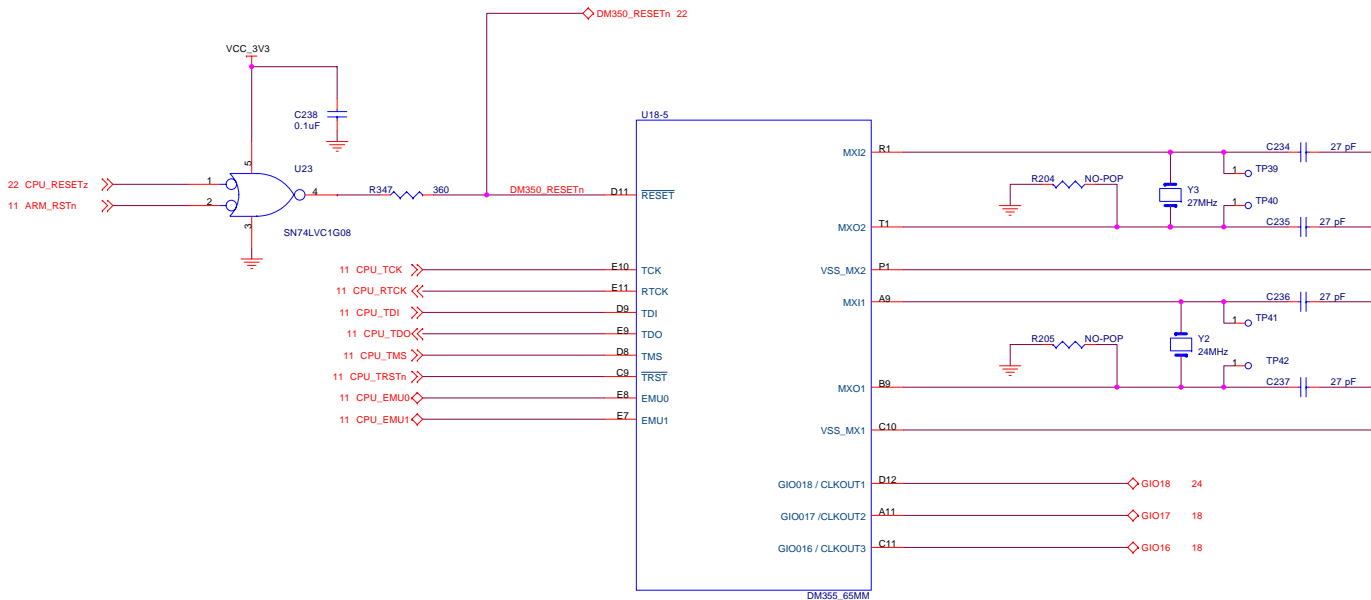
USE INTERNAL CONTROL REGISTER TO FLIP DM/DP POLARITIES



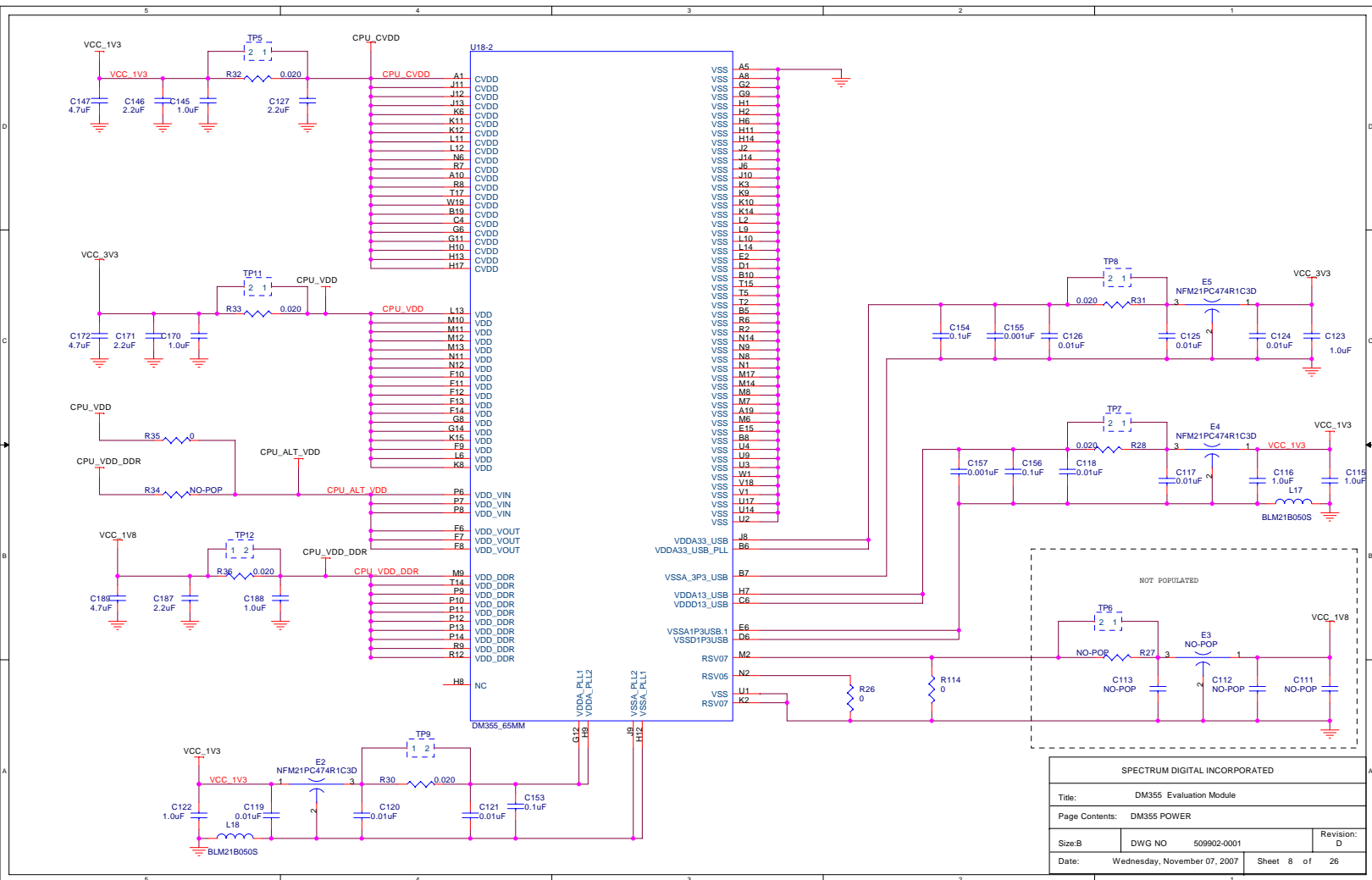
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: DM355 USB			
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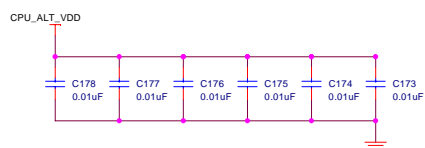
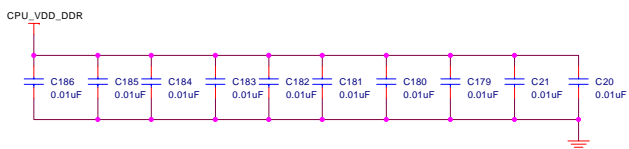
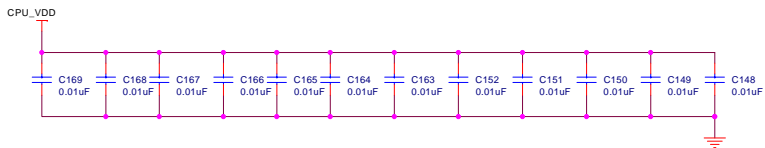
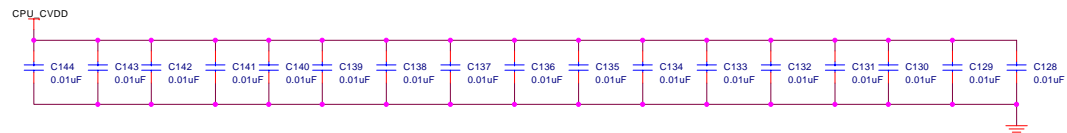
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: DM355 VIDEO			
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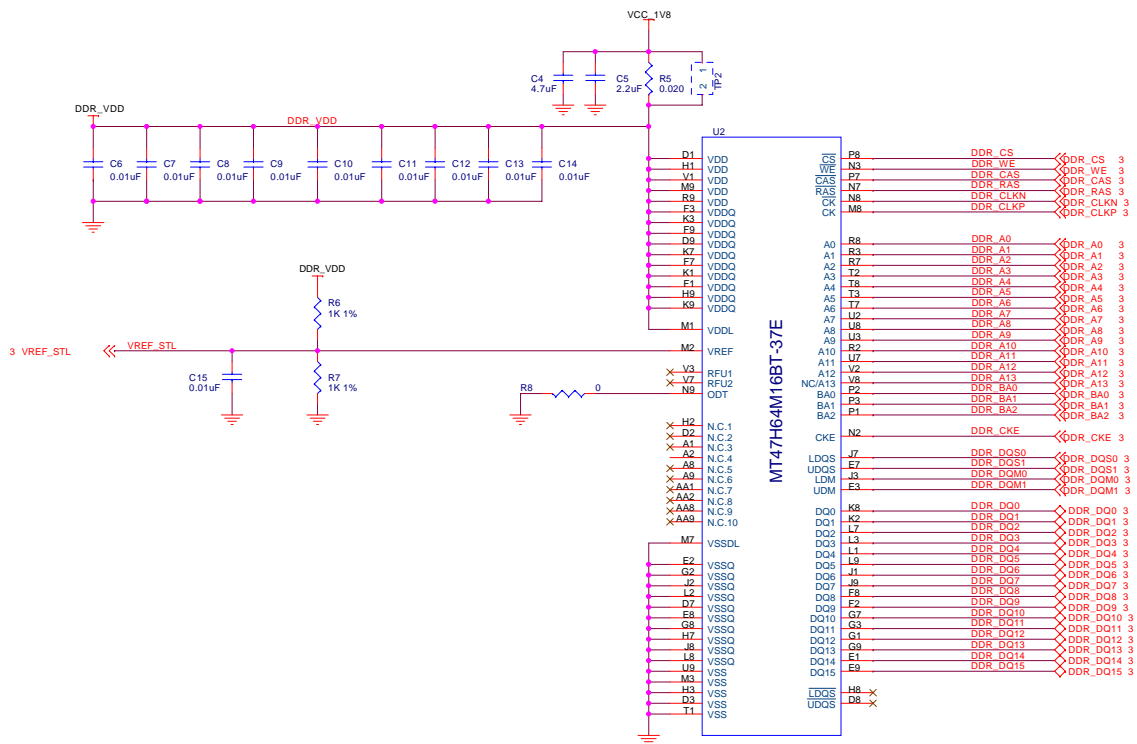
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: DM355 JTAG.RESET.CLOCKS			
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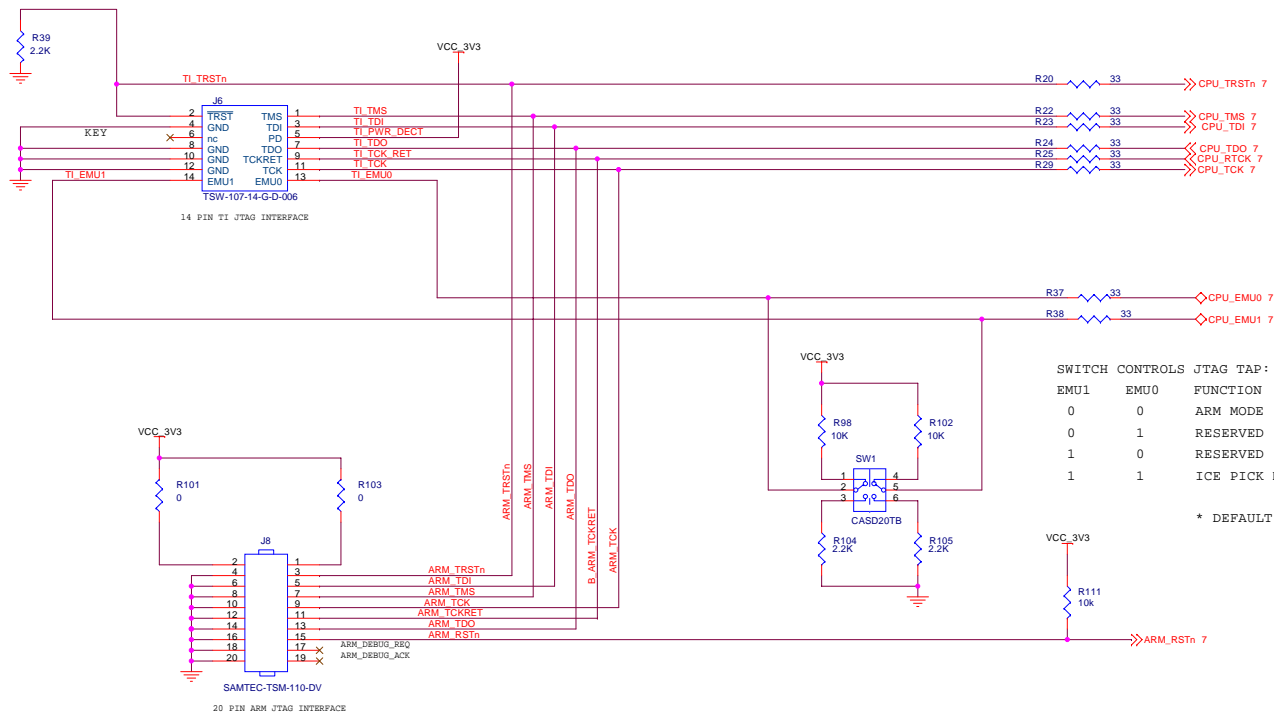
SPECTRUM DIGITAL INCORPORATED			
Title:	DM355 Evaluation Module		
Page Contents:	DM355 POWER		
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Page Contents: DDR2 MEMORY			
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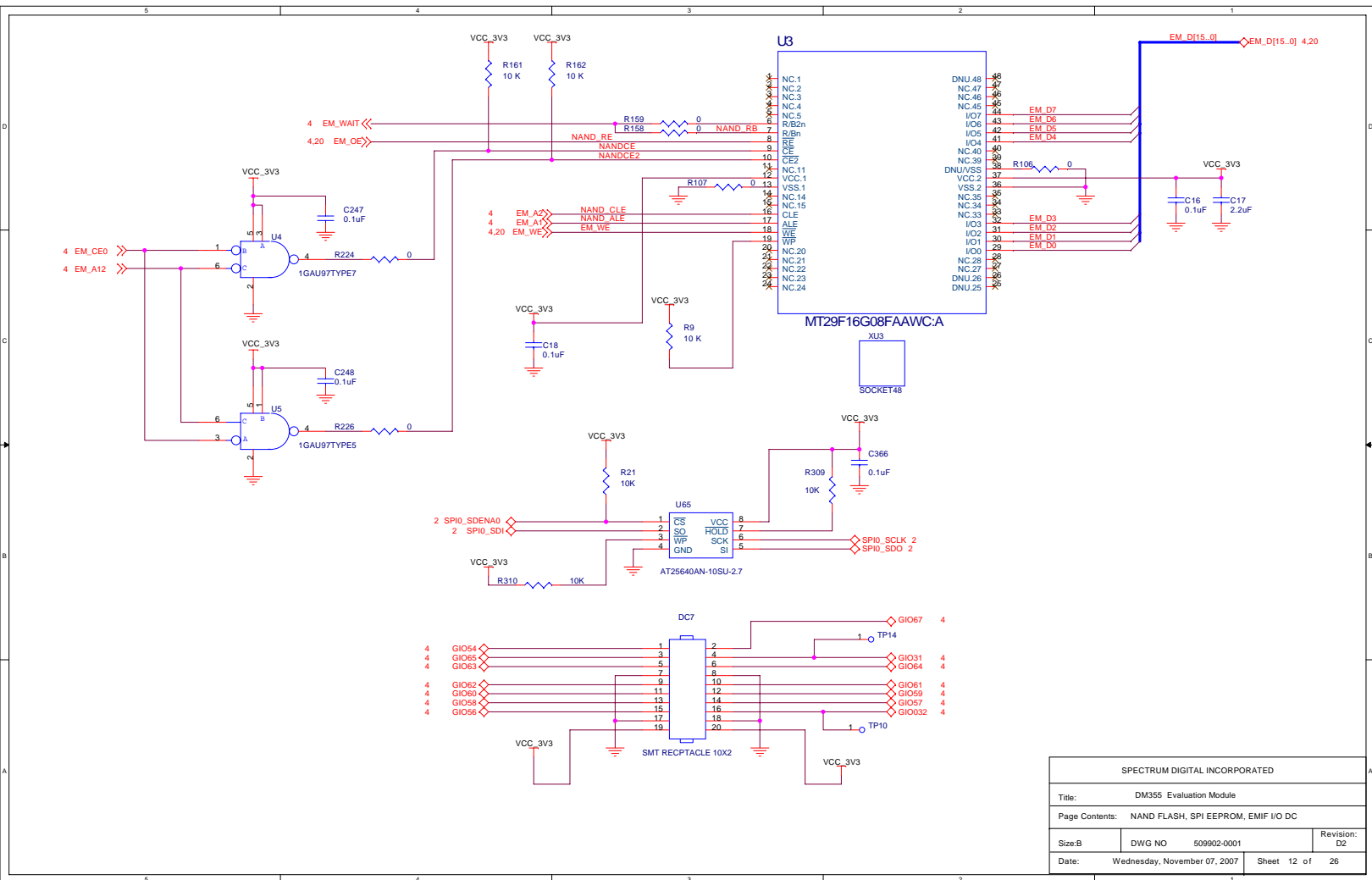


SWITCH CONTROLS JTAG TAP:

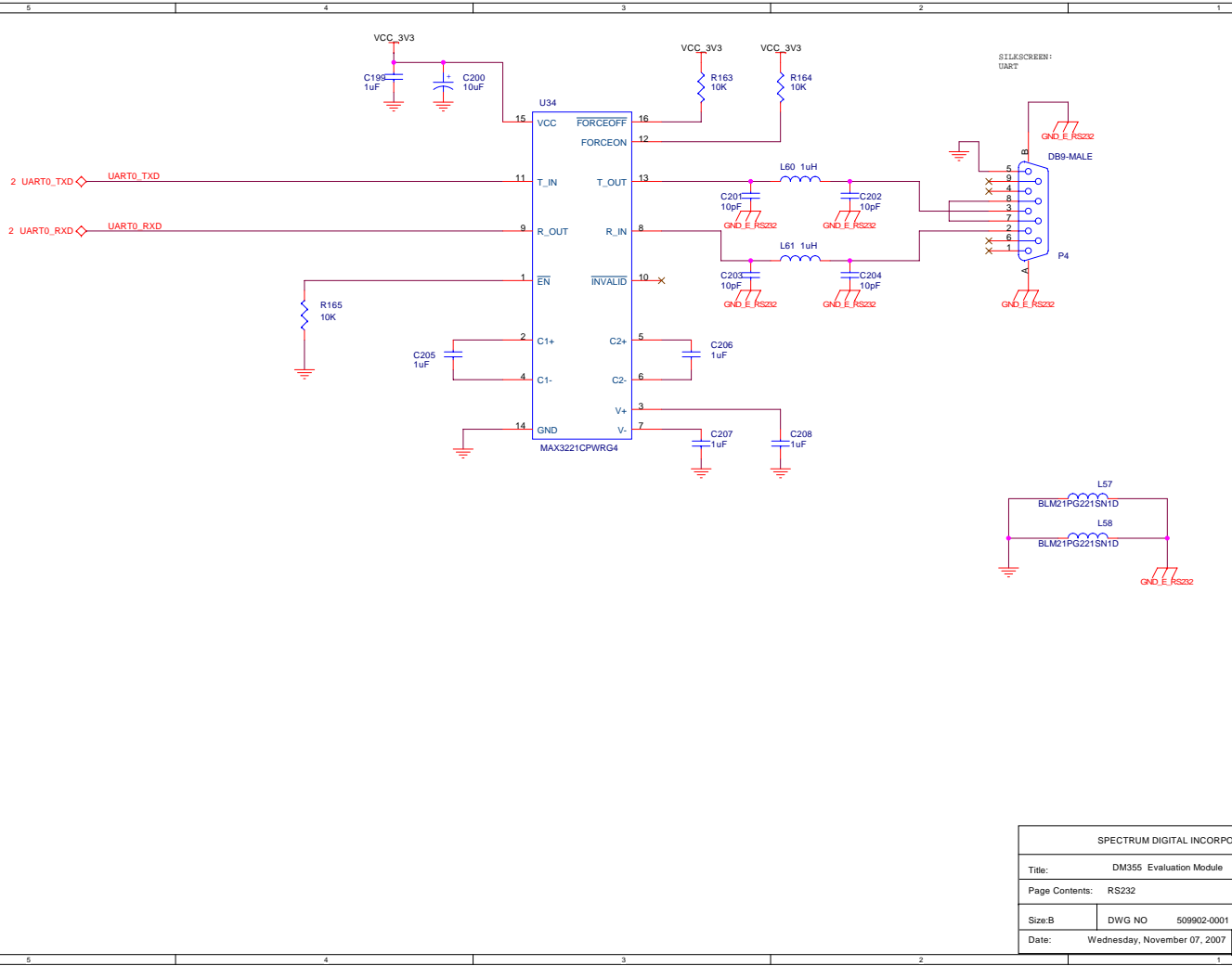
EMU1	EMU0	FUNCTION
0	0	ARM MODE
0	1	RESERVED
1	0	RESERVED
1	1	ICE PICK MODE *

* DEFAULT

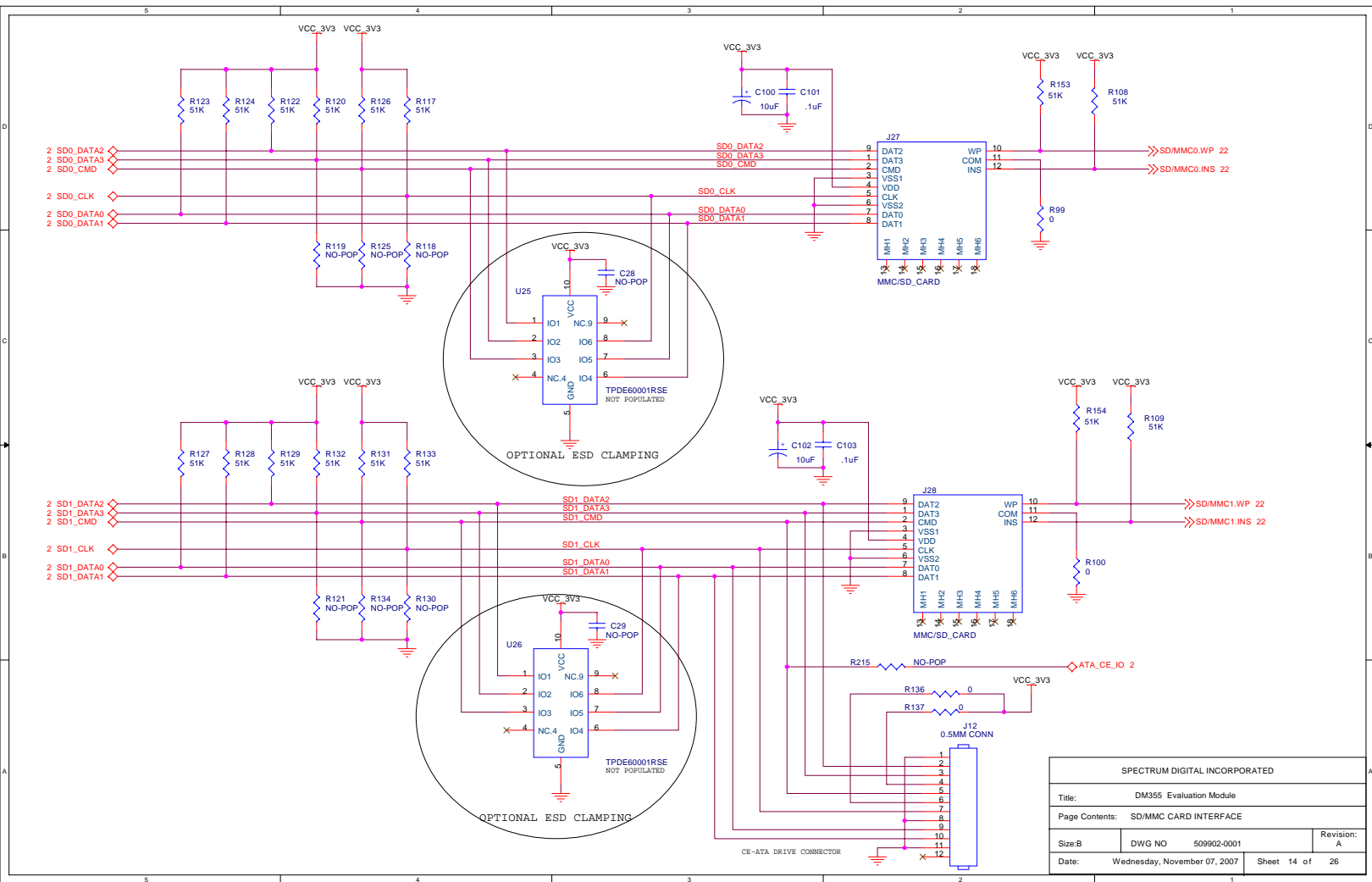
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: JTAG INTERFACE			
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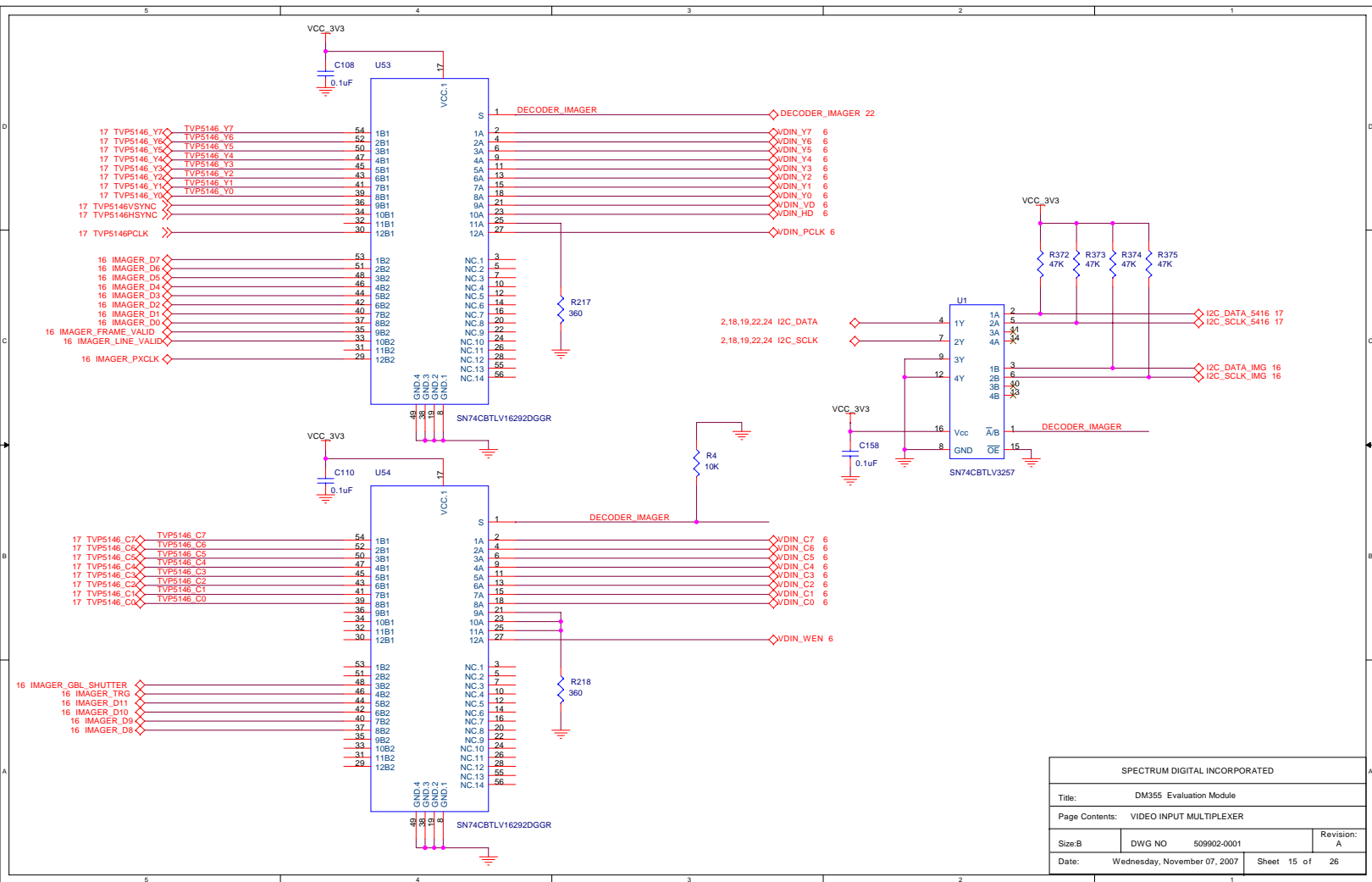


SPECTRUM DIGITAL INCORPORATED			
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Page Contents: NAND FLASH, SPI EEPROM, EMIF I/O DC			
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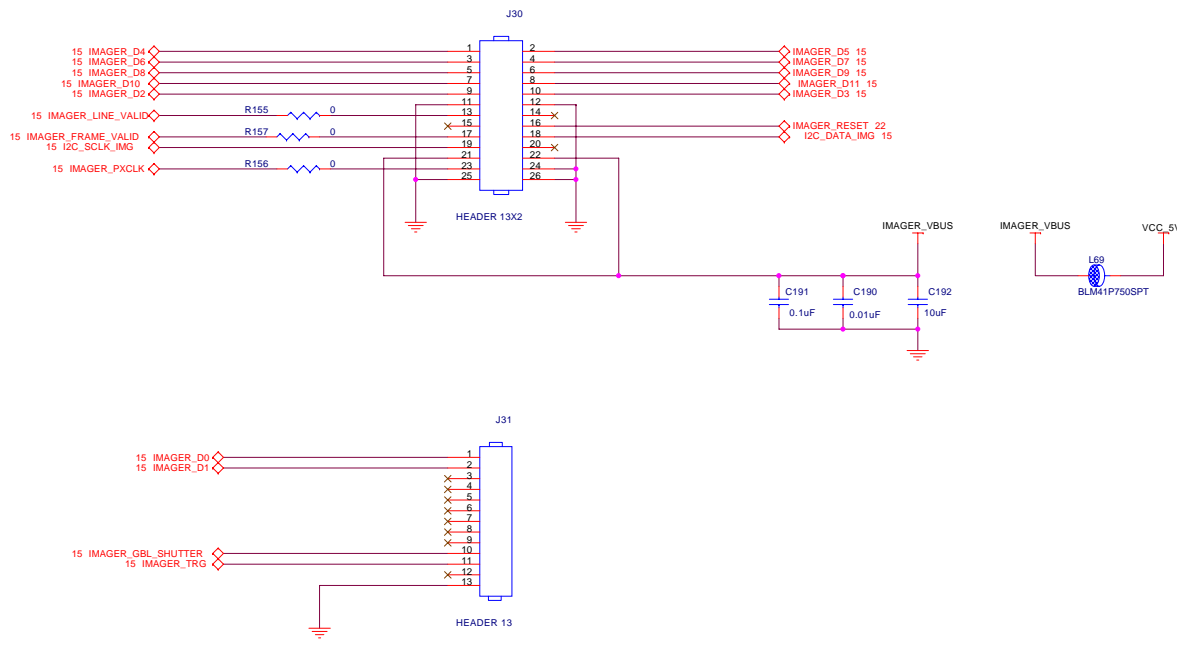


SPECTRUM DIGITAL INCORPORATED		
Title: DM355 Evaluation Module		
Page Contents: RS232		
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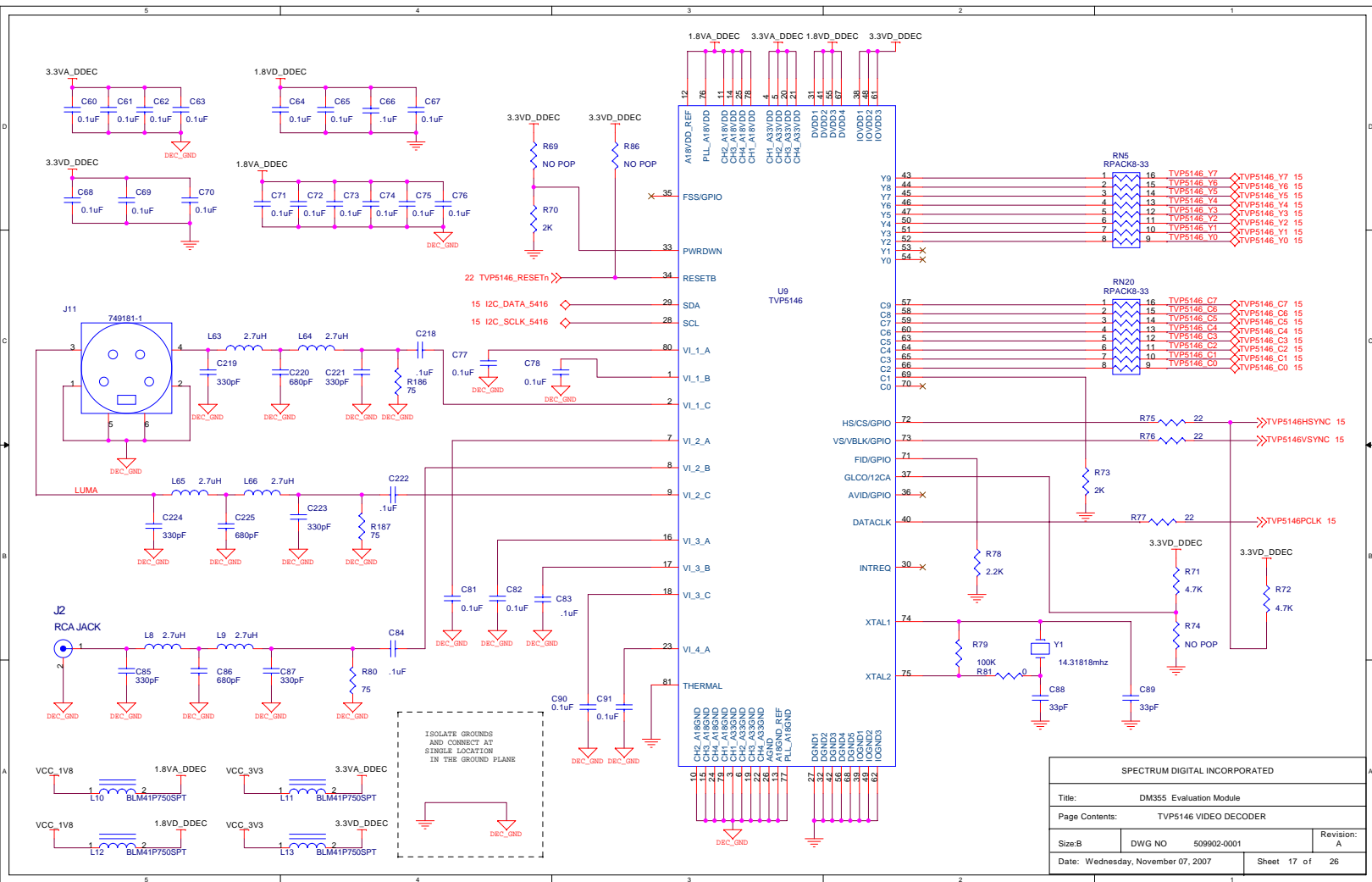


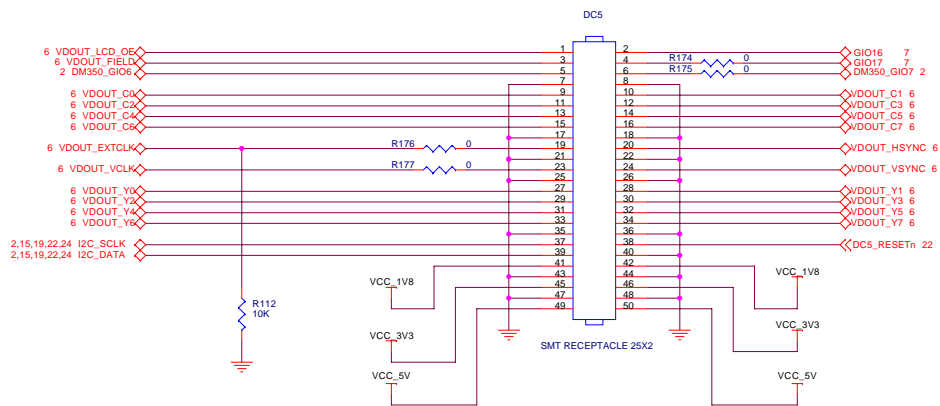


SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: VIDEO INPUT MULTIPLEXER			
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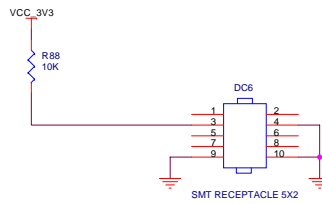


SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: IMAGER INTERFACE			
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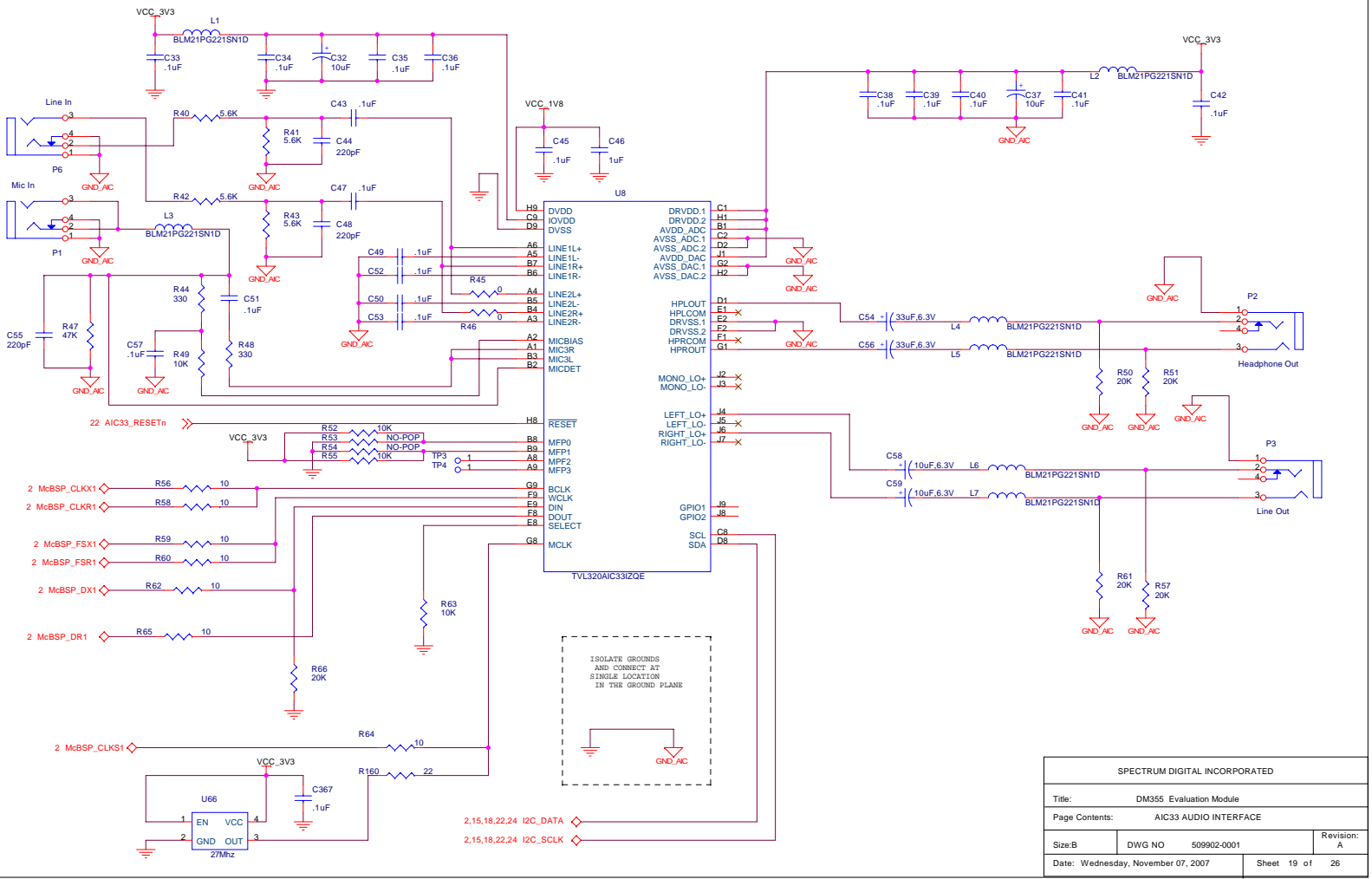


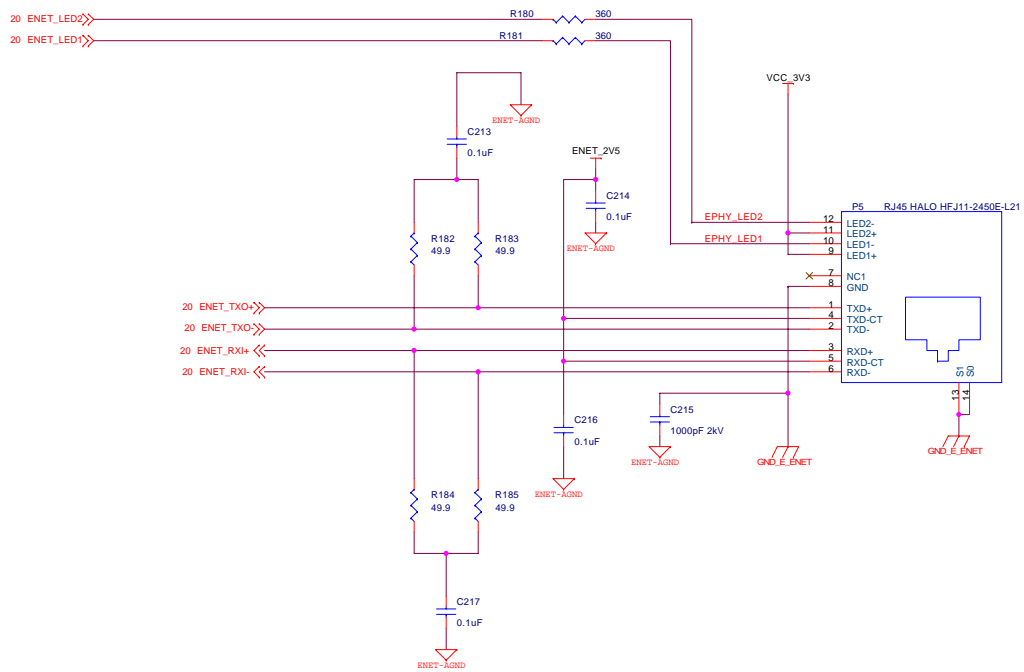


VIDEO OUTPUT CONNECTOR

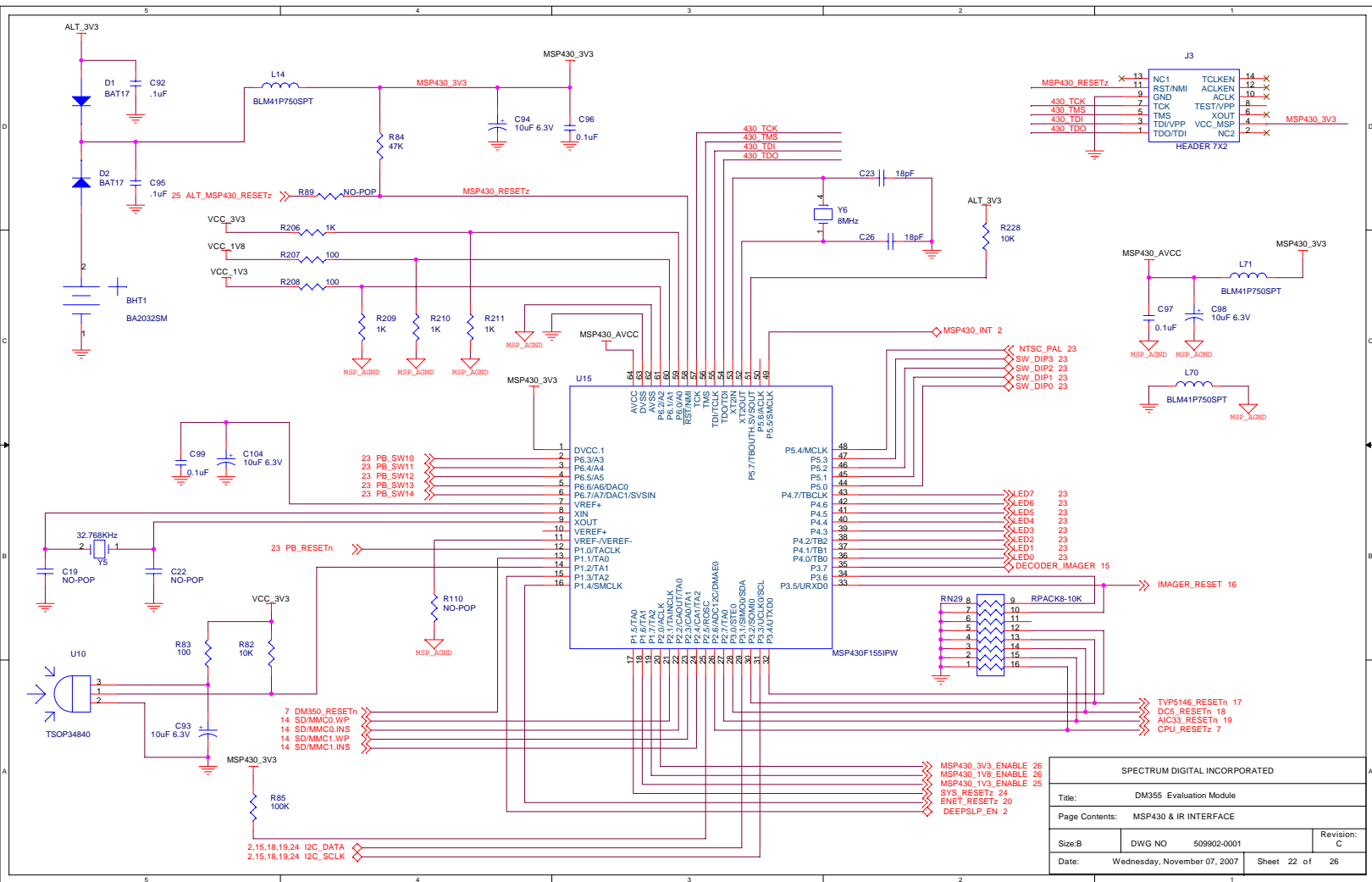


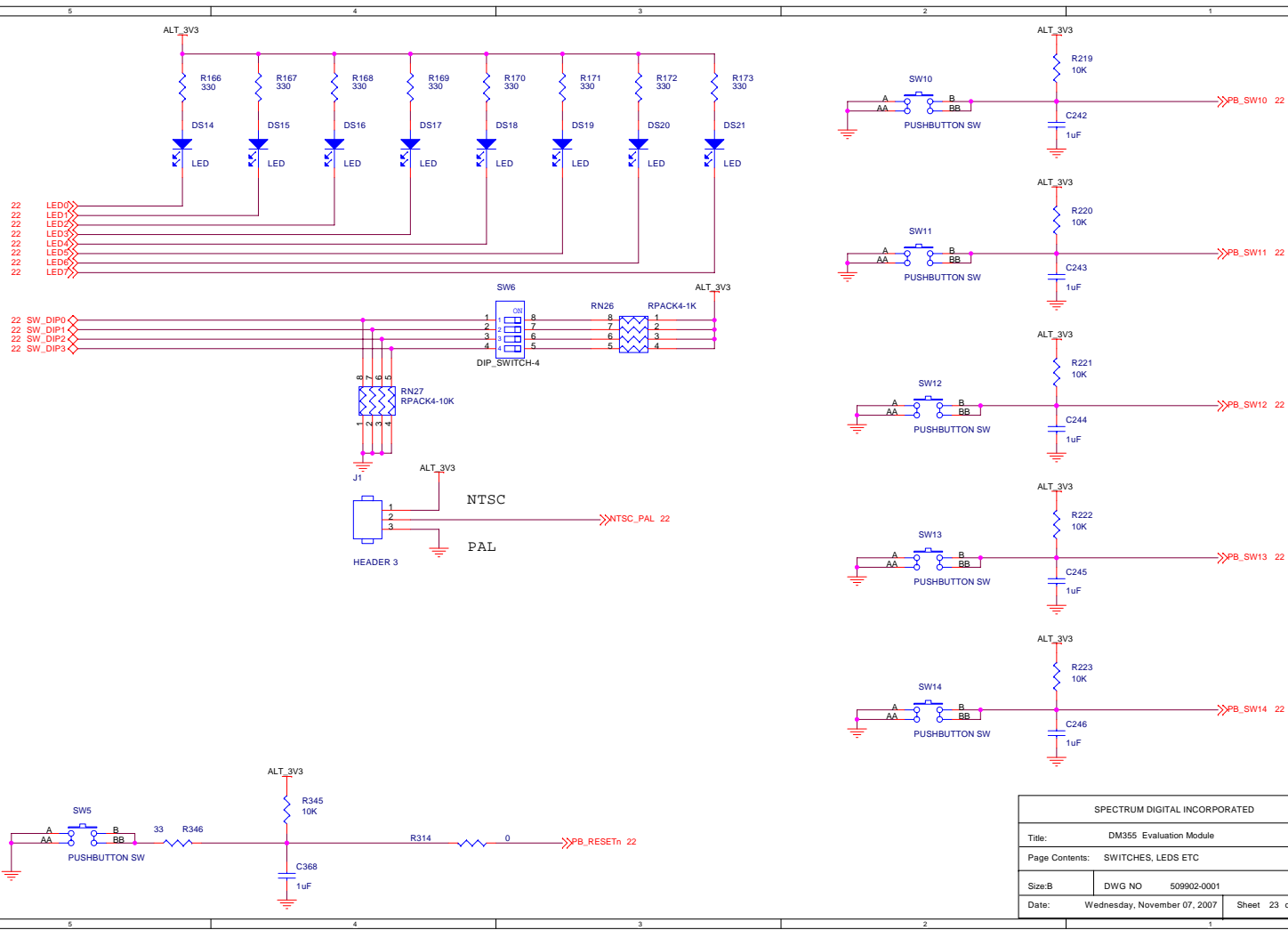
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: THS8200 DAUGHTER CARD INTERFACE			
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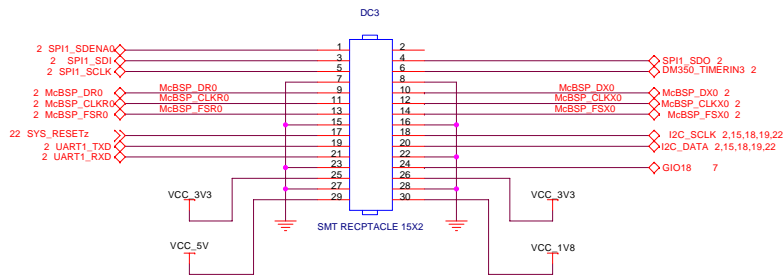


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Title: DM355 Evaluation Module			
Page Contents: ETHERNET OUTPUT			
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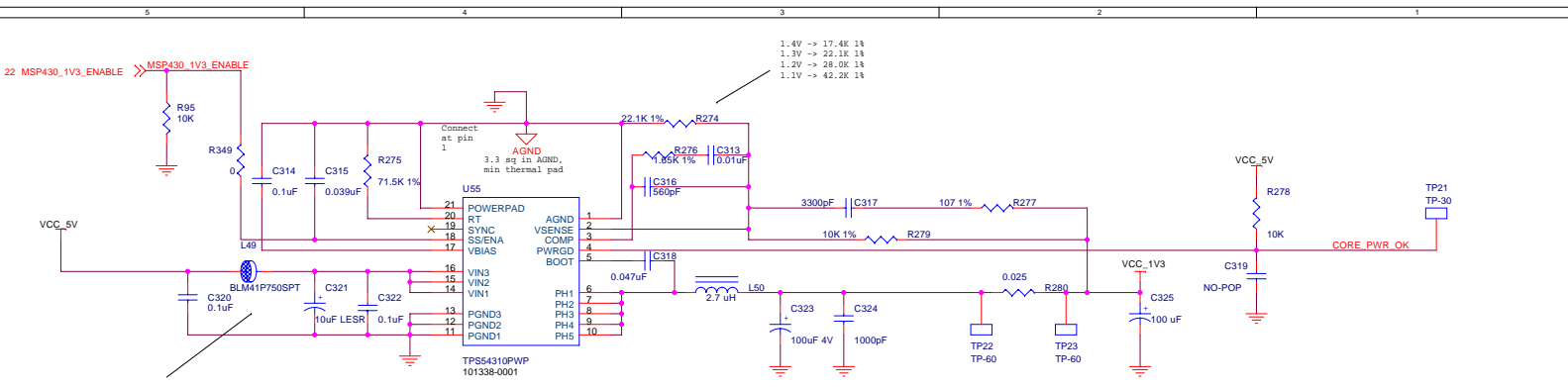




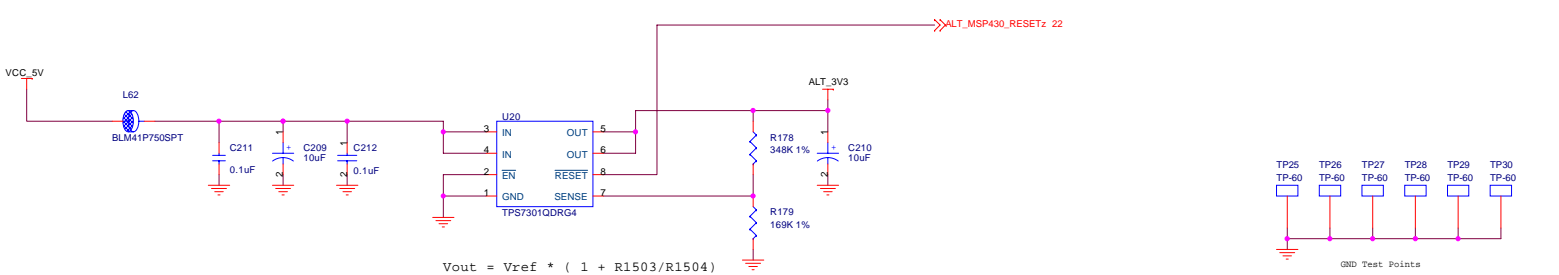
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
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Title: DM355 Evaluation Module			
Page Contents: I/O DAUGHTER CARD INTERFACE			
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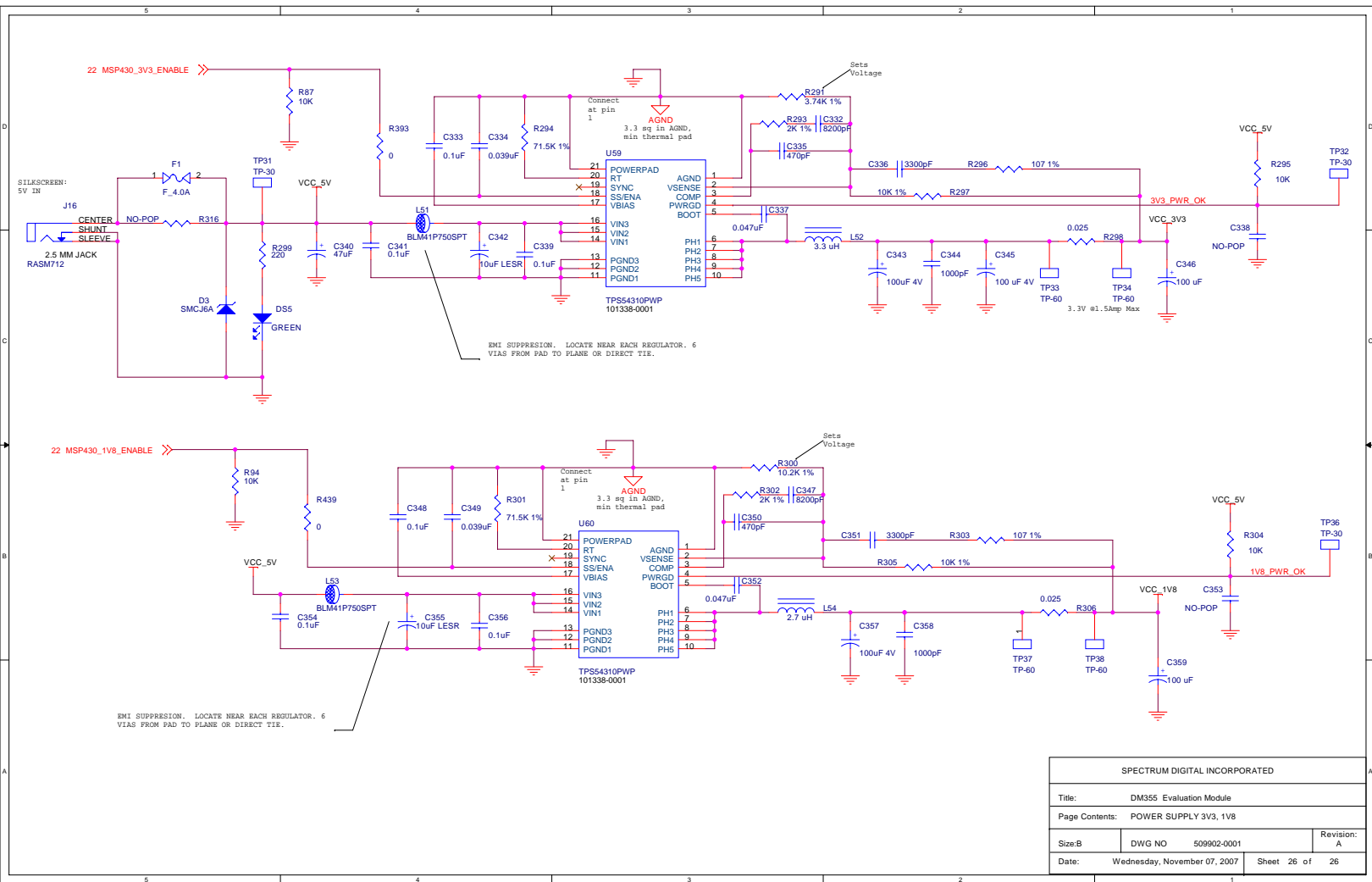
EMI SUPPRESSION. LOCATE NEAR EACH REGULATOR. 6 VIAS FROM PAD TO PLANE OR DIRECT TIE.



$$V_{out} = V_{ref} * (1 + R_{1503}/R_{1504})$$

$V_{ref} = 1.182 \text{ Volts}$
 $V_{out} = 3.6 \text{ volts}$
 $R_{1503} = 346K$

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Page Contents: POWER SUPPLY MSP430_3V3, DSP CORE(1V3)			
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